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ML510 Embedded Development Platform

User Guide

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
08/25/08	1.0	Initial Xilinx release.
08/29/08	1.0.1	Minor typographical edits.
12/11/08	1.1	• Added “System Monitor” section. • Corrected Table 1-40, page 71, pins A15 and A16. • Removed support for unbuffered DIMMs.
06/16/11	1.2	Corrected FPGA pin “H7” to pin ”J15” in section “CPU Reset (SW2),” page 58.

Table of Contents

Appendix A: References

About This Guide

This manual accompanies the ML510 series of Embedded Development Platforms and contains information about the ML510 hardware and software tools.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "ML510 Embedded Development Platform" provides an overview of the embedded development platform and details the components and features of the ML510 board
- Appendix A, "References"

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.
- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.
- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT and SXT platform devices that are PCI Express® compliant.
- Virtex-5 FPGA User Guide

  Chapters in this guide cover the following topics: Clocking resources, Clock Management Technology (CMT), Phase-Locked Loops (PLLs), block RAM, Configurable Logic Blocks (CLBs), SelectIO™ resources, and SelectIO logic resources
- Virtex-5 FPGA RocketIO™ GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform devices.
- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platform devices.

- XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA Packaging Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-5 Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Documentation" for details.

Convention	Meaning or Use	Example
Red text	Cross-reference link to a location in another document	See Figure 5 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

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Chapter 1

ML510 Embedded Development Platform

Overview

The ML510 series of Embedded Development Platforms offer designers a versatile Virtex®-5 FXT platform for rapid prototyping and system verification. In addition to the more than 130,000 logic cells, over 10,700 kb of block RAM, dual IBM PowerPC® 440 (PPC440) processors, and RocketIO transceivers available in the FPGA, the ML510 provides an onboard Ethernet MAC PHY, DDR2 memory, multiple PCI bus slots, and standard front panel interface ports within an ATX form factor motherboard. An integrated System ACE™ CompactFlash (CF) controller is deployed to perform board bring-up and to load applications from the CompactFlash card.

The ML510 website contains up-to-date documentation and files, including tutorials, device data sheets, reference designs, and utilities. The *Embedded Processor Block in Virtex-5 FPGAs Reference Guide* [Ref 4] should be reviewed as well as the data sheets corresponding to the devices listed in "Detailed Description."

The setup and quickstart documentation highlights the functionality of the ML510, using the applications contained on the CompactFlash card. The reference designs were produced using the Xilinx® Embedded Development Kit (EDK), ISE, and Answer Browser solution records. Tutorials, in coordination with Xilinx documentation for EDK, ISE, and the Answer Browser, describe how the reference designs and applications were produced. These tutorials can be used to re-create the provided applications and also as a basis for the development of new designs. Xilinx EDK provides for the development of basic board-specific systems, beginning with Base System Builder (BSB), to highly customized systems that leverage the flexibility of Xilinx Platform Studio (XPS) and the EDK intellectual property (IP).

Package Contents

- Xilinx Virtex-5 FPGA ML510 Embedded Development Platform
- System ACE CompactFlash card
- Power supply
- 2 x 512 MB DDR2 DIMMs
- 16-character LCD display

Additional Information

Additional information and support material is located at:

- http://www.xilinx.com/ml510

This information includes:

- Current version of this user guide in PDF format
- Example design files for demonstration of Virtex-5 FPGA features and technology
- Demonstration hardware and software configuration files for the System ACE controller, Platform Flash configuration storage device, CPLD, and linear flash chips
- EDK reference design files
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Allegro PCB format
- Gerber files for the PC board (Many free or shareware Gerber file viewers are available on the internet for viewing and printing these files.)
- Additional documentation, errata, frequently asked questions, and the latest news

For information about the Virtex-5 family of FPGA devices, including product highlights, data sheets, user guides, and application notes, see the Virtex-5 FPGA website at www.xilinx.com/virtex5. Additional information is available from the data sheets and application notes from the component manufacturers.

Features

- ATX form factor motherboard and ATX-compliant power supply
- Dual DDR2 registered DIMMs; each 512 MB density and 72 bits wide
- 512 MB CompactFlash (CF) card and System ACE CF controller for configuration*
- Intel P30 StrataFlash linear flash chip (256 Mb)
- Two onboard 10/100/1000 Ethernet PHYs with RJ-45 connectors
- PCI Express interface and MIC2592B PCI Express power controller
- Two UARTs with RS-232 connectors
- DVI graphics interface
- LEDs, LCD*, and switches
- 32/33 PCI subsystem
  - Two 3.3V slot and two 5V slots
  - ALi South Bridge SuperIO controller
    - PS/2 mouse and keyboard connectors
    - 3.5 mm headphone and microphone connectors
    - Two USB peripheral ports
- Two serial ATA connectors
- Xilinx Personality Module (XPM) interface for access to:
  - RocketIO GTX transceivers
  - SPI4.2
  - GPIO
  - Power

- JTAG and trace debug ports
- High-speed I/O through RocketIO GTX transceivers
- Encryption battery
- Fan controller
- Onboard power regulators for all necessary voltages
- IIC/SMBus interface*
  - LTC1694 SMBus accelerator
  - RTC8566 Real Time Clock (RTC)
  - 64 kb 24LC64 EEPROM
  - LM87 voltage/temp monitor
  - Two DDR2 DIMMs with SPD EEPROMs
- SPI EEPROM (64 Kb)*

Note: * Compatible with EDK supported IP and software drivers

Block Diagram

Figure 1-1 shows a high-level block diagram of the ML510 and its peripherals.

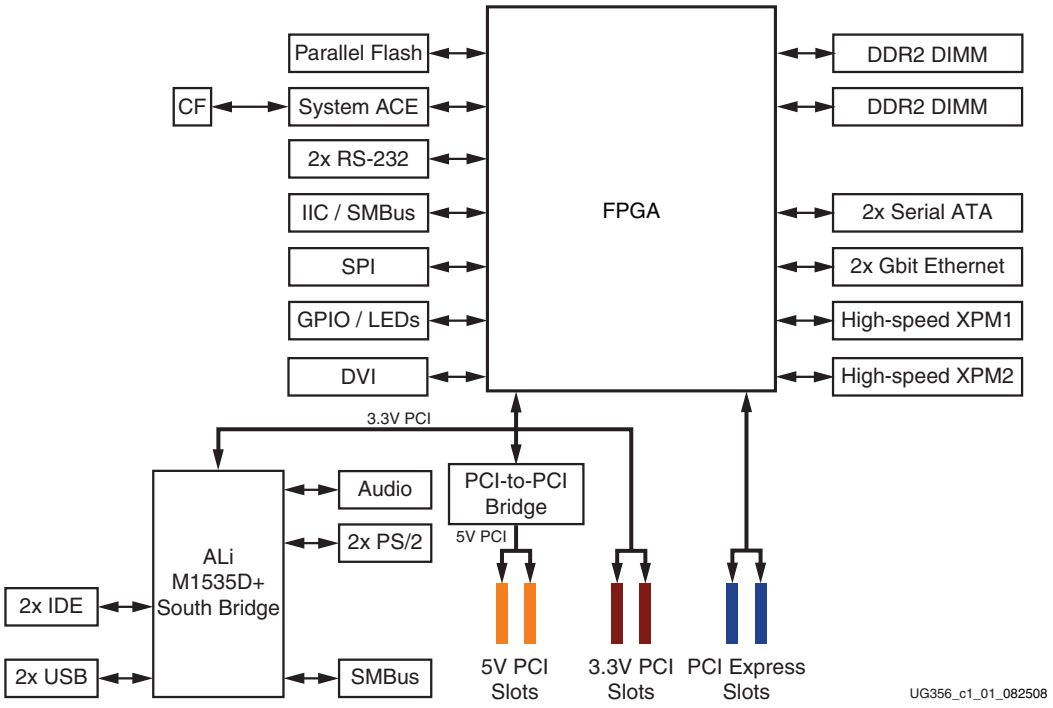

Figure 1-1: **ML510 High-Level Block Diagram**

Related Xilinx Documents

Prior to using the ML510 Embedded Development Platform, users should be familiar with Xilinx resources. See Appendix A, "References" for direct links to Xilinx documentation. See the following locations for additional documentation on Xilinx tools and solutions:

- EDK: www.xilinx.com/edk

- ISE: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Intellectual Property: www.xilinx.com/ipcenter

Detailed Description

The ML510, shown in Figure 1-2, is an example of the ML510 series described in this user guide.

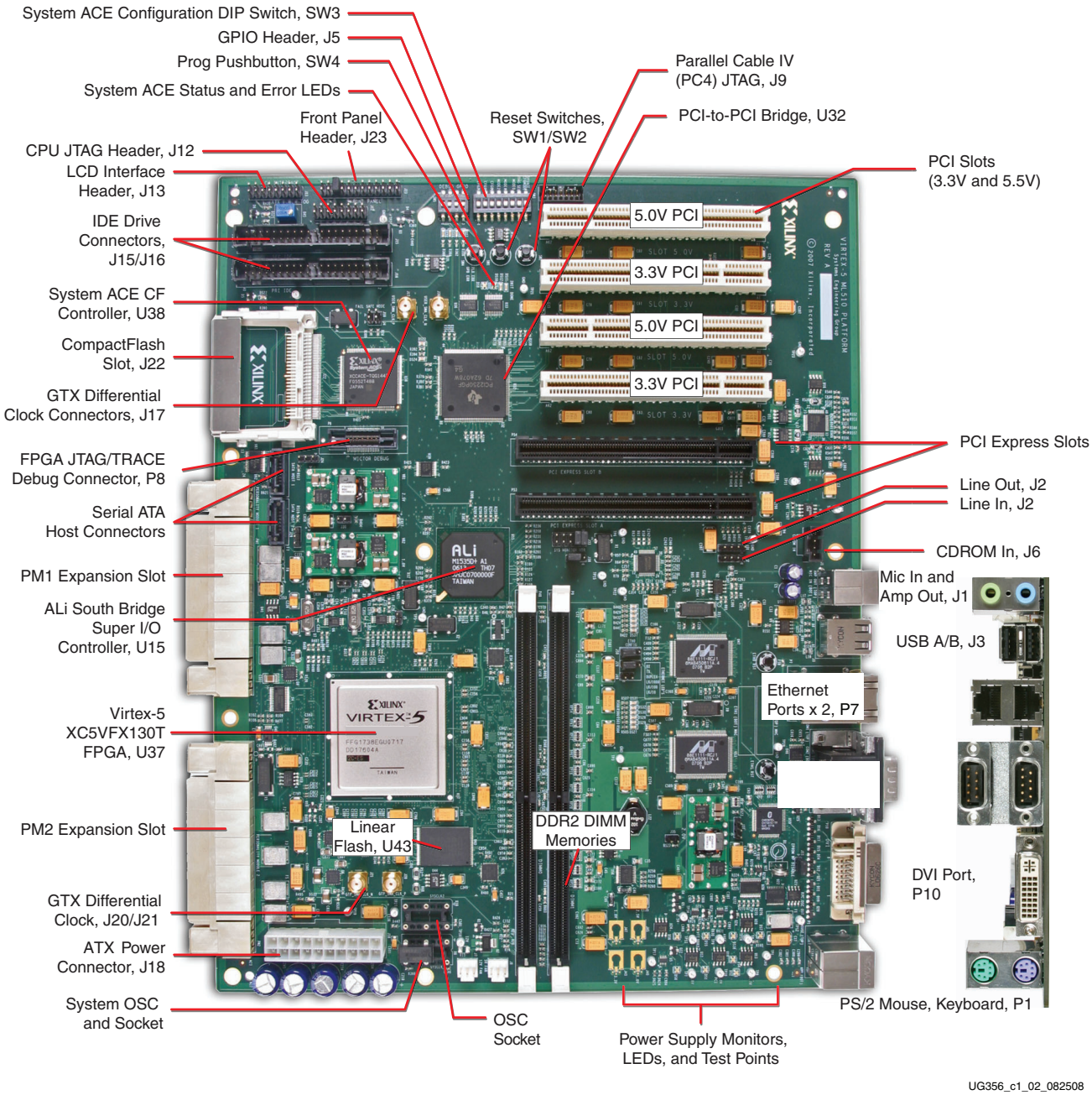

Figure 1-2: **ML510 Board and Front Panel Detail**

Virtex-5 FPGA

A Xilinx Virtex-5 FPGA, XC5VFX130T-2FFG1738C, is installed on the Embedded Development Platform (the board).

Configuration

ML510 platforms support configuration in JTAG mode only. Configuration can be accomplished by using a Xilinx download cable (such as Parallel Cable IV or Platform Cable USB) or by using the onboard System ACE CompactFlash solution. See the *System ACE Configuration Solution Data Sheet*. [Ref 12]

I/O Voltage Rails

The FPGA requires different banking voltages that are set based on the I/O voltage interface requirements of each device directly connected to the FPGA. The Virtex-5 FPGA I/O can be configured to use different I/O standards such as SSTL18 as required on the DDR2 DIMM interface. See the *Virtex-5 Data Sheet* [Ref 2] for more information regarding I/O standards.

The voltage applied to the FPGA I/O banks used by the ML510 board is summarized in Table 1-1. Some banks can support the DCI feature in Virtex-5 FPGAs.

Table 1-1: **I/O Voltage Rail of FPGA Banks**

FPGA Bank	I/O Voltage Rail	DCI-Capable	Description
1	3.3V	No	Flash
2	3.3V	No	Flash, System ACE controller, and DVI
3	2.5V	No	PCI Express controls and clocks
4	3.3V	No	Flash and DVI
5	2.5V	Yes	PMIO
6	2.5V	Yes	Debug
7	-	-	Unused
8	-	-	Unused
11	1.8V	No	DIMM0 and DIMM1
12	1.2V	Yes	PMIO
13	1.8V	Yes	DIMM0
15	1.8V	Yes	DIMM0
17	1.8V	Yes	DIMM1
18	2.5V	Yes	PMIO
19	1.8V	Yes	DIMM0
20	3.0V	No	PCI
21	1.8V	Yes	DIMM1
23	1.8V	Yes	DIMM0
24	3.0V	No	PCI

Table 1-1: **I/O Voltage Rail of FPGA Banks *(Cont'd)***

FPGA Bank	I/O Voltage Rail	DCI-Capable	Description
25	2.5V	No	PHY0 and PMIO
26	3.3V	No	System ACE controller and DVI

Clock Generation

ML510 boards are equipped with two crystal oscillator sockets (X6 and X10) each wired for standard LVTTL-type oscillators. Both sockets accept half- and full-size oscillators. See the reference design documentation on the ML510 website for examples of how to set up the clocks on ML510 boards.

X6 is populated with a 100 MHz oscillator that provides the system clock. This system clock is typically used to generate multiple other clocks with varying frequencies and phases within the FPGA fabric by using the Virtex-5 DCMs. The FPGA also generates and drives clocks required by the DDR2 DIMM memory and PCI bus interfaces. If required, a second user clock can be brought into the FPGA by installing a second oscillator in the X10 socket.

High-precision clock signals can be supplied to the FPGA using differential clock signals brought in through 50Ω SMA connectors. A single-ended clock can be connected to USER_SMA_CLK_P. Two additional single-ended clocks can be supplied through the XPM connectors. Furthermore, ML510 boards are equipped with several high-precision clocks for driving the high-speed RocketIO transceivers. These clocks can also be used to drive the global clock nets of the FPGA. See the *Virtex-5 Data Sheet* [Ref 2] for details.

Figure 1-3 is an example of the clock distribution for the ML510 board.

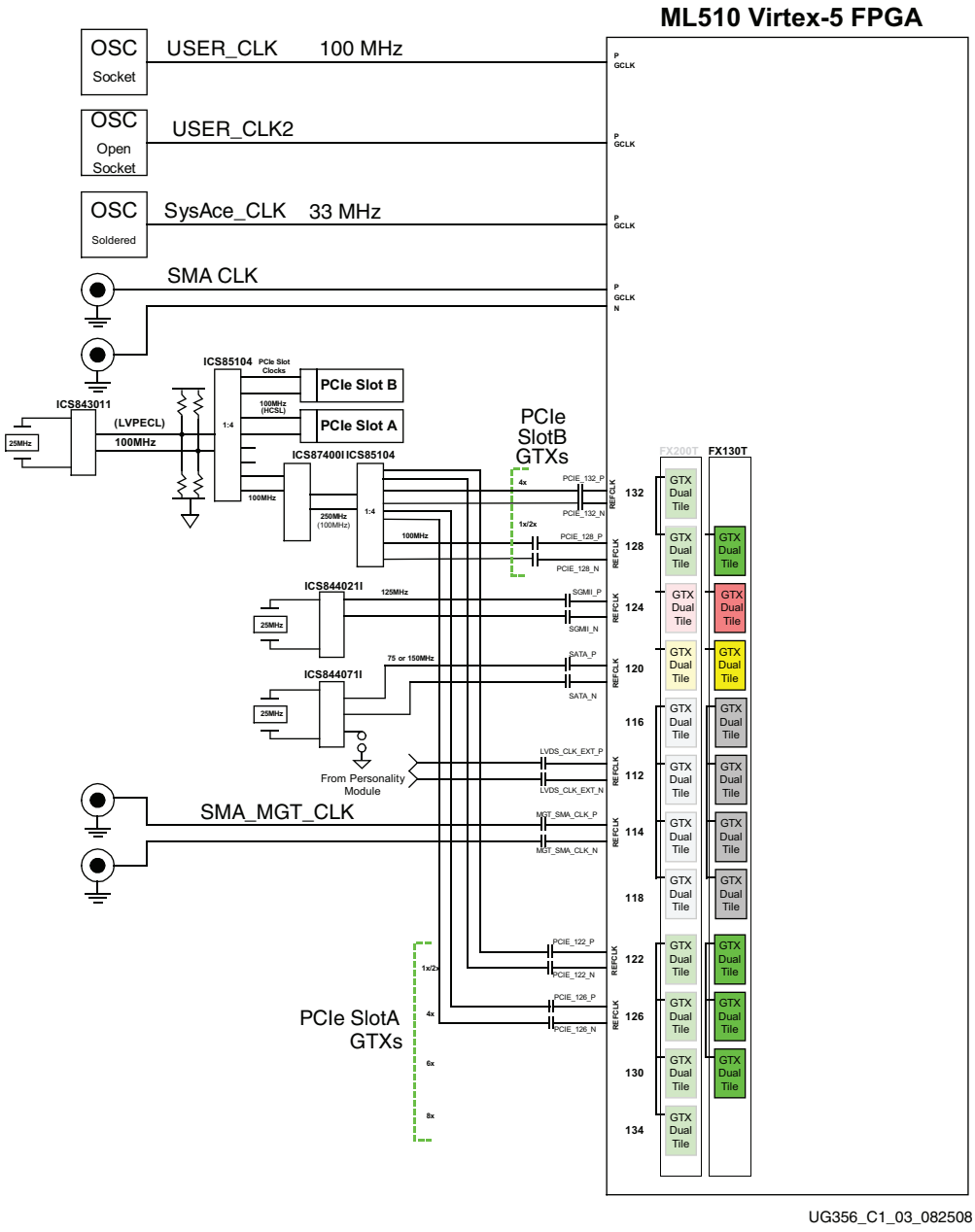

Figure 1-3: **ML510 Clock Distribution**

Table 1-2 shows the ML510 clock connections.

Table 1-2: **Clock Connections**

Schematic Net Name	Clock Source	FPGA Pin (U37)	Description
USER_CLKSYS	X6	L29	100 MHz socketed user clock oscillator (2.5V).
USER_CLK2	X10	K29	Socket for user-supplied clock oscillator (3.3V)(1).
USER_SMA_CLK_N	J36	L30	100Ω differential SMA connections that can be used as a differential pair clock.
USER_SMA_CLK_P	J17	K30	100Ω differential SMA connections that can be used as a differential pair clock. J17 can be used single ended at 50Ω
PM_CLK_TOP	PM1.F9	M27	Personality module clock (top) (2.5V)(1).
PM_CLK_BOT	PM2.F10	L14	Personality module clock (bottom) (2.5V)(1).
LVDS_CLKEXT_P_C	PM1.F12	V4	LVDS pair (2.5V)(1). Frequency is user-defined.
LVDS_CLKEXT_N_C	PM1.F11	V3	LVDS pair (2.5V)(1). Frequency is user-defined.
SGMIICLK_QO_P	X7	C4	125 MHz SMA
SGMIICLK_QO_N		C3	125 MHz SMA
GTP_SMA_CLK_P	J20	AD4	RocketIO GTX REFCLK_114 (P)
GTP_SMA_CLK_N	J21	AD3	RocketIO GTX REFCLK_114 (N)
SATACLK_QO_P	(Selectable)	F4	75 or 150 MHz jumper selectable.
SATACLK_QO_N	(Selectable)	F3	75 or 150 MHz jumper selectable.

Notes:

1. See "High-Speed I/O," page 66.

DDR2 Memory

ML510 platforms have two DDR2 SDRAM Dual Inline Memory Modules (DIMMs) that enable users to build independent systems.

MIG Compliance

The ML510 DDR2 memory interfaces are MIG-compliant, having passed simulation using standard Virtex-5 IBIS models. DDR2 routing guidelines are achieved. The DDR2 Clocks are fanned out using zero-delay buffers.

The board's DDR2 memory interfaces are designed to the requirements defined by the *Xilinx Memory Interface Generator (MIG) User Guide* [Ref 21] using the MIG tool [Ref 23]. The MIG documentation requires that designers follow the MIG pinout and layout guidelines. The MIG tool generates and ensures that the proper FPGA I/O pin selections are made in support of the board's DDR2 interfaces. The initial pin selection for the board was modified and then re-verified to meet the MIG pinout requirements. To ensure a robust interface, the ML510 DDR2 layout incorporates matched trace lengths for data signals to the corresponding data strobe signal as defined in the MIG user guide. See Appendix A, "References" for links to additional information about MIG and Virtex-5 FPGAs in general.

Dual DDR2 SDRAM DIMMs

The DDR2 DIMMs are standard 240-pin DIMM sockets, supporting standard computer DDR2 memory.

ML510 boards are shipped with dual single-rank registered 512 MB PC2-5300 DDR2-667 DIMMs. The DDR2 DIMM is commercially available from Wintec Industries. The DDR2 DIMM uses nine 32M x 8 DDR2 SDRAM devices with 14-row address lines, 10-column address lines, and two bank address lines. Read and write access is programmable in burst lengths of 4 or 8. The memory module inputs and outputs are compatible with SSTL18 signaling. Serial Presence Detect (SPD) using an IIC interface to the DDR DIMM is also supported. See the "IIC/SMBus Interface" section for more details on accessing the DIMM module's SPD EEPROM.

The DDR2 DIMM memory interface includes a 72-bit wide datapath to the DDR2 DIMM, which includes 8 bits for ECC.

DDR2 Memory Expansion

The DDR2 interface is very flexible and can accommodate different DDR2 memory requirements, such as increased memory size. Please review the *Embedded Processor Block in Virtex-5 FPGAs Reference Guide* [Ref 4] when migrating to a different DDR2 DIMM.

DDR2 Clock Signal

The DDR2 clock signal is broadcast from the FPGA as a single differential pair that drives a clock fan-out chip, which then drives the DDR2 DIMM. The delay on the clock trace is designed to match the delay of the other DDR2 control and data signals. The DDR2 clock is also fed back to the FPGA to allow for clock deskew using Virtex-5 DCMs. The board is designed so that the DDR2 clock signal reaches the FPGA clock feedback pin at the same time as it arrives at the DDR2 DIMM. This clock fanout circuit is duplicated for both DIMM interfaces.

DDR2 Signaling

Only DDR2 SDRAM control signals are terminated through 47Ω resistors to a 0.9V VTT reference voltage. The board is designed for matched length traces across all DDR2 control and data signals, except clocks. The FPGA DDR2 interface supports SSTL18 signaling. All DDR2 signals are controlled impedance and are SSTL18 at the DIMM via ODT and at the FPGA via DCI.

Table 1-3, page 18 describes all the signals associated with DDR2 DIMM component memories. Note that the DDR2_DQ signal names do not correlate because the FPGA uses IBM notation, big endian, while the DDR2 DIMM uses Intel notation, little endian.

Table 1-3: **Connections from FPGA to DDR2 DIMM0 Interface (P48)**

Schematic Net Name	FPGA Pin (U37)	DDR2 DIMM0 (P48)
DIMM0_DDR2_WE_B	Y40	73
DIMM0_DDR2_S1_B	M37	77
DIMM0_DDR2_S0_B	U32	193
DIMM0_DDR2_RAS_B	W40	192
DIMM0_DDR2_CAS_B	AA37	74
DIMM0_DDR2_PLL_CLKIN_P	AA40	138
DIMM0_DDR2_PLL_CLKIN_N	AA39	137
DIMM0_DDR2_ODT1	K35	76
DIMM0_DDR2_ODT0	U31	195
DIMM0_DDR2_DQS8_P	H40	46
DIMM0_DDR2_DQS8_N	J40	45
DIMM0_DDR2_DQS7_P	K38	114
DIMM0_DDR2_DQS7_N	J38	113
DIMM0_DDR2_DQS6_P	M38	105
DIMM0_DDR2_DQS6_N	L39	104
DIMM0_DDR2_DQS5_P	U36	93
DIMM0_DDR2_DQS5_N	V36	92
DIMM0_DDR2_DQS4_P	R35	84
DIMM0_DDR2_DQS4_N	T36	83
DIMM0_DDR2_DQS3_P	T34	37
DIMM0_DDR2_DQS3_N	U33	36
DIMM0_DDR2_DQS2_P	E32	28
DIMM0_DDR2_DQS2_N	E33	27
DIMM0_DDR2_DQS1_P	F31	16
DIMM0_DDR2_DQS1_N	F32	15
DIMM0_DDR2_DQS0_P	E34	7
DIMM0_DDR2_DQS0_N	F34	6
DIMM0_DDR2_DQM8	G39	164
DIMM0_DDR2_DQM7	W36	232
DIMM0_DDR2_DQM6	T39	223
DIMM0_DDR2_DQM5	V35	211

Table 1-3: **Connections from FPGA to DDR2 DIMM0 Interface (P48) *(Cont'd)***

Schematic Net Name	FPGA Pin (U37)	DDR2 DIMM0 (P48)
DIMM0_DDR2_DQM4	M36	202
DIMM0_DDR2_DQM3	F36	155
DIMM0_DDR2_DQM2	P33	146
DIMM0_DDR2_DQM1	L32	134
DIMM0_DDR2_DQM0	F35	125
DIMM0_DDR2_DQ63	W35	236
DIMM0_DDR2_DQ62	W37	235
DIMM0_DDR2_DQ61	T37	230
DIMM0_DDR2_DQ60	P37	229
DIMM0_DDR2_DQ59	Y34	117
DIMM0_DDR2_DQ58	AA34	116
DIMM0_DDR2_DQ57	AA36	111
DIMM0_DDR2_DQ56	AA35	110
DIMM0_DDR2_DQ55	V39	227
DIMM0_DDR2_DQ54	R37	226
DIMM0_DDR2_DQ53	R39	218
DIMM0_DDR2_DQ52	N38	217
DIMM0_DDR2_DQ51	W38	107
DIMM0_DDR2_DQ50	Y35	108
DIMM0_DDR2_DQ49	P38	99
DIMM0_DDR2_DQ48	U38	98
DIMM0_DDR2_DQ47	W33	215
DIMM0_DDR2_DQ46	Y33	214
DIMM0_DDR2_DQ45	T35	209
DIMM0_DDR2_DQ44	R34	208
DIMM0_DDR2_DQ43	AA32	96
DIMM0_DDR2_DQ42	Y32	95
DIMM0_DDR2_DQ41	W32	90
DIMM0_DDR2_DQ40	V33	89
DIMM0_DDR2_DQ39	P35	206
DIMM0_DDR2_DQ38	N36	205
DIMM0_DDR2_DQ37	L36	200
DIMM0_DDR2_DQ36	J35	199

Table 1-3: **Connections from FPGA to DDR2 DIMM0 Interface (P48) *(Cont'd)***

Schematic Net Name	FPGA Pin (U37)	DDR2 DIMM0 (P48)
DIMM0_DDR2_DQ35	U34	87
DIMM0_DDR2_DQ34	V34	86
DIMM0_DDR2_DQ33	P36	81
DIMM0_DDR2_DQ32	N35	80
DIMM0_DDR2_DQ31	J37	159
DIMM0_DDR2_DQ30	H35	158
DIMM0_DDR2_DQ29	E38	153
DIMM0_DDR2_DQ28	D37	152
DIMM0_DDR2_DQ27	K37	40
DIMM0_DDR2_DQ26	J36	39
DIMM0_DDR2_DQ25	G36	34
DIMM0_DDR2_DQ24	F37	33
DIMM0_DDR2_DQ23	T31	150
DIMM0_DDR2_DQ22	R32	149
DIMM0_DDR2_DQ21	P31	144
DIMM0_DDR2_DQ20	N34	143
DIMM0_DDR2_DQ19	T32	31
DIMM0_DDR2_DQ18	R33	30
DIMM0_DDR2_DQ17	P32	25
DIMM0_DDR2_DQ16	N33	24
DIMM0_DDR2_DQ15	N31	141
DIMM0_DDR2_DQ14	M32	140
DIMM0_DDR2_DQ13	K33	132
DIMM0_DDR2_DQ12	K32	131
DIMM0_DDR2_DQ11	M34	22
DIMM0_DDR2_DQ10	M33	21
DIMM0_DDR2_DQ9	L31	13
DIMM0_DDR2_DQ8	J33	12
DIMM0_DDR2_DQ7	H34	129
DIMM0_DDR2_DQ6	H31	128
DIMM0_DDR2_DQ5	G33	123
DIMM0_DDR2_DQ4	G32	122
DIMM0_DDR2_DQ3	H33	10

Table 1-3: **Connections from FPGA to DDR2 DIMM0 Interface (P48) *(Cont'd)***

Schematic Net Name	FPGA Pin (U37)	DDR2 DIMM0 (P48)
DIMM0_DDR2_DQ2	J31	9
DIMM0_DDR2_DQ1	G31	4
DIMM0_DDR2_DQ0	E35	3
DIMM0_DDR2_CKE1	L37	171
DIMM0_DDR2_CKE0	M31	52
DIMM0_DDR2_CB7	H39	168
DIMM0_DDR2_CB6	G38	167
DIMM0_DDR2_CB5	E39	162
DIMM0_DDR2_CB4	E40	161
DIMM0_DDR2_CB3	H38	49
DIMM0_DDR2_CB2	K40	48
DIMM0_DDR2_CB1	F39	43
DIMM0_DDR2_CB0	F40	42
DIMM0_DDR2_CAS_B	AA37	74
DIMM0_DDR2_BA2	K39	54
DIMM0_DDR2_BA1	M39	190
DIMM0_DDR2_BA0	N39	71
DIMM0_DDR2_A13	Y37	196
DIMM0_DDR2_A12	N41	176
DIMM0_DDR2_A11	N40	57
DIMM0_DDR2_A10	AA41	70
DIMM0_DDR2_A9	L40	177
DIMM0_DDR2_A8	P42	179
DIMM0_DDR2_A7	R42	58
DIMM0_DDR2_A6	P41	180
DIMM0_DDR2_A5	T40	60
DIMM0_DDR2_A4	U42	61
DIMM0_DDR2_A3	T42	182
DIMM0_DDR2_A2	U41	63
DIMM0_DDR2_A1	P40	183
DIMM0_DDR2_A0	AA42	188

Table 1-4: **Connections from FPGA to DDR2 DIMM1 Interface (P9)**

UCF Signal Name	FPGA Pin (U37)	DDR2 DIMM1 (P9)
DIMM1_DDR2_WE_B	V40	73
DIMM1_DDR2_S1_B	AE37	77
DIMM1_DDR2_S0_B	AU42	193
DIMM1_DDR2_RAS_B	V41	192
DIMM1_DDR2_CAS_B	Y42	74
DIMM1_DDR2_PLL_CLKIN_P	Y39	138
DIMM1_DDR2_PLL_CLKIN_N	Y38	137
DIMM1_DDR2_ODT1	AF37	76
DIMM1_DDR2_ODT0	AV41	195
DIMM1_DDR2_DQS8_P	AH34	46
DIMM1_DDR2_DQS8_N	AG34	45
DIMM1_DDR2_DQS7_P	AF35	114
DIMM1_DDR2_DQS7_N	AF36	113
DIMM1_DDR2_DQS6_P	AE35	105
DIMM1_DDR2_DQS6_N	AF34	104
DIMM1_DDR2_DQS5_P	AT39	93
DIMM1_DDR2_DQS5_N	AR39	92
DIMM1_DDR2_DQS4_P	AV40	84
DIMM1_DDR2_DQS4_N	AU39	83
DIMM1_DDR2_DQS3_P	AR40	37
DIMM1_DDR2_DQS3_N	AT40	36
DIMM1_DDR2_DQS2_P	AC40	28
DIMM1_DDR2_DQS2_N	AC39	27
DIMM1_DDR2_DQS1_P	AE40	16
DIMM1_DDR2_DQS1_N	AD40	15
DIMM1_DDR2_DQS0_P	AB39	7
DIMM1_DDR2_DQS0_N	AC38	6
DIMM1_DDR2_DQM8	AD33	164
DIMM1_DDR2_DQM7	AV39	232
DIMM1_DDR2_DQM6	AK35	223
DIMM1_DDR2_DQM5	AN40	211
DIMM1_DDR2_DQM4	AG37	202

Table 1-4: **Connections from FPGA to DDR2 DIMM1 Interface (P9) *(Cont'd)***

UCF Signal Name	FPGA Pin (U37)	DDR2 DIMM1 (P9)
DIMM1_DDR2_DQM3	AC36	155
DIMM1_DDR2_DQM2	AP41	146
DIMM1_DDR2_DQM1	AH41	134
DIMM1_DDR2_DQM0	AC41	125
DIMM1_DDR2_DQ63	AN34	236
DIMM1_DDR2_DQ62	AU38	235
DIMM1_DDR2_DQ61	AR37	230
DIMM1_DDR2_DQ60	AN36	229
DIMM1_DDR2_DQ59	AU37	117
DIMM1_DDR2_DQ58	AT36	116
DIMM1_DDR2_DQ57	AT37	111
DIMM1_DDR2_DQ56	AP35	110
DIMM1_DDR2_DQ55	AK34	227
DIMM1_DDR2_DQ54	AR38	226
DIMM1_DDR2_DQ53	AL36	218
DIMM1_DDR2_DQ52	AE32	217
DIMM1_DDR2_DQ51	AL34	107
DIMM1_DDR2_DQ50	AM34	108
DIMM1_DDR2_DQ49	AM36	99
DIMM1_DDR2_DQ48	AL35	98
DIMM1_DDR2_DQ47	AN39	215
DIMM1_DDR2_DQ46	AN38	214
DIMM1_DDR2_DQ45	AK38	209
DIMM1_DDR2_DQ44	AL39	208
DIMM1_DDR2_DQ43	AP38	96
DIMM1_DDR2_DQ42	AM37	95
DIMM1_DDR2_DQ41	AP40	90
DIMM1_DDR2_DQ40	AM38	89
DIMM1_DDR2_DQ39	AJ37	206
DIMM1_DDR2_DQ38	AK39	205
DIMM1_DDR2_DQ37	AG38	200
DIMM1_DDR2_DQ36	AF39	199
DIMM1_DDR2_DQ35	AM39	87

Table 1-4: **Connections from FPGA to DDR2 DIMM1 Interface (P9) *(Cont'd)***

UCF Signal Name	FPGA Pin (U37)	DDR2 DIMM1 (P9)
DIMM1_DDR2_DQ34	AL37	86
DIMM1_DDR2_DQ33	AH38	81
DIMM1_DDR2_DQ32	AJ38	80
DIMM1_DDR2_DQ31	AD37	159
DIMM1_DDR2_DQ30	AD35	158
DIMM1_DDR2_DQ29	AC35	153
DIMM1_DDR2_DQ28	AB34	152
DIMM1_DDR2_DQ27	AE38	40
DIMM1_DDR2_DQ26	AD36	39
DIMM1_DDR2_DQ25	AC34	34
DIMM1_DDR2_DQ24	AB36	33
DIMM1_DDR2_DQ23	AT41	150
DIMM1_DDR2_DQ22	AT42	149
DIMM1_DDR2_DQ21	AM41	144
DIMM1_DDR2_DQ20	AN41	143
DIMM1_DDR2_DQ19	AR42	31
DIMM1_DDR2_DQ18	AP42	30
DIMM1_DDR2_DQ17	AL42	25
DIMM1_DDR2_DQ16	AK42	24
DIMM1_DDR2_DQ15	AL41	141
DIMM1_DDR2_DQ14	AJ42	140
DIMM1_DDR2_DQ13	AH40	132
DIMM1_DDR2_DQ12	AG42	131
DIMM1_DDR2_DQ11	AJ40	22
DIMM1_DDR2_DQ10	AJ41	21
DIMM1_DDR2_DQ9	AF42	13
DIMM1_DDR2_DQ8	AE42	12
DIMM1_DDR2_DQ7	AF41	129
DIMM1_DDR2_DQ6	AF40	128
DIMM1_DDR2_DQ5	AB42	123
DIMM1_DDR2_DQ4	AB41	122
DIMM1_DDR2_DQ3	AD41	10
DIMM1_DDR2_DQ2	AD42	9

Table 1-4: **Connections from FPGA to DDR2 DIMM1 Interface (P9) *(Cont'd)***

UCF Signal Name	FPGA Pin (U37)	DDR2 DIMM1 (P9)
DIMM1_DDR2_DQ1	AB37	4
DIMM1_DDR2_DQ0	AB38	3
DIMM1_DDR2_CKE1	AE39	171
DIMM1_DDR2_CKE0	AU41	52
DIMM1_DDR2_CB7	AE33	168
DIMM1_DDR2_CB6	AE34	167
DIMM1_DDR2_CB5	AC33	162
DIMM1_DDR2_CB4	AB32	161
DIMM1_DDR2_CB3	AH36	49
DIMM1_DDR2_CB2	AG36	48
DIMM1_DDR2_CB1	AD32	43
DIMM1_DDR2_CB0	AB33	42
DIMM1_DDR2_CAS_B	Y42	74
DIMM1_DDR2_BA2	AH35	54
DIMM1_DDR2_BA1	AJ36	190
DIMM1_DDR2_BA0	AJ35	71
DIMM1_DDR2_A13	W41	196
DIMM1_DDR2_A12	F41	176
DIMM1_DDR2_A11	G41	57
DIMM1_DDR2_A10	W42	70
DIMM1_DDR2_A9	F42	177
DIMM1_DDR2_A8	G42	179
DIMM1_DDR2_A7	J42	58
DIMM1_DDR2_A6	H41	180
DIMM1_DDR2_A5	M42	60
DIMM1_DDR2_A4	L42	61
DIMM1_DDR2_A3	K42	182
DIMM1_DDR2_A2	M41	63
DIMM1_DDR2_A1	J41	183
DIMM1_DDR2_A0	R40	188