Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ML52*x* User Guide

Virtex-5 FPGA RocketIO Characterization Platform

UG225 (v2.1) August 4, 2010

XILINX®

0402527-03

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
03/02/07	1.0	Initial Xilinx release.
08/06/07	1.1	Removed *UG091, Xilinx Generic Interface (XGI) SuperClock Module User Guide* from“Package Contents.” Removed “Power Bus and Switches” diagram from Figure 1. Added Power Supply Block Diagram, Figure 3. Updated Micron part number in “18. DDR2 Memory,” page 21. Corrected DDR to DDR2 throughout. Updated ML521 connections for A11 and A12 in Table 15. Corrected CK0N and CK0P pin numbers in Table 15.
04/17/08	2.0	Added GTX transceiver and FXT device information. Updated VCCINT for ML525 in Table 2. Modified the power brick connection in Figure 3 for consistency and accuracy. Added Voltage Adjust Potentiometer column in Table 3. Added Platform Cable USB to “3. FPGA Configuration.” Corrected ML521 pins in Table 9. Updated Infineon and Micron part numbers in “18. DDR2 Memory.” Corrected numerous pins in Table 15. Corrected CTS and RXD pins in Table 18. Corrected the RS232 and DB9 reference designators in Figure 4. Corrected J113 and J135 column headings in Table 19. Renumbered XGI pins in columns E and F and corrected XGI pin F27 description in Table 20. Renumbered XGI pins in columns A and B in Table 22. Several updates to Table 23.
08/04/10	2.1	Section “Features,” page 10: Corrected the number of pairs of transceiver SMA connectors from “32 to 96” to “16 to 48.” Figure 1, page 11, corrected the number of transceivers/SMAs in FF665 from 12/48 to 8/32, and the number of clocks/SMAs in FF665 from 6/12 to 4/8. Section “19. GTP/GTX Transceiver Clock Input SMAs,” page 25, removed material from introductory paragraph describing the lack of AC coupling. Table 22, page 33, corrected ML523 pin for signal XGI_SE_30 from AH32 to AH34.

Table of Contents

About This Guide

This user guide describes the features and operation of the Virtex®-5 FPGA ML52x series of RocketIO™ characterization platforms.

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- Virtex-5 FPGA User Guide

  Chapters in this guide cover the following topics:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources

- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platforms.

- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.

- Virtex-5 FPGA Tri-Mode Ethernet Media Access Controller

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.

- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.

- XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E slice.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the Virtex-5 *FPGA Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

This document uses the following conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Support Resources" for details. Refer to "DMA Operation" in Chapter 13 for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-5 FPGA Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

ML52x User Guide

Package Contents

- ML52x RocketIO characterization platform (referred to as the ML52x platform)
- UG225, *ML52x User Guide: Virtex-5 RocketIO Characterization Platform*
- SMA-to-SMA cable assemblies:
  - Four 24-inch cable assemblies
  - Two 12-inch cable assemblies
- System ACE™ CompactFlash memory card
- SuperClock module
- Power supply module
- Power supply brick
- SMA wrench

Additional Information

For current information about the ML52x RocketIO characterization platform, visit www.xilinx.com/ml52x

The information includes:

- Current version of this user guide in PDF format
- Example design files for demonstration of Virtex-5 FPGA features and technology
- Demonstration hardware and software configuration files for the System ACE controller
- MicroBlaze™ EDK reference design files (Board Support Builder)
- Full schematics in PDF format and ViewDraw schematic format
- PC board layout in Allegro PCB format
- Gerber files for the PC board (Many free or shareware Gerber file viewers are available on the Internet for viewing and printing these files)
- Additional documentation, errata, frequently asked questions, and the latest news
- Contents of the CompactFlash card provided with the ML52x platform

Related Documents

Prior to using the ML52x platforms, users should be familiar with Xilinx resources. See "References," page 35 for direct links to Xilinx and other related documentation. See the following locations for additional documentation on Xilinx tools and solutions.

- EDK: www.xilinx.com/edk
- ISE® Design Tools: www.xilinx.com/ise
- Answer Browser: www.xilinx.com/support
- Virtex-5 FPGAs: www.xilinx.com/virtex5
- ChipScope™ Pro: www.xilinx.com/chipscope

Introduction

The ML52x RocketIO transceiver characterization platform allows designers to investigate and experiment with the features of the RocketIO transceivers (the *transceivers*). This document describes the features and operation of the boards.

> ***Caution!*** To protect the ML52x platform from damage caused by electrostatic discharge (ESD), follow standard ESD prevention measures when handling the board.

The platforms and their corresponding packages are shown in Table 1.

Table 1: **Platforms and Packages**

Platform	Device		Package
	LXT	FXT	
ML521	XC5VLX50T	XC5VFX70T	FF665
ML523	XC5VLX110T	XC5VFX100T	FF1136
ML525	XC5VLX330T	XC5VFX200T	FF1738

Features

- Virtex-5 FPGA (referred to as the device under test, or DUT, in this user guide)
- Onboard power supplies for all necessary voltages
- Power supply jacks for optional use of external power supplies
- JTAG configuration port for use with Parallel Cable III and Parallel Cable IV cables
- System ACE controller with 8-bit MPU port support
- Power supply module supporting all transceiver power requirements
- Two 2.5V / 3.3V global clock oscillator sockets
- Two single-ended global clock inputs with SMA connectors
- Two pairs of differential global clock inputs with SMA connectors
- SuperClock module supporting multiple frequencies
- Xilinx Generic Interface (XGI)
- 16 to 48 pairs of SMA connectors for the RocketIO transceivers
- 4 to 12 pairs of SMA connectors for RocketIO transceiver clock inputs
- Power indicator LEDs

- General purpose DIP switches, LEDs, and pushbutton switches
- 32 MB - 128 MB of DDR2 Memory

Figure 1 shows the block diagram of the board.

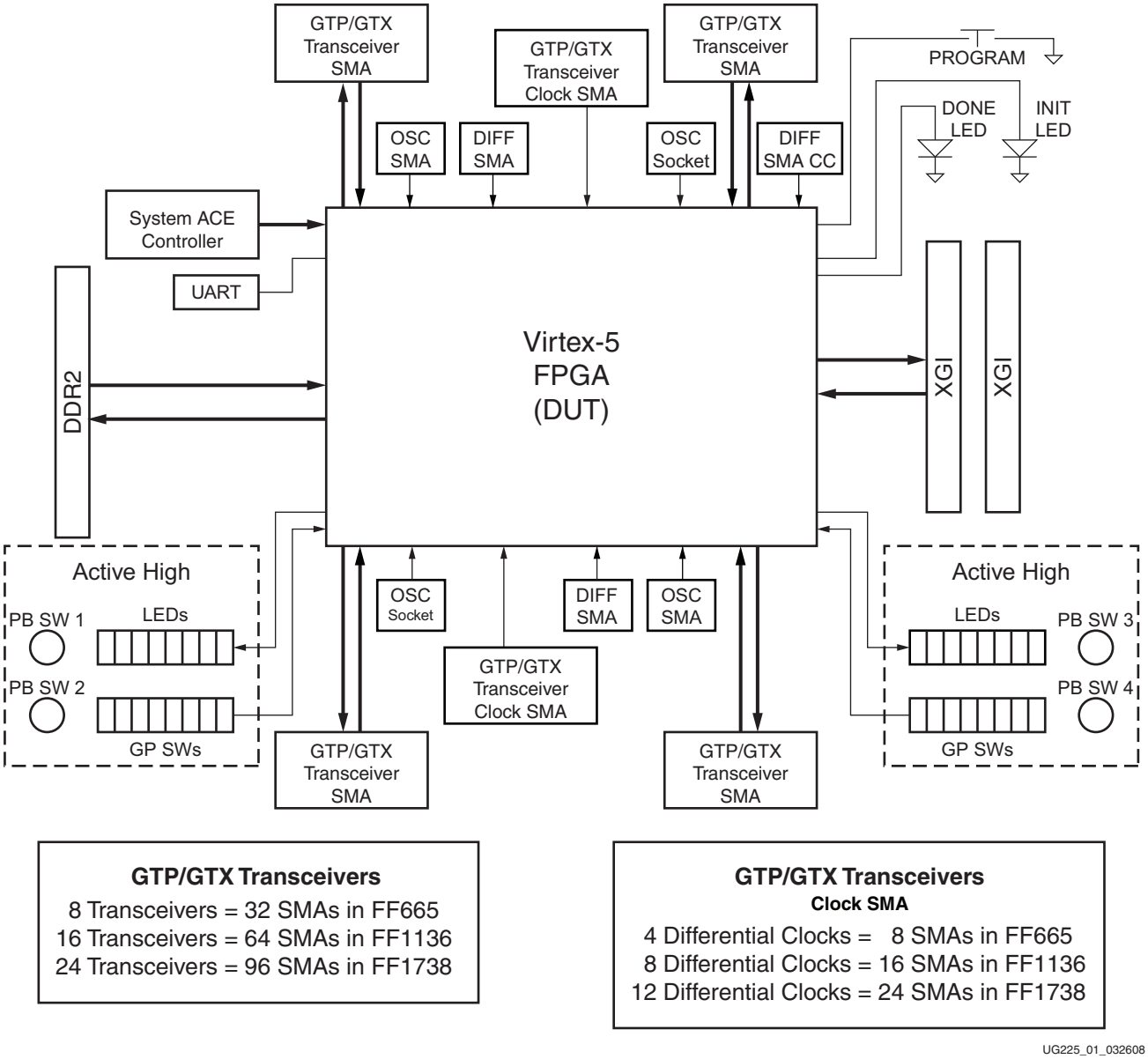
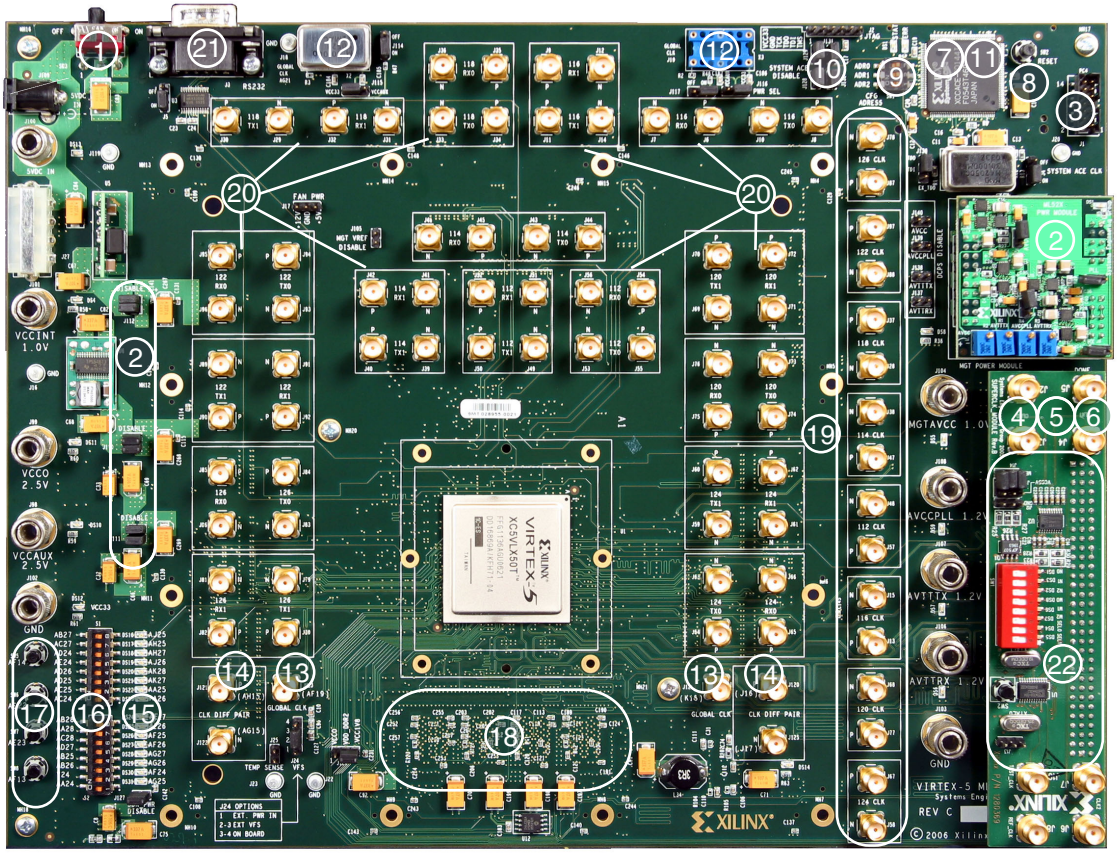


Figure 1: **Virtex-5 FPGA ML52x Platform Block Diagram**

Detailed Description

The ML52*x* platform shown in Figure 2 represents the ML52*x* series described in this user guide. Each feature is detailed in the numbered sections that follow.

Note: The image might not reflect the current revision of the board.



UG225_02_100206

Figure 2: **Detailed Description of Virtex-5 FPGA ML52x Platform Components**

1. Power Switch

The board has onboard power supplies controlled by the power switch. When the V5 LED is lit, this indicates the board is powered.

On Position

In the ON position, the power switch enables delivery of all power on the board by way of voltage regulators situated close to the left side of the board and the MGT power module situated close to the right side of the board. These regulators feed off the 5V external power brick or the 5V power supply jack.

The 5V power brick is capable of providing a maximum of 6.5A. For designs that require greater than 6.5A, an ATX power supply can be connected to the J27 hard drive power connector.

Note: 5V must always be supplied to the board to enable the 3.3V regulator for the System ACE controller chip. It is always recommended to check the power supply voltage values before testing your design or taking measurements.

Off Position

In the OFF position, the power switch disables all modes of power on the board.

2. Power Regulation

Main Board Regulation

The ML52x platform has onboard regulation for the DUT main power supplies listed in Table 2. These regulators also have a corresponding input voltage jack to supply each voltage independently from the bench-top power supply (see Figure 3, page 14). This is done by removing the power supply enable jumpers for the headers that correspond to each supply voltage listed in Table 2.

Note:

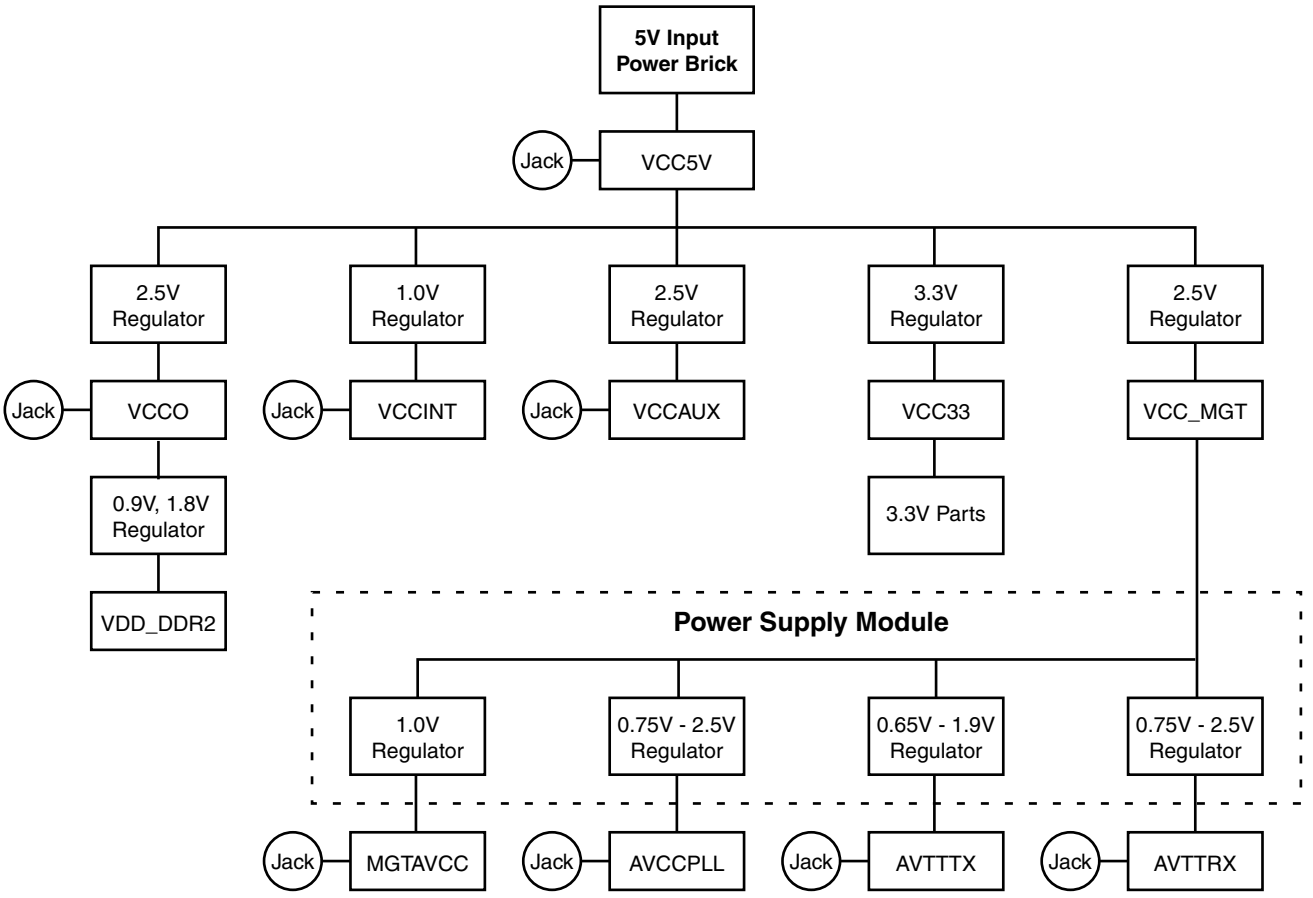
- If your design exceeds the maximum current rating for any of the onboard regulators for any given rail, that rail must be supplied by the external power jack.
- The power enable jumper must be removed before supplying an external supply on its corresponding supply jack.

Table 2: **Onboard Regulation: Voltage, Current, Jacks, and Jumpers**

Power Supply Name	Max Current Rating	Typical Voltage	Jack/ Connector	Enable Jumper	Description
5V	N/A	5V	J27 J109 J100	N/A	Main input voltage for the ML52x boards supplied through the jack, barrel connector or Molex connector.
VCC33	3.0A	3.3V	N/A	N/A	Supplies 3.3V of the System ACE chip and other onboard circuits.
VCCINT	7.0A / 30.0A	1.0V	J101	J112	Core voltage for the FPGA (DUT). Max current rating: • ML521 and ML523 boards rated at 7A • ML525 board rated at 30A

Table 2: **Onboard Regulation: Voltage, Current, Jacks, and Jumpers *(Cont'd)***

Power Supply Name	Max Current Rating	Typical Voltage	Jack/ Connector	Enable Jumper	Description
VCCO	6.0A	2.5V	J99	J19/J110	I/O voltage for the FPGA (DUT).
VCCAUX	3.0A	2.5V	J98	J111	Auxiliary voltage for the FPGA (DUT).
GND	N/A	N/A	J102/J103	N/A	Ground connection for all circuits.



NOTE:
The GTP/GTX transceiver power supply names might have the prefix *MGT* in other Xilinx documentation. Names with and without the MGT prefix are synonymous to each other.

UG225_03_100207

Figure 3: **Power Supply Block Diagram**

Power Supply Module

The power supply module supplies all voltages shown in Table 3, page 15 to the DUT RocketIO transceivers. This module plugs in on the right side of the board on header J134, J133, and J26 of the ML52x platform.

The onboard regulators also have corresponding input voltage jacks to supply each voltage independently from a bench-top power supply. This is done by installing the power supply disable jumpers for the headers that correspond to each supply voltage

listed in Table 3. The power supply disable jumper must be installed before supplying an external supply on its corresponding supply jack.

Table 3: **Power Supply Module Jumpers**

GTP/GTX Power Supply Name(1)	Max Current Rating	Typical Voltage		Voltage Adj. Pot.	Jack	Disable Jumper	Description
		LXT	FXT				
MGTAVCC	3.0A	1.0V	1.0V	R2	J104	J5	Powers all transceiver analog circuits.
AVCCPLL	1.5A	1.2V	1.0V	R4	J108	J7	Powers all transceiver PLL and clock network.
AVTTTX	1.5A	1.2V	1.2V	R1	J107	J4	Termination voltage for transceiver transmitter.
AVTTRX	1.5A	1.2V	1.2V	R3	J106	J6	Termination voltage for transceiver receiver.

Notes:

1. The GTP/GTX transceiver power supply names might have the prefix *MGT* in other Xilinx documentation. Names with and without the MGT prefix are synonymous to each other.

3. FPGA Configuration

The FPGA can only be configured in JTAG mode using one of the following options:

- Parallel Cable III cable
- Parallel Cable IV cable
- Platform Cable USB
- System ACE controller

For detailed information, see *System ACE CompactFlash Solution* [Ref 1].

Using the configuration address DIP switches, one of eight bitstreams stored in the CompactFlash memory card can be accessed through the on-board System ACE controller.

Note: The System ACE controller is bypassed when the flying wire leads or the Parallel Cable IV cable is used, thus causing no disruption in the JTAG chain.

4. Program Switch (Active-Low)

The active-Low program switch, when pressed, grounds the program pin on of the FPGA.

5. DONE LED

The DONE LED indicates the status of the DONE pin of the FPGA. The LED lights when DONE is high, indicating the FPGA configured successfully.

6. INIT LED

The INIT LED lights during initialization.

7. System ACE Controller

An onboard System ACE controller allows the user to store multiple configuration files on a CompactFlash card. These configuration files can be used to program the FPGA.

8. Reset Switch (Active-Low)

The active-Low reset switch resets the System ACE controller.

9. Configuration Address DIP Switch

This switch is used to select one of eight addresses in the CompactFlash memory card, from which a configuration bitstream can be read. The open (O) position indicates a logic 0 and the closed (C) position indicates a logic 1 as shown in Table 4.

Table 4: **DIP Switch Configuration**

Address	2	1	0
0	O	O	O
1	O	O	C
2	O	C	O
3	O	C	C
4	C	O	O
5	C	O	C
6	C	C	O
7	C	C	C

10. JTAG Isolation Jumpers

The 2-pin headers shown in Table 5 provide the ability for the user to isolate the DUT JTAG interface from the System ACE controller. This is done by removing the shorting jumpers. The user may also drive the DUT JTAG interface directly from these headers by attaching the flying wire JTAG cable to pin one of each header.

Table 5: **JTAG Isolation Jumpers**

Ref Des	Pin Name
J128	TDI
J129	TDO
J131	TMS
J132	TCK

11. System ACE MPU Port

The 8-bit MPU port of the System ACE controller implemented on the ML52x series boards and the port connection to the DUT are shown in Table 6. For more information on the System ACE MPU port see *System ACE CompactFlash Solution* [Ref 1].

Table 6: **System ACE Port Connections**

Pin Name	ML521	ML523	ML525
MPA00	K7	E8	N8
MPA01	K6	E9	N9
MPA02	U5	K9	G8
MPA03	R5	C13	U9
MPA04	N6	E11	V11
MPA05	P6	F11	U11
MPA06	N7	L9	K9
MPD00	U6	K8	G7
MPD01	T5	B13	U8
MPD02	H6	G13	L9
MPD03	G6	F13	M9
MPD04	L8	G12	T11
MPD05	M7	G11	T10
MPD06	T7	L8	J7
MPD07	R6	M8	J8
MPIRQ	P8	E13	L7
MPBRDY	R7	N9	M8
MPCE#	M6	M10	K8
MPOE#	N8	E12	K7
MPWE#	R8	N10	M7
CLK	G20	G23	N30

12. Oscillator Sockets

The ML52x platform has two oscillator sockets, each wired for standard LVCMOS-type oscillators. These connect to the DUT clock pins as shown in Table 7. The oscillator sockets accept both half- and full-sized oscillators and are powered by 3.3V or the VCCAUX 2.5V power supply.

Table 7: **Oscillator Sockets Connections**

Ref Des	Enable/Disable Jumper	Power Select Jumper	Pin Name	ML521	ML523	ML525
X2	J114	J115	CLK_IN_B	AB19	AG21	AP27
X3	J117	J116	CLK_IN_A	D18(1)	J19(1)	K29

Notes:

1. For ML521 and ML523, the X3 clock input is not placed on the master clock IOB site. The environment variable XIL_PLACE_ALLOW_LOCAL_BUFG_ROUTING must be set to demote this condition to a warning and allow the design to continue.

13. Single-Ended SMA Clock Inputs

The ML52x platform has two single-ended clock input SMA connections that allow connection to an external function generator. These connect to the DUT clock pins as shown in Table 8.

Table 8: **SMA Clock Pin Connections**

Ref Des	Pin Name	ML521	ML523	ML525
J123	CLK_B	AB17(1)	AF19(1)	AM27
J124	CLK_A	E17	K18	M27

Notes:

1. For ML521 and ML523, the J123 clock input is not placed on the master clock IOB site. The environment variable XIL_PLACE_ALLOW_LOCAL_BUFG_ROUTING must be set to demote this condition to a warning and allow the design to continue.

14. Differential SMA Global Clock Inputs

The ML52x platform has two pairs of differential SMA transceivers clock inputs that allow connection to an external function generator. These connect to the DUT clock pins as shown in Table 9.

Table 9: **Differential SMA clock connections**

Ref Des	Pin Name	ML521	ML523	ML525
J120	CLK_DIFF_A_P	E13	J16	L17
J125	CLK_DIFF_A_N	E12	J17	M17
J121	CLK_DIFF_B_P	AC12	AH15	AM16
J122	CLK_DIFF_B_N	AC13	AG15	AM17

15. User LEDs (Active-High)

There are 16 active-High LEDs, as shown inTable 10 and Table 11 that are connected to user I/O pins on the DUT. These LEDs can be used to indicate status or any other purpose the user sees fit.

Table 10: **User LEDs Top Column**

Ref Des	LED	ML521	ML523	ML525
DS16	LED8	AE6	AJ25	AP37
DS17	LED7	AF5	AH25	AP36
DS18	LED6	AE8	AH27	AH35
DS19	LED5	AE7	AJ26	AG36
DS20	LED4	AB6	AK28	AH34
DS21	LED3	AB7	AK27	AG34
DS22	LED2	AF12	AA25	AB33
DS23	LED1	AE12	AA26	AB32

Table 11: **User LEDs Bottom Column**

Ref Des	LED	ML521	ML523	ML525
DS24	LED16	AC8	AE27	AH36
DS25	LED15	AD8	AE26	AJ36
DS26	LED14	AD6	AF25	AN34
DS27	LED13	AC7	AF26	AM34
DS28	LED12	AF4	AG27	AM36
DS29	LED11	AF3	AG26	AN35
DS30	LED10	AE5	AF24	AP35
DS31	LED9	AD4	AG25	AN36

16. User DIP Switches (Active-High)

There are 16 active-High DIP switches, as shown in Table 12 and Table 13, that are connected to user I/O pins on the DUT. These pins can be used to set control pins or any other purpose the user sees fit.

Table 12: **User DIP Switches Top Column**

Ref Des	Net Name	ML521	ML523	ML525
S1	SW8	W9	AB27	AC33
	SW7	W8	AC27	AD32
	SW6	AE11	AD24	AL34
	SW5	AD11	AE24	AK34
	SW4	V8	AD26	AL36
	SW3	V9	AD25	AL35
	SW2	AD9	AC25	AJ35
	SW1	AC9	AC24	AK35

Table 13: **User DIP Switches Bottom Column**

Ref Des	Net Name	ML521	ML523	ML525
S2	SW16	AA7	AB28	AU38
	SW15	AA8	AA28	AU37
	SW14	AF9	AC28	AV39
	SW13	AF10	AD27	AV38
	SW12	Y7	AB25	AE33
	SW11	Y8	AB26	AE34
	SW10	AD10	Y24	AD33
	SW9	AE10	AA24	AE32

17. User Pushbutton Switches (Active-High)

There are four active-High pushbutton switches, as shown in Table 14, that are connected to user I/O pins on the DUT. These switches can be used for any purpose that the user sees fit.

Table 14: **User Pushbutton Switches**

Ref Des	Switch	ML521	ML523	ML525
SW5	PB_SW4	AA12	AF14	AM13
SW6	PB_SW3	AA18	AE22	AL30
SW7	PB_SW2	Y18	AE23	AM29
SW8	PB_SW1	AA10	AF13	AK15

18. DDR2 Memory

The DDR2 memory interface on the ML52x board consists of four 256-Mbit DDR2 SDRAM chips (Micron MT47H16M16BG-3:B or Infineon HYB18T256160AF) for a total of 1-Gbit (128-MB) capacity. The pins conform to the SSTL_1.8V standard and must connect to SSTL18_II type IOBs on the FPGA. Note that the data strobe pins (DQS*) might need to be connected to IOBs with digitally-controlled impedance (SSTL18_II_DCI). The designer can also choose to use differential IOBs (DIFF_SSTL18_II and DIFF_SSTL18_II_DCI) for clock and data strobe signals. Table 15 shows the DDR2 connections to the DUT.

For more information on the DDR2 memory devices refer to the Micron *DDR2 SDRAM* data sheet [Ref 6].

Table 15: **DDR2 Connections to the DUT**

Pin Name	ML521	ML523	ML525
A0	K26	K24	R34
A1	K25	N28	D37
A2	L24	M28	E38
A3	M24	P24	W33
A4	AF18	AE31	AH39
A5	N21	E27	V36
A6	M21	E26	U36
A7	J24	M27	G37
A8	H24	N27	H36
A9	J26	L28	G36
A10	J25	L24	P35
A11	E25	K28	F36
A12	E26	K27	F37
BA0	AC26	W24	AB34
BA1	B19	L30	N39
CAS#	C18	M30	M39
CK0N	H22	H24	J36
CK0P	G22	H25	H35
CK1N	M26	P27	V34
CK1P	N26	P26	V35
CKE	B20	P29	L39
CS#	AD19	AB30	AV40
D0	C14	F29	H39
D1	C13	E29	H38

Table 15: **DDR2 Connections to the DUT *(Cont'd)***

Pin Name	ML521	ML523	ML525
D2	C22	R29	U37
D3	D23	R28	V38
D4	A22	R31	U38
D5	B22	T31	T37
D6	C23	T29	W38
D7	B24	T28	V39
D8	C24	U28	AA36
D9	D24	U27	AA35
D10	A25	R27	Y34
D11	B25	R26	AA34
D12	C26	T26	W35
D13	B26	U26	Y35
D14	D25	T25	W37
D15	D26	U25	W36
D16	B14	G30	G38
D17	A15	J29	F40
D18	A14	H29	F39
D19	C16	E31	E40
D20	B15	F31	E39
D21	B16	L29	R39
D22	A17	G31	P37
D23	B17	H30	R37
D24	G24	M26	P36
D25	F24	M25	N36
D26	E23	J27	L36
D27	F22	G26	J35
D28	F23	G25	K35
D29	J23	F26	J37
D30	K23	G28	U33
D31	K22	H28	T34
D32	AF15	AF29	AN39
D33	AE13	AH30	AM38
D34	AF13	AJ30	AN38

Table 15: **DDR2 Connections to the DUT *(Cont'd)***

Pin Name	ML521	ML523	ML525
D35	AD13	AH29	AM37
D36	AD24	W26	AB36
D37	AD25	Y26	AC35
D38	AE26	W25	AD35
D39	AE25	V25	AC36
D40	AF19	AD31	AG39
D41	AD18	AC29	AK39
D42	AE18	AD30	AJ38
D43	AD16	AD29	AH38
D44	AE16	AE29	AJ37
D45	AE15	AK31	AM39
D46	AD15	AJ31	AL39
D47	AF14	AF30	AP38
D48	N23	N25	W32
D49	N24	P25	Y33
D50	M22	T24	AA32
D51	N22	R24	Y32
D52	G26	L26	M36
D53	F25	L25	N35
D54	G25	J25	M37
D55	H26	J24	L37
D56	AF24	W27	AD37
D57	AF25	Y27	AD36
D58	AF23	V30	AE37
D59	AD23	V27	AE38
D60	AE22	V28	AE39
D61	AC23	Y31	AG38
D62	AC24	W31	AF39
D63	AB22	V29	AF37
DQM0	A23	U30	T39
DQM1	A13	F30	G39
DQM2	A19	J31	N38
DQM3	H23	F25	K37

Table 15: **DDR2 Connections to the DUT *(Cont'd)***

Pin Name	ML521	ML523	ML525
DQM4	AD14	AG30	AL37
DQM5	AE17	AF31	AK38
DQM6	M25	N24	V33
DQM7	AC22	W29	AG37
DQS0	D21	P31	H40
DQS0#	D20	P30	J40
DQS1	B21	M31	K40
DQS1#	C21	N30	K39
DQS2	C19	K31	K38
DQS2#	D19	L31	J38
DQS3	J21	G27	U34
DQS3#	K21	H27	T35
DQS4	AF22	Y28	AN40
DQS4#	AE21	Y29	AP40
DQS5	AC21	AA29	AT39
DQS5#	AD21	AA30	AR39
DQS6	L23	E28	R35
DQS6#	L22	F28	T36
DQS7	AF20	AB31	AR40
DQS7#	AE20	AA31	AT40
ODT	A20	N29	M38
RAS#	A18	J30	P38
WE#	AD20	AC30	AU39

19. GTP/GTX Transceiver Clock Input SMAs

The ML52x series platforms provide differential SMAs that allow connection to an external function generator for all GTP/GTX transceiver reference clock inputs of the DUT. These SMAs connect to the DUT reference clock pins as shown in Table 16.

Table 16: **Transceiver Reference Clock Inputs to the DUT**

REF DES	PIN NAME(1)	ML521	ML523	ML525
J48	REFCLKN_112	K3	P3	V3
J57	REFCLKP_112	K4	P4	V4
J38	REFCLKN_114	T3	Y3	AD3
J47	REFCLKP_114	T4	Y4	AD4
J15	REFCLKN_116	D3	H3	M3
J13	REFCLKP_116	D4	H4	M4
J28	REFCLKN_118	AB3	AF3	AK3
J37	REFCLKP_118	AB4	AF4	AK4
J68	REFCLKN_120		D4	F3
J77	REFCLKP_120		E4	F4
J88	REFCLKN_122		AL4	AT3
J97	REFCLKP_122		AL5	AT4
J58	REFCLKN_124		C8	C3
J67	REFCLKP_124		D8	C4
J78	REFCLKN_126		AM7	AY4
J87	REFCLKP_126		AL7	AW4
J147	REFCLKN_128			C10
J155	REFCLKP_128			D10
J167	REFCLKN_130			AY9
J175	REFCLKP_130			AW9
J179	REFCLKN_132			C16
J146	REFCLKP_132			D16
J159	REFCLKN_134			AY15
J166	REFCLKP_134			AW15

Notes:

1. The GTP/GTX transceiver clock pin names might have the prefix *MGT* in other Xilinx documentation. Names with and without the MGT prefix are synonymous to each other.