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Virtex-5 FPGA ML550 Networking Interfaces Platform

User Guide

UG202 (v1.4) April 18, 2008

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/12/06	1.0	Initial Xilinx release.
04/02/07	1.1	Revised User Guide with LXT and SXT devices. Added reference to Power Monitor header in Figure 1-1, page 13. Added note to Table 3-2, page 21. Changed fuse in Figure 3-7, page 29. Added "Power Monitor Connector" section. Revised LVDS_DATAOUT_1, Pin 47 and Pin 49, in Table A-1, page 51. Revised LVDS_DATAOUT_43 in Table A-3, page 54.
06/22/07	1.2	Updated pin numbers in Table 3-12, page 33. Added Appendix D, "ML550 Starter UCF."
10/08/07	1.3	Updated pin names/numbers in Table A-1, Table A-2, and Table A-4.
04/18/08	1.4	Added new section "ML550 System Monitor and Power Monitor Support," page 34 to Chapter 3.

Table of Contents

Preface: About This Guide

Chapter 1: Introduction

Chapter 2: Getting Started

Chapter 3: Hardware Description

Appendix D: ML550 Starter UCF

About This Guide

This user guide is a description of the Virtex®-5 FPGA ML550 Networking Interfaces Development Board. Complete and up-to-date documentation of the Virtex-5 family of FPGAs is available on the Xilinx website at http://www.xilinx.com/virtex5.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction"
- Chapter 2, "Getting Started"
- Chapter 3, "Hardware Description"
- Chapter 4, "Configuration"
- Appendix A, "LVDS"
- Appendix B, "LVDS Loopback Board"
- Appendix C, "LCD Interface"
- Appendix D, "ML550 Starter UCF"

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- Virtex-5 FPGA User Guide

  Chapters in this guide cover the following topics:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources

- SelectIO Logic Resources

- Advanced SelectIO Logic Resources

- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platforms.

- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.

- Virtex-5 FPGA Embedded Processor Block for PowerPC® 440 Designs

  This reference guide is a description of the embedded processor block available in the Virtex-5 FXT platform.

- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.

- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.

- Virtex-5 FPGA XtremeDSP Design Considerations User Guide

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at:
http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-5 Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Support Resources" for details. Refer to "Clock Generation" in Chapter 3 for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

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Chapter 1

Introduction

About the Virtex-5 FPGA Source-Synchronous Interfaces Tool Kit

The Virtex®-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit provides a complete development platform for designing and verifying applications based on the Virtex-5 LXT FPGA family. This kit allows designers to implement high-speed applications with extreme flexibility using IP cores and customized modules. The Virtex-5 LXT FPGA, with its column-based architecture, makes it possible to develop highly flexible networking applications.

The Virtex-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit includes the following:

- Virtex-5 FPGA ML550 Networking Interfaces Development Board (XC5VLX50T-FFG1136 FPGA)
- 5V/6.5 A DC power supply
- Country-specific power supply line cord
- USB B-to-A cable
- Xilinx® LVDS Loopback board PN 0431395
- Documentation and reference design CD-ROM

Optional items that also support development efforts include:

- Xilinx ISE® software
- JTAG cable or Xilinx Platform Cable USB

For assistance with any of these items, contact your local Xilinx distributor or visit the Xilinx online store at www.xilinx.com.

The heart of the Virtex-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit is the ML550 Development Board. This manual provides comprehensive information on Rev 1 and later revisions of this board.

Virtex-5 FPGA ML550 Networking Interfaces Development Board

The ML550 Development Board includes the following:

- XC5VLX50T-FFG1136 FPGA

- 64M x 8 DDR SDRAM memory

- Eight clock sources:

    ♦ 200 MHz, 250 MHz, 133 MHz, and 33 MHz on-board oscillators

    ♦ Two ICS8442 clock synthesizer devices

    ♦ Two sets of SMA differential clock input connectors

- One USB "B" port

- One 64 x 128 pixel LCD – Optional

- A System ACE™ CompactFlash (CF) Configuration Controller that allows storing and downloading of up to eight FPGA configuration image files

- Six Samtec LVDS connectors (a total of 53 differential input and 53 differential output channels)

- Onboard power regulators with ±5% output margin test capabilities, in 2.5% increments

Figure 1-1 shows the ML550 Development Board.
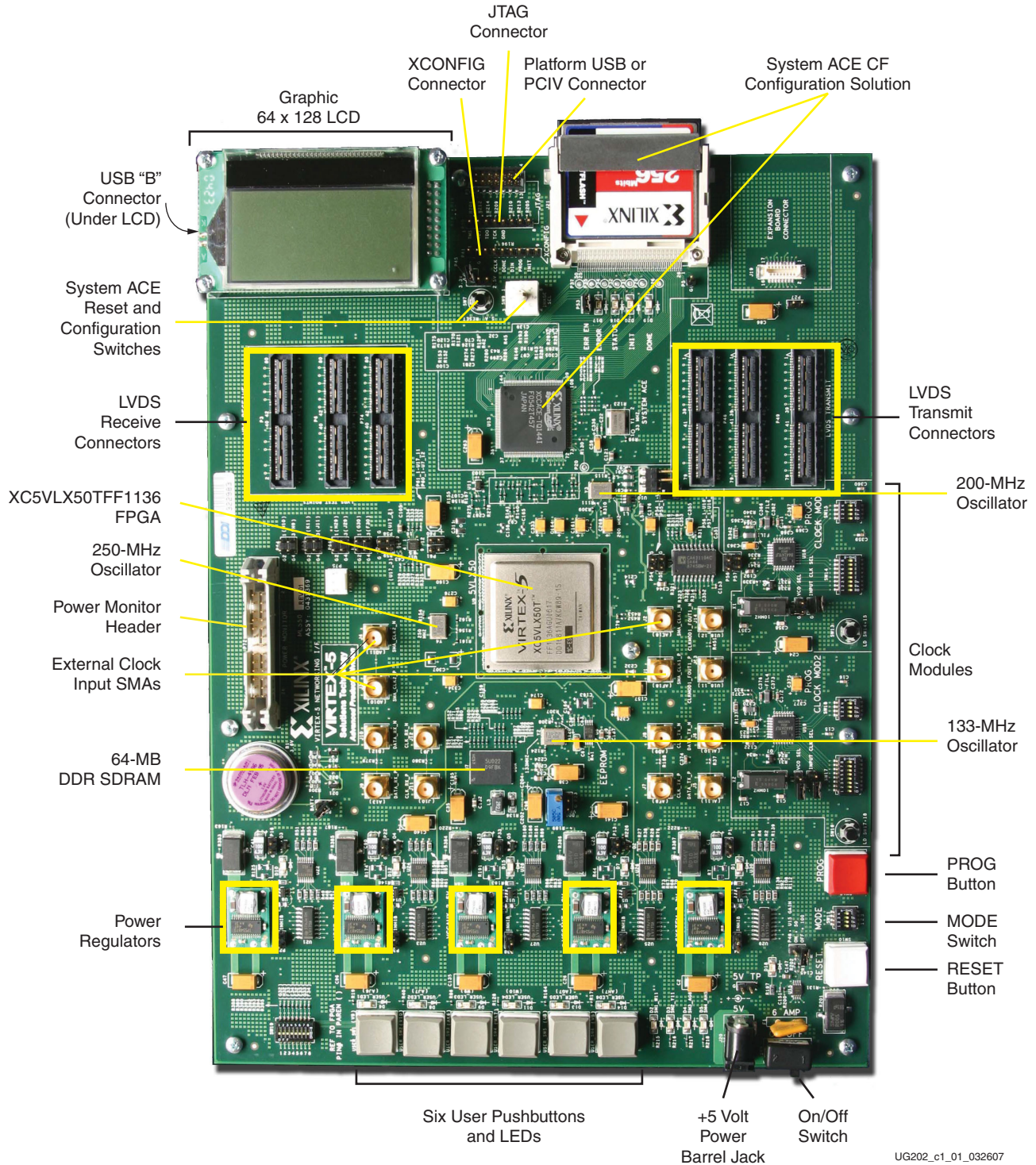
Figure 1-1: **Virtex-5 FPGA ML550 Networking Interfaces Development Board**

Getting Started

This chapter describes the items needed to configure the Virtex-5 FPGA ML550 Networking Interfaces Development Board. The ML550 Development Board is tested at the factory after assembly and should be received in working condition. It is set up to load a bitstream from the CompactFlash card through the System ACE controller U13.

Documentation and Reference Design CD-ROM

The CD-ROM included in the Virtex-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit contains the design files for the ML550 Networking Interfaces Platform, including schematics, board layout, and reference design files. Open the `ReadMe.txt` file on the CD-ROM to review the list of contents.

Quick Start Guide

Welcome to the ML550 Source Synchronous Interfaces Tool Kit!

Initial Setup

Check Kit Contents

The ML550 shipping carton contains:

- ML550 Board
- Compact Flash Card
- CD-ROM
- 120/240 VAC to 5 VDC 6A power supply with country-specific line cord
- USB Cable, B-to-A
- LVDS Loopback Board
- Welcome letter
- Misc. Xilinx Promo Kits and documentation

Unpack the Kit and Make Connections

- Remove the ML550 from the anti-static bag. Confirm that Power slide switch is OFF. Do not turn Power ON until instructed to do so.
- Remove the LVDS Loopback board from its bag, and install it on the ML550.
- Remove the Compact Flash card from its bag and install it into the ML550 at J21.

- Plug the 5V power supply line cord into a power outlet, and plug the barrel plug into the ML550 J20 jack.
- Plug the "B" end of the kit USB cable into the ML550 (the jack is under the LCD), and plug the "A" end into a PC USB port.

Installation

Silicon Labs USB-to-RS232 Bridge Chip Driver Installation

Assumptions:

- ♦ PC operating system is Microsoft Windows XP
- ♦ No previous versions of this driver have been installed on the PC
- ♦ The ML550 board is powered OFF
- ♦ The USB B-to-A cable is installed between the ML550 and the PC

1. Copy the ML550 BERT REV1.x.zip file from the kit CD-ROM to `C:\`.

2. Unzip the file. When this file is unzipped, a folder called `ML550 BERT REV1.x` is created.

3. Locate the self-extracting ZIP file `CP210x_Drivers.exe` in the folder `C:\ML550 BERT Rev1.x\USB_2_Serial Driver`. Double-click on this file.

   If the default target directory isn't changed, the folder `C:\SiLabs\MCU\CP210x` is created. This folder contains various drivers.

4. Turn on the ML550 power.

   Windows XP recognizes that new hardware is present, and opens the Add New Hardware Wizard.

5. Choose **Install from a list or specific location** and click **Next**.

6. Choose **Search for the best driver in these locations**. Enter the path `C:\SiLabs\MCU\CP210x\WIN` and click **Next**.

7. The wizard installs a driver and reports:

   ```
   The wizard has finished installing the software for CP2101 USB
   Composite Device.
   ```

   Click **Finish**.

8. Windows XP now recognizes the USB to Serial Bridge and wants to install its driver as well. Repeat step 5 and step 6.

9. The wizard installs another driver and reports:

   ```
   The wizard has finished installing the software for CP2101 USB to
   UART Bridge Controller.
   ```

10. Windows XP displays:

    ```
    Your new hardware is installed and ready to use.
    ```

Note: This driver assigns itself the lowest *unassigned* serial COM port number. This number varies with PC hardware configuration. COM3 or COM4 is typically assigned.

BERT GUI Tcl Interface Installation

1. Locate executable file `ActiveTcl8.4.7.0-win32-ix86-108887.exe` in `C:\ML550 BERT REV1.x` and double-click on it.

2. The Active State Active Tcl installer opens. Follow the dialog and accept the defaults.

    At the end of the process, the installer reports the folders created during the install. Click **Finish**.

3. Create a GUI shortcut for the Windows desktop:

    a. Locate executable file `gui_rev1.x.exe` in `C:\ML550 BERT REV1.x\GUI_Rev1.x`.

    b. Right-click on this file and choose **Create shortcut**.

    c. Drag the shortcut to the Windows XP desktop.

The BERT GUI is now ready to use.

ML550 Board Startup and Operation

1. Turn OFF the ML550 power.

2. Install either the LVDS Loopback board across the six LVDS Samtec connectors (if not already installed), or install a single Blue Ribbon cable between the center TX and RX Samtec connectors, P46 and P6 respectively.

3. Install the Compact Flash card into the J21 socket (if not already installed).

4. Confirm that the flash card image select rotary switch SW9 is set to position 0.

5. The CLOCK MOD 1 & 2 parallel programming DIP switches default to all OFF and can be safely ignored.

    The BERT test uses Clock Module 2 / U19. The GUI sets the Clock Module 2 / U19 initial frequency to 400 MHz.

6. Turn ON the ML550 power. The DONE LED D19 should come on.

7. On the PC, double-click on the `gui_rev1.x.exe` shortcut. The BERT GUI launches.

8. At the upper left are two selection boxes. The upper chooses the COM port, the lower chooses the test type. Click on the upper and select **COM4**. Click on the lower and select **PRBS15**.

9. Click on the big **Start/Restart** button.

    If the COM port is correct, the test begins.

    If the COM port is not correct, the GUI most likely will hang. If this occurs, close and relaunch the application. When repeating the selection sequence, choose COM3. If this also fails, repeat this procedure choosing a lower COM port number each time through.

    Some computers have more than four COM ports. It is possible that the USB-to-COM bridge driver will select a COM port that the GUI will not communicate with (e.g., COM14.) The workaround in this instance is to go to:

    Control Panel -> System -> Hardware -> Device Manager -> Ports

    Identify the port selected by the CP210x USB to UART driver. If the COM port is not **COM1**, **COM2**, **COM3**, or **COM4,** change the port using this path:

    Control Panel -> System -> Hardware -> Device Manager -> Ports -> CP210x USB to UART-> Port Settings -> Advanced COM Port Number

Select change to **COM#** where # is either 1, 2, 3, or 4.

10. The GUI reflects the frequency set at Clock Module 2 and initially reports 400 MHz. More information resides in the file
    `C:\ML550 BERT REV1.x\DDR_8TO1_16CHAN_PICO_REV1.x\README.doc.`
    Also refer to the `ML550 Networking Interfaces Board.ppt` presentation on the kit CD-ROM.

11. The clock frequency can be changed by clicking on the **+100 MHz**, **+10 MHz**, **–100 MHz**, and **–10 MHz** GUI buttons to the left of the Frequency display. More detailed information is available in the CD file `BERTGUI_README.doc`.

Programmable Clock Module Switch Position Chart

Four-Pole SW DIP2 Settings

	Switch Position			
	1	**2**	**3**	**4**
Always	OFF	OFF	OFF	OFF

Eight-Pole SW DIP1 Settings

	Switch Position							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
700 MHz	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
690 MHz	ON	OFF	ON	OFF	OFF	OFF	ON	OFF
680 MHz	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
670 MHz	ON	ON	OFF	OFF	OFF	OFF	ON	OFF
660 MHz	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
650 MHz	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF
600 MHz	OFF	OFF	ON	ON	ON	ON	OFF	OFF
400 MHz	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF

Hardware Description

A high-level block diagram of the Virtex-5 FPGA ML550 Networking Interfaces Development Board is shown in Figure 3-1, followed by a brief description of each board section.
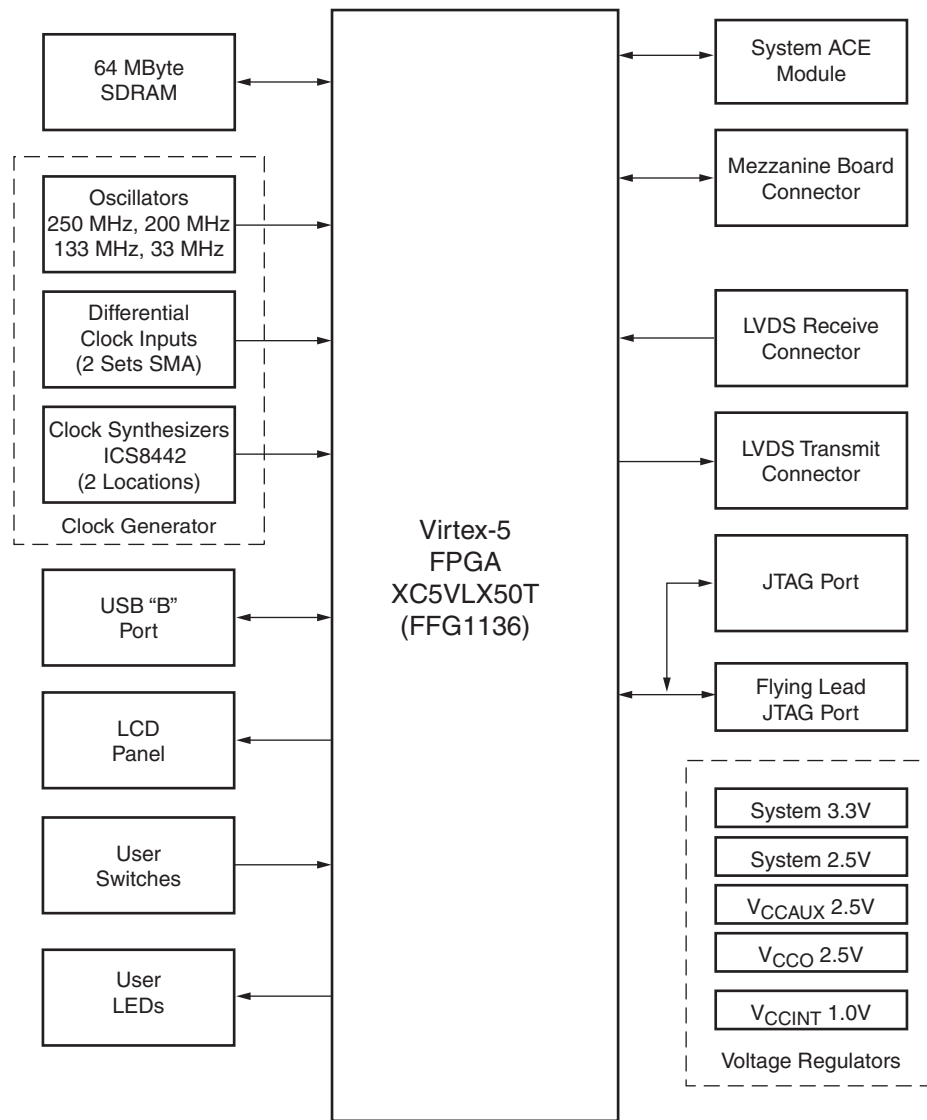
Figure 3-1: **Virtex-5 FPGA ML550 Networking Interfaces Development Board**

Clock Generation

The clock generation section of the ML550 Development Board provides all necessary clocks for the Virtex-5 FPGA. Eight clock sources are provided:

- Epson EG2121CA 2.5V 250-MHz differential LVPECL oscillator (Y4) for general use
- Epson EG2121CA 2.5V 200-MHz differential LVPECL oscillator (Y3) for Virtex-5 FPGA ISERDES support
- Epson EG2121CA 2.5V 133-MHz differential LVDS oscillator (Y2) for DDR memory interface
- Epson SG8002CA 3.3V 33-MHz LVCMOS single-ended oscillator (Y1) for SystemAce device (U13)
- Two differential SMA clock inputs (CLOCK-1: J3, J1 and CLOCK-2: J4, J2)
- Two clock synthesizer ICS8442 devices (U18,U19)

The differential SMA clock inputs are connected to the global clock inputs of the FPGA. An onboard 200-MHz oscillator calibrates the I/O delay, and an onboard 250-MHz oscillator is provided for general use.

The two ICS8442 clock synthesizer devices output differential LVDS clocks in the 31.25 MHz to 700 MHz range.

The on-chip LVDS differential terminator is recommended for use in designs. The clock is received by an IBUFGDS module, and beneath that module instantiation, the synthesis attribute DIFF_TERM must be set to TRUE. Refer to the *Virtex-5 FPGA User Guide* (UG190) for information and examples using SelectIO primitives for LVDS inputs.

Table 3-1 shows the clock generation components for the ML550 board.

Table 3-1: **Clock Generation – ML550 Rev 01 Board**

Clock Source Component	Reference Designator	Output Frequency	Output Type	Signal Name	FPGA Pin #		Bank
					P	**N**	
Epson SG8002CA	Y1	33 MHz	3.3V LVCMOS Single-Ended	SYSACE_CLK	V33	N/A	13
Epson EG2121CA	Y2	133 MHz	2.5V LVDS Differential	OSC_133M_P and N	R7	R8	12
Epson EG2121CA	Y3	200 MHz	2.5V LVPECL Differential	OSC_200M_P and N	L19	K19	3
Epson EG2121CA	Y4	250 MHz	2.5V LVPECL Differential	OSC_250M_P and N	H17	H18	3
ICS8442AY	U18	31.25 MHz	3.3V LVDS Differential #1	LVDSCLKMOD1_P and N	AH18	AG17	4
		to 700 MHz	3.3V LVDS Differential #2	CLKMOD1_FOUT1_P and N	J13	J14	N/A
ICS8442AY	U19	31.25 MHz	3.3V LVDS Differential #1	LVDSCLKMOD2A_P and N	AB30	AC30	17
		to 700 MHz	3.3V LVDS Differential #2	LVDSCLKMOD2B_P and N	AK28	AK27	21
SMA Connector	J1			SMA_CLK1_P	AF18	N/A	4
SMA Connector	J2			SMA_CLK1_N	N/A	AE18	4
SMA Connector	J3			SMA_CLK2_P	AD10	N/A	22
SMA Connector	J4			SMA_CLK2_N	N/A	AD11	22

SDRAM Memory

The ML550 Development Board provides 64 MBytes of SDRAM memory (Micron Semiconductor MT46V64M8BN-75). The high-level block diagram of the SDRAM interface is shown in Figure 3-2. Table 3-2 lists the SDRAM memory interface signals for the FFG1136 package used on the ML550 Development Board.

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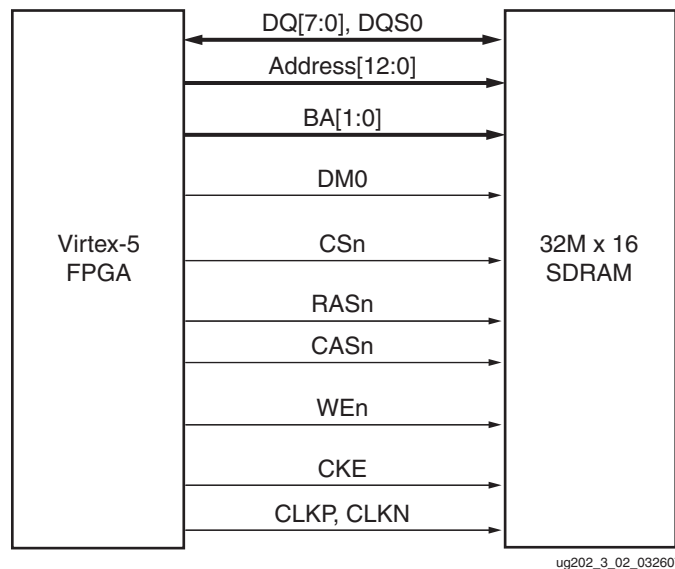
Figure 3-2: **Block Diagram of the SDRAM Interface**

Table 3-2: **SDRAM Memory Interface Signal Descriptions**

Signal Name	Description	FPGA Pin Number (FFG1136 Package, Bank 12)
A0	Address 0	J5
A1	Address 1	J6
A2	Address 2	T6
A3	Address 3	R6
A4	Address 4	K6
A5	Address 5	K7
A6	Address 6	P6
A7	Address 7	P7
A8	Address 8	L4
A9	Address 9	P5
A10	Address 10	N5
A11	Address 11	L6
A12	Address12	M7
DQ0	Data 0	T10
DQ1	Data 1	F6

Table 3-2: **SDRAM Memory Interface Signal Descriptions** *(Continued)*

Signal Name	Description	FPGA Pin Number (FFG1136 Package, Bank 12)
DQ2	Data 2	F5
DQ3	Data 3	R11
DQ4	Data 4	N7
DQ5	Data 5	N8
DQ6	Data 6	M5
DQ7	Data 7	M6
DQS0[1]	DQ Strobe	T9
BA0	Bank Select 0	G6
BA1	Bank Select 1	T11
DM0	Write Mask	G7
CSn	Chip Select	E7
RASn	Row Address Strobe	U7
CASn	Column Address Strobe	T8
WEn	Write Enable	E6
CLK_P	Positive Clock	H7
CLK_N	Negative Clock	J7
CKE	Clock Enable	U10

Notes:

1. Because DQS0 is not located on a clock capable I/O pin, the Xilinx MIG tool cannot be used to generate a SDRAM memory controller for the 64M x 8 SDRAM on the ML550 board.

Liquid Crystal Display

The ML550 Development Board provides an 8-bit interface to a 64 x 128 LCD panel (DisplayTechQ 64128E-FC-BC-3LP, 64 x 128). This display was chosen because of its possible use in embedded systems. Appendix C, "LCD Interface," describes the LCD operation in detail.

Table 3-3 describes the LCD interface signal descriptions for the FFG1136 package used on the ML550 Development Board.

Table 3-3: **LCD Interface Signal Descriptions**

Signal Name	LCD Pin Number	Description	FPGA Pin Number (FFG1136 Package, Bank 13)
V_{SS}	1	GND	Ground
V_{DD}	2	3.3V DC	Logic Supply
MI	3	H = 6800 CPU, L = 8080 CPU	Pull-up R14 to 3.3V
DB7	4	LCD Data Bit 7	AK33

Table 3-3: **LCD Interface Signal Descriptions** *(Continued)*

Signal Name	LCD Pin Number	Description	FPGA Pin Number (FFG1136 Package, Bank 13)
DB6	5	LCD Data Bit 6	AG32
DB5	6	LCD Data Bit 5	AH32
DB4	7	LCD Data Bit 4	AJ32
DB3	8	LCD Data Bit 3	AK32
DB2	9	LCD Data Bit 2	AL34
DB1	10	LCD Data Bit 1	AL33
DB0	11	LCD Data Bit 0	AM33
E	12	LCD Enable	AN33
R/W	13	LCD Write	AN32
RS	14	LCD Register Select	AP32
RST	15	LCD Reset	AM32
CS1B	16	LCD Chip Select	AN34
LED +	17	LCD Backlight Anode	Ctrl. Transistor Q1
LED –	18	LCD Backlight Cathode	Ground
LCD_BL_ON	N/A	LCD Backlight Control	AK34

The LCD can display alphanumeric (ASCII) information; however, a hardware character generator must be designed in the FPGA fabric in order to display the characters on the LCD screen. A character-type display (with on-board character generator) can also be connected because the graphical LCD has the same interface as many character-type LCD panels.

Display Hardware Design

The I/Os of the FPGA function at 2.5V. The FPGA is connected to the graphic LCD display through a set of voltage-level converting devices. These switches translate the 2.5V I/O signals to the 3.3V signals that the LCD display requires.

Control for the LCD panel is based on the KS0713 controller from Samsung. The KS0713 is a 65-column, 132-segment driver-controller device for graphic dot matrix LCD display systems. The chip accepts serial or parallel display data. The 8-bit parallel interface is compatible with most LCD panel manufacturers. The serial connection mode is write only.

Extra features added to the interface in addition to the normal parallel signals are:

- Intel or Motorola compatible interface
- External reset of the chip
- External chip select

The interface also contains the following built-in options for the display and controller:

- On-chip oscillator circuitry
- On-chip voltage converter (x2, x3, x4, and x5)

- A 64-step electronic contrast control function

Table 3-4 summarizes the controller specifications.

Table 3-4: **Display Controller Specifications**

Parameter	Specification
Supply Voltage	2.4V to 3.6V (V_{DD})
LCD Driving Voltage	4V to 15V ($V_{LCD} = V_0 - V_{DD}$) Generated On-Chip
Power Consumption	70 µA typical ($V_{DD} = 3V$, x4 boost, $V_0 = 11V$, internal supply = ON)
Sleep Mode	2 µA
Standby Mode	10 µA

Hardware Schematic Diagrams

Figure 3-3 shows the schematic for connections to the display. Figure 3-4 shows a block diagram of the display, and Figure 3-5 shows the dimensions of the display.
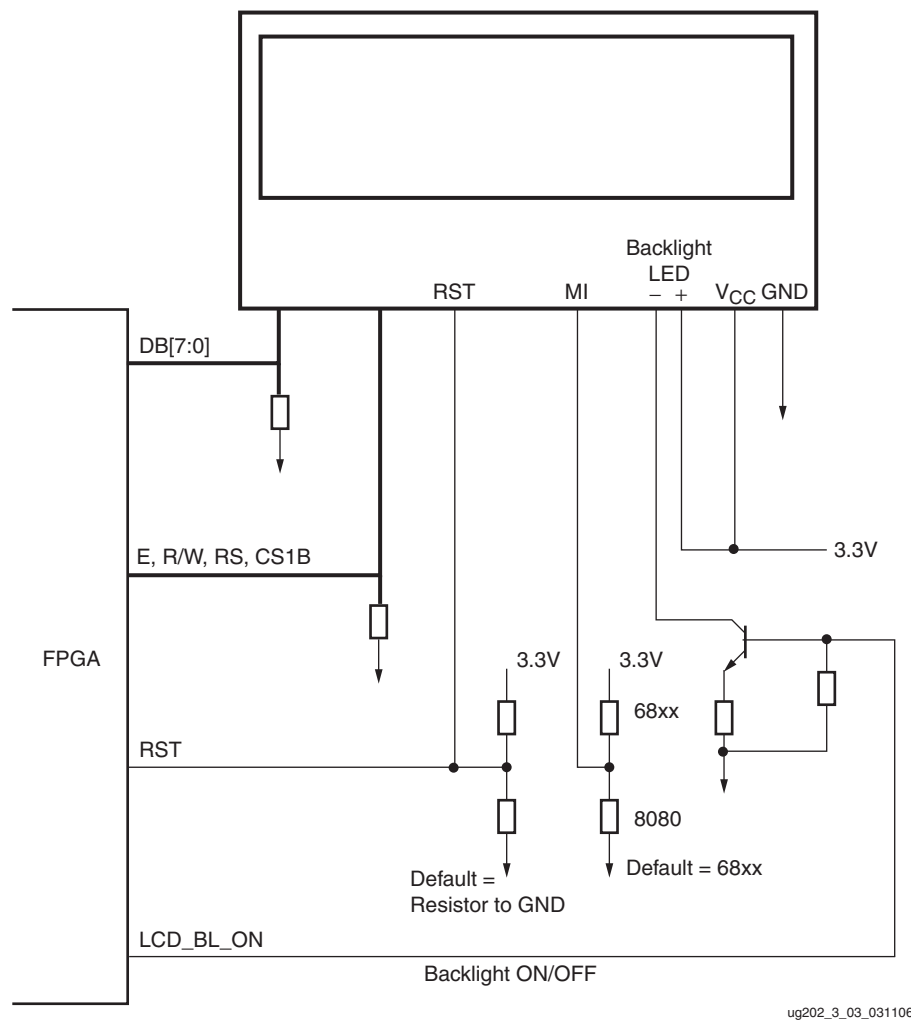

ug202_3_03_031106

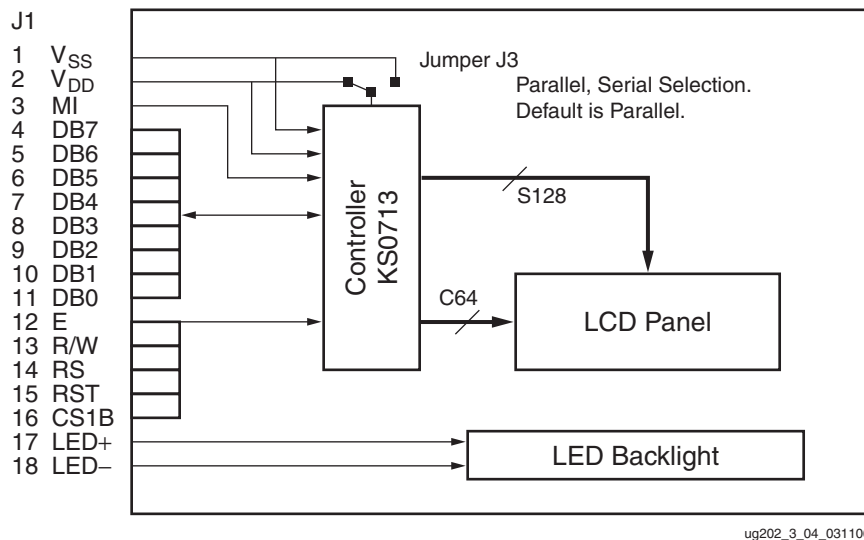*Figure 3-3:* **Display Schematic Diagram**

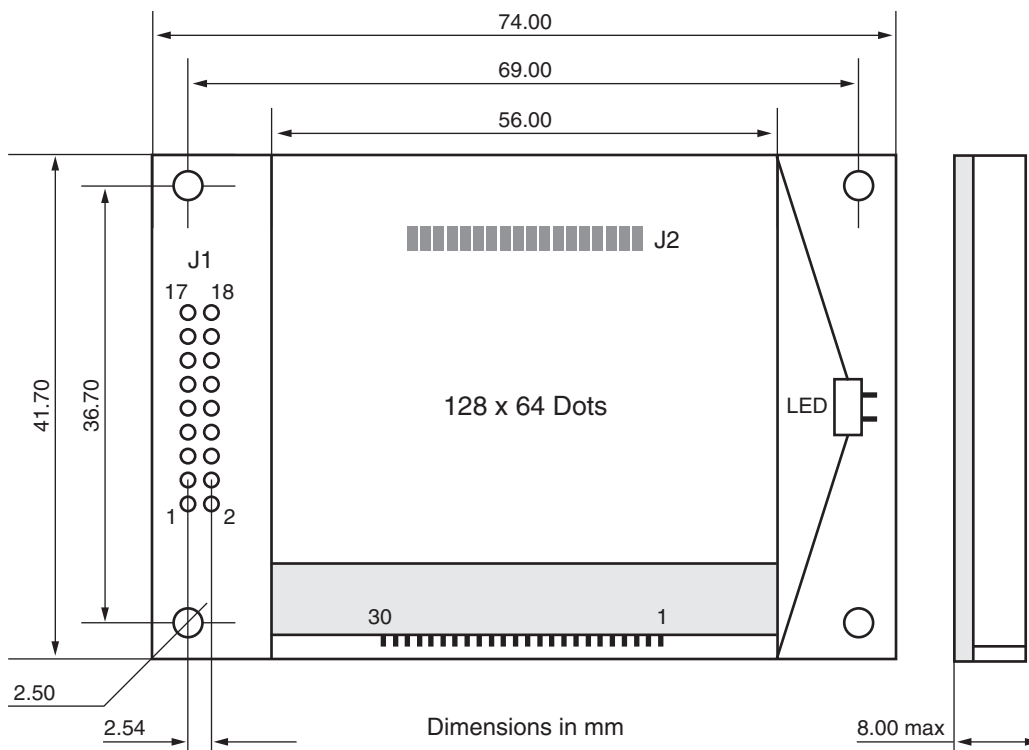*Figure 3-4:*   **64128EFCBC-3LP Block Diagram**

Figure 3-5:   **64128EFCBC-3LP Dimensions**

User LED

The ML550 Development Board provides six user LEDs that can be turned ON by driving the LEDs signal Low. Table 3-5 describes the user LEDs and their associated pin assignments for the FFG1136 FPGA used on the ML550 Development Board.