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Virtex-5 FPGA ML555 Development Kit for PCI and PCI Express Designs

User Guide

UG201 (v1.4) March 10, 2008

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
09/27/06	1.0	Initial Xilinx release.
12/27/06	1.1	Changed device package to FFG1136. Inserted new Table 3-3 showing correlation between PCIe® signals, P13 connector, FPGA pins, and GTP_DUAL tile. Revised Chapter 3, “Hardware Description,” to reflect board design change where ICS874003-02 PCI Express® Clock Jitter attenuator module is now a customer option (added Figure 3-8, and changed Table 3-1, Table 3-9, Table 3-18, Table 3-19, Table 3-20, and “Serial Bus Clocking with Optional ICS874003-02 Clock Jitter Attenuator (PCI Express Operation),” page 60). Removed Appendix A.

Date	Version	Revision
02/27/07	1.2	Changed document title and updated "Additional Documentation," page 7. Specified FPGA device speed grade as "-1C ES". Updated "Initial Board Checks Before Applying Power," page 19. Corrected board reference designator for Table 3-4, page 30 to use P1 as PCI™ Edge Connector pinout. Updated "DDR2 SDRAM SODIMM," page 34 to reference DDR2 reference design included with kit. Added lane assignments to Table 3-20, page 58. Added link to www.idt.com for availability of clock jitter attenuator circuits on page 60. Updated Table 3-33, page 80 to include ML555 support for plugging board into 16-lane add-in card connector. Updated Table 3-37, page 86 to include reference designs pre-loaded into ML555 Platform Flash devices. Add Note 3 to Table 4-1, page 89; Slave SelectMAP not supported. Updated "SelectMAP Clock Selection" including Table 4-7 and Figure 4-8. Added reference to the Development System Reference Guide for PROMGen and BitGen software applications. Updated "Specifying the Xilinx PROM Device" including Figure 4-10 and Figure 4-13. Added Figure 4-14 and Figure 4-15.
06/18/07	1.3	Updated Table 1-1, page 14 to clarify version and build information for PCI and PCI-X IP cores. Revised Serial Bus Development section. Removed "ES" from FPGA part number. Added footnote 3 to Table 3-3, page 27. Updated Figure 3-8, page 55 and Figure 3-9, page 56 to include a 4.7KΩ pull-up resistor on the SATA_MGT_CLKSEL FPGA output and labeled the Clock MUX inputs. Defined the SATA_MGT_CLKSEL default selection in Table 3-19, page 57 for FPGA output H15. Added additional text to footnote 6 in Table 3-20, page 58. Updated "Parallel Mode Operation," page 62 to indicate pressing and releasing of SW9 and SW11 to parallel load clock synthesizers after power on to guarantee clock frequency. Updated Figure 3-14, page 76 and Table 3-34, page 81. Added footnote 1 to Table 4-5, page 95. Updated "Generic Dynamic Reconfiguration," page 98 and "Platform Flash Image Generation and Programming," page 101 to include process steps and screen shots from ISE 9.1i. Inserted two new figures (Figure 4-11, page 105 and Figure 4-12, page 105).

Date	Version	Revision
03/10/08	1.4	Added additional reference documents and application notes in "Additional Documentation," page 7. Added link to ML555 website in "About the Virtex-5 FPGA ML555 Development Kit," page 13. Updated "Serial Bus Development," page 15, including removal of Virtex-5 LogiCORE Endpoint Block Wrapper. Included Platform USB Programming Cable and ISE Evaluation Software in "Kit Contents," page 15. Specified 30 MHz LVCMOS oscillator as one of three on board clock sources in "ML555 Board," page 15. Updated Figure 3-1, page 21 to reflect "as built" 30 MHz LVCMOS oscillator. Added reference and link to Xilinx application notes XAPP1022 and XAPP1002 in "Edge Connector for PCI Express Operation," page 23. Added footnote 6 to Table 3-1, page 24 to identify FPGA connection of PCIE_PERST. Added PCIE_PERST to Table 3-3, page 27. Added reference and link to XAPP999 in "Reference Designs for PCI and PCI-X Operation," page 33. Added reference and links to Xilinx application notes XAPP858 and XAPP865 in "DDR2 SDRAM SODIMM," page 34. Corrected FPGA pin assignments for IIC_SDA_SFP{1/2} and IIC_SCK_SFP{1/2} signals and updated footnotes 2 and 5 in Table 3-7, page 39. Added reference and link to application note XAPP870 in "Serial ATA Interface," page 40. Corrected FPGA pin assignment for P1_RCLK1 signal in Table 3-11, page 43. Added website link to download Silicon Laboratories VCP device drivers in the "USB to UART Bridge," page 51. Specify 30 MHz oscillator frequency for component Y2 in Table 3-18, page 53. Changed signal name for FPGA GCLK input pin L19 to FPGA_GCLK_30MHZ in Figure 3-8, page 55, Figure 3-9, page 56, and Table 3-19, page 57. Changed signal name for FPGA GCLK input pin AD32 to FPGA_GCLK_30MHZ in Table 3-26, page 70. Added footnote to Table 3-37, page 86. Updated footnote 3 in Table 4-1, page 89 to recommend Master SelectMAP configuration of the ML555. Changed CPLD CLK to 30 MHz in Figure 4-5, page 92, Figure 4-6, page 98, and Figure 4-7, page 99 as well as Table 4-4, page 94. Changed oscillator Y2 frequency to 30 MHz in Figure 4-8, page 100. Added footnote to Table 4-7, page 100 concerning CCLK configuration frequency recommendation. Added BitGen command sequence to demonstrate selection of 20 MHz CCLK configuration clock in "Platform Flash Image Generation and Programming," page 101.

Table of Contents

Chapter 4: Configuration

About This Guide

This user guide is a description of the Virtex™-5 FPGA ML555 Development Kit for PCI™ and PCI Express® designs. Complete and up-to-date documentation of the Virtex-5 family of FPGAs is available on the Xilinx website at http://www.xilinx.com/virtex5.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction"
- Chapter 2, "Getting Started"
- Chapter 3, "Hardware Description"
- Chapter 4, "Configuration"

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.
- Virtex-5 Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.
- Virtex-5 FPGA User Guide

  This user guide includes chapters on:
  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM and FIFO memory
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - I/O Logic Resources
  - Advanced I/O Logic Resources

- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This user guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platform devices.

- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This user guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT and SXT platform devices.

- Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs

  This user guide describes the integrated Endpoint blocks in the Virtex-5 LXT and SXT platform devices for PCI Express® designs.

- Virtex-5 FPGA XtremeDSP Design Considerations

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E.

- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.

- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.

- Virtex-5 FPGA Packaging Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.

- Virtex-5 PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

The following documents provide supplemental material useful to this user guide:

1. DS090, *CoolRunner-II CPLD Family*
2. DS123, *Platform Flash In-System Programmable Configuration PROMs*
3. UG065, *PHY Daughter Card User Guide*
4. XAPP938, *Dynamic Bus Mode Reconfiguration of PCI-X and PCI Designs*
5. XAPP1022, *Using the Memory Endpoint Test Driver (MET) with the Programmed Input/Output Example Design for PCI Express Endpoint Cores*
6. XAPP1002, *Using ChipScope Pro to Debug Endpoint Block Plus Wrapper, Endpoint, and Endpoint PIPE Designs for PCI Express*
7. XAPP999, *Reference System: PLBv46 PCI Using the ML555 Embedded Development Platform*
8. XAPP858, *High-Performance DDR2 SDRAM Interface in Virtex-5 Devices*
9. XAPP865, *Hardware Accelerator for RAID6 Parity Generation / Data Recovery Controller with ECC and MIG DDR2 Controller*
10. UG086, *Xilinx Memory Interface Generator (MIG) User Guide*
11. XAPP870, *Serial ATA Physical Link Initialization with the GTP Transceiver of Virtex-5 LXT FPGAs*

12. XAPP693, *A CPLD-Based Configuration and Revision Manager for Xilinx Platform Flash PROMs and FPGAs*

The Endpoint Block Plus for PCI Express solution from Xilinx is a reliable, high-bandwidth, scalable serial interconnect building block for use with the Virtex-5 LXT and SXT platform FPGAs. The core instantiates the Virtex-5 FPGA Integrated Block for PCI Express designs found in the Virtex-5 LXT and SXT devices. The Endpoint Block Plus core is a Xilinx CORE Generator™ IP core included in the latest IP Update on the Xilinx IP Center. Included with the Xilinx IP are a data sheet, a getting started guide, and a user guide. These documents are generated by the CORE Generator tool when starting a design project. The documents can be downloaded from the Xilinx website at:

http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ds551.pdf

http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_gsg343.pdf

http://www.xilinx.com/support/documentation/ip_documentation/pcie_blk_plus_ug341.pdf

Additional technical information on PCI Express solutions is available at:

http://www.xilinx.com/pciexpress

Xilinx provides customizable LogiCORE™ Initiator/Target cores for PCI and PCI-X applications designed to work with Virtex-5 FPGAs. Included with the Xilinx IP are a data sheet, getting started guide, and user guide. These documents are generated by the CORE Generator tool when starting a design project. Additional information is available on the Xilinx website at:

http://www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm

PCI, PCI-X™, and PCI Express specifications are available from the PCI Special Interest Group (PCISIG). Contact the PCI Special Interest Group office to obtain the latest revision of these specifications. Questions regarding the PCI Local Bus Specification or the PCI-X Addendum or membership in the PCI Special Interest Group can be forwarded through:

PCI Special Interest Group (PCI-SIG)
5440 SW Westgate Dr., #217
Portland, OR 97221

Phone: 800-433-5177 (inside the U.S.), 503-291-2569 (outside the U.S.)
Fax: 503-297-1090
e-mail: administration@pcisig.com

Website: http://www.pcisig.com

- PCI Local Bus Specification, Revision 3.0
- PCI-X Addendum to the PCI Local Bus Specification
- PCI Express Base Specification
- PCI Express Card Electromechanical Specification

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-5 FPGA Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Documentation" for details. Refer to "Clock Management Technology (CMT)" in Chapter 2 for details.
Red text	Cross-reference link to a location in another document	See Figure 5 in the *Virtex-5 FPGA Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

Chapter 1

Introduction

About the Virtex-5 FPGA ML555 Development Kit

To develop parallel Peripheral Component Interconnect (PCI™) bus and serial PCI Express® bus add-in card applications, the Virtex™-5 FPGA ML555 board is configured and then plugged into a parallel PCI bus system unit or a serial PCI Express system unit. The board supports 32-bit or 64-bit PCI bus datapaths. The ML555 board has an eight-lane connector that allows the board to be plugged into an eight-lane add-in card socket for PCI Express operation. The ML555 kit does not include a lane conversion adapter, which would allow the eight-lane ML555 board to plug into an add-in card socket for single-lane PCI Express operation.

Additional information and design resources associated with the ML555 development kit is available at:

http://www.xilinx.com/products/devkits/HW-V5-ML555-G.htm

Parallel Bus Development for PCI Operation

This Virtex-5 FPGA based kit provides a development platform for designing and verifying PCI and PCI-X™ applications utilizing Xilinx LogiCORE™ intellectual property (IP) cores in a 3.3V signaling environment. The ML555 board is intended to plug-in to a 3.3V keyed system board. The ML555 board is not a Universal add-in card nor is it intended to plug into a 5V keyed system board. Figure 1-1 shows how to identify a 3.3V system board slot (left side) from a non-supported 5V system board slot (right side).

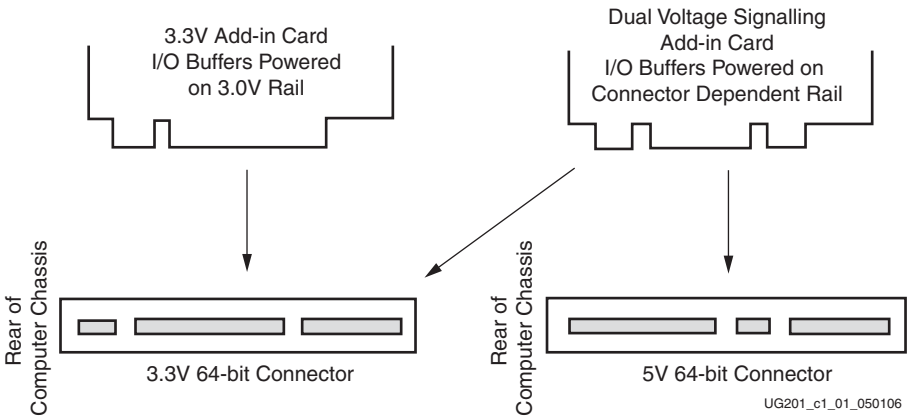

Figure 1-1: **Add-in Card Connectors**

The ML555 board is supported by Xilinx LogiCORE IP versions 4 and 6, respectively. Each core has a primary version number, shown in Table 1-1, followed by a revision or build number. More information about the current versions of these cores is available in the LogiCORE data sheets for the PCI and PCI-X section of the PCI/PCI-X product lounge (refer to http://www.xilinx.com/products/logicore/lounge/lounge.htm). Table 1-1 lists the Xilinx cores for PCI and PCI-X operation.

Table 1-1: **Xilinx Cores Supporting PCI and PCI-X Operation**

Version	Bus Mode	Bus Width	Clock Frequency	Clock Type (FPGA Pin #)
v4	PCI	32 bits	33 MHz	Global (J14)
v4	PCI	32 bits	66 MHz	Global (J14)
v4	PCI	64 bits	33 MHz	Global (J14)
v6	PCI-X	64 bits	133 MHz	Global (J14)
v6	PCI-X	64 bits	100 MHz	Global (J14)
v6	PCI-X	64 bits	66 MHz	Global (J14)
v6	PCI	64 bits	33 MHz	Global (J14)

These Xilinx interface cores are pre-implemented and fully tested modules for Xilinx FPGAs.

The v4 64-bit interface is compliant with the PCI Local Bus Specification, revision 3.0. The v6 64-bit interface is compliant with the PCI Local Bus Specification, revision 3.0, and the PCI-X Addendum, revision 2.0.

The pinout for each Virtex-5 device and the relative placement of the internal logic are predefined. Critical paths are controlled by constraints to ensure predictable timing, significantly reducing the engineering time required to implement the bus interface portion of a user design. When targeting an XC5VLX50T-FFG1136 FPGA, the Xilinx CORE Generator™ tool provides an example design and a constraints file utilizing the ML555 board pinout for PCI and PCI-X designs.

Resources can instead be focused on unique user application logic in the FPGA and on the system-level design. As a result, the Xilinx interface products for PCI and PCI-X operation minimize product development time.

The following links provide more information:

- Xilinx LogiCORE products:
  www.xilinx.com/products/design_resources/conn_central/index.htm
- PCI and PCI-X specific applications:
  www.xilinx.com/products/design_resources/conn_central/protocols/pci_pcix.htm

Included with the purchase of the ML555 development kit is a 90-day access to full system hardware evaluation versions of the Virtex-5 FPGA LogiCORE products for PCI and PCI-X designs. The following link provides additional information specific to the ML555 board and LogiCORE products:

www.xilinx.com/ipcenter/ml555/ml555_eval_instr.htm

Serial Bus Development

The ML555 board is supported by a LogiCORE endpoint wrapper to configure the Integrated Endpoint Block for PCI Express operation in Virtex-5 LXT and SXT FPGAs:

- *Virtex-5 FPGA LogiCORE Endpoint Block Plus Wrapper for PCI Express designs*

  This is the recommended wrapper for PCI Express designs. It provides many ease-of-use features and optimal configuration for Endpoint applications while simplifying the design process and reducing the time-to-market.

The endpoint solution is delivered through the Xilinx CORE Generator tool. Full access to the core, including bitstream generation capability, can be obtained through registration at no extra charge.

Additional technical information on Xilinx PCI Express solutions is available at:

www.xilinx.com/pciexpress

Refer to UG197, *Virtex-5 Integrated Endpoint Block User Guide for PCI Express Designs* for more information on the integrated Endpoint solution.

Kit Contents

The ML555 board kit includes the following:

- Virtex-5 FPGA ML555 board (XC5VLX50T-FFG1136C-1 speed grade FPGA)
- Documentation and reference design CD
- Time-out evaluation licenses for the LogiCORE IP for PCI and PCI-X designs
- Drivers for Jungo Software Technologies WinDriver device driver development kit can be downloaded from www.jungo.com/dnload.html and evaluated for 60 days
- Xilinx Platform Cable USB programming cable
- ISE™ evaluation software

For assistance with any of these items, contact your local Xilinx distributor or visit the Xilinx online store at www.xilinx.com.

The heart of the kit is the ML555 board. This manual provides comprehensive information on this board.

ML555 Board

The ML555 board includes the following:

- XC5VLX50T-FFG1136C -1 speed grade FPGA
- 200-pin 1.8V SODIMM socket with 256 MB (32M x 64 bit) DDR2 SDRAM SODIMM
- Three on-board clock sources, two differential SMA clock inputs, and two programmable clock synthesizers:
  - 30 MHz LVCMOS
  - 125 and 200 MHz Epson 2.5V EG-2121CA LVDS and LVPECL, respectively
- One Universal Serial Bus (USB) 2.0 port (USB interface cable not provided)
- Support for up to four FPGA design images in two Xilinx XCF32P-FSG48C Platform Flash configuration PROM devices
- Static or dynamic device reconfiguration support with the XC2C32 CoolRunner™ II CPLD

- 64-bit 3.3V system board keyed connector for PCI or PCI-X operation
- Support for Endpoint designs in x1, x4, and x8 lane configurations
- Two Small Form-factor Pluggable (SFP) Transceiver module ports (SFP modules are not included)
- Xilinx Generic Interface (XGI) headers support installation of Xilinx Ethernet PHY daughtercard (sold separately) for 10/100/1000 Mb Ethernet connectivity
- Two SAMTEC LVDS interface connectors with up to 24 high-speed LVDS channels each (cables sold separately)
- One Serial ATA (SATA) disk drive interface connector (SATA cable not provided)
- One set of SMA ports for offboard GTP transceiver connectivity
- User pushbutton switches and LEDs
- Device configuration through on-board Platform Flash or Xilinx Platform Cable USB
- PCI clocking support for global and regional clocking applications
- On-board power regulators (3.0V PCI, 2.5V, 1.8V, 1.0V, 0.9V V_{TT})
- Two programmable clock synthesizer chips to support DDR2 memory interfaces, 10/100/1000 Mb Ethernet protocols, SATA, Fibre Channel, Aurora, and other serial GTP baud rates

Available Xilinx Accessories

The ML555 board has one set of SMA connectors connected to one of the GTP transceiver ports of the XC5VLX50T FPGA. Xilinx sells a number of SMA conversion module boards that permit the conversion of the on-board SMA interface to other popular multi-gigabit serial connector interfaces. These accessories boards are available through your local Xilinx Sales office.

Xilinx also provides an Ethernet PHY daughtercard that can be used to provide dual Ethernet connectivity to the ML555 development kit.

Note: Not all accessories are RoHS compliant, and they might not be available in all countries. Contact your local Xilinx Sales office to determine product availability.

Conversion Module, SMA to SATA (HW-AFX-SMA-SATA)

The SMA to SATA module can be used in conjunction with the ML555 SMA connectors. The ML555 only provides one set of SMA connectors, whereas the HW-AFX-SMA-SATA conversion module contains two sets of SMA connectors and two SATA connectors. DC power is not provided to the SATA disk drive from either the ML555 board or the conversion module.

The SMA to SATA conversion module can be ordered from Xilinx as part number HW-AFX-SMA-SATA. Contact your local sales office for pricing information. Additional information on the conversion module is available from the Xilinx website at:

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=HW-AFX-SMA-SATA

Conversion Module, SMA to RJ45 (HW-AFX-SMA-RJ45)

The SMA to RJ45 module can be used in conjunction with the ML555 SMA connectors to convert the SMA interface to a RJ45 interface. This adapter does not support 10/100/1000BASE-T applications.

The SMA to RJ45 conversion module can be ordered from Xilinx as part number HW-AFX-SMA-RJ45. Contact your local sales office for pricing information. Additional information on the conversion module is available from the Xilinx website at:

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=HW-AFX-SMA-RJ45

Conversion Module, SMA to HSSDC2 (HW-AFX-SMA-HSSDC2)

The SMA to HSSDC2 module can be used in conjunction with the ML555 SMA connectors to convert the SMA interface to a HSSDC2 interface.

The SMA to HSSDC2 conversion module can be ordered from Xilinx as part number HW-AFX-SMA-HSSDC2. Contact your local sales office for pricing information. Additional information on the conversion module is available from the Xilinx website at:

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=HW-AFX-SMA-HSSDC2

PHY Daughtercard (HW-AFX-BERG-EPHY)

The PHY daughtercard plugs into the XGI headers on the ML555 board. The PHY daughtercard provides Ethernet capability to the ML555 development platform by using two Marvel Alaska 88E1111 Gigabit over copper transceivers. These PHY devices perform all physical layer (PHY) functions, operate at 10/100/1000 Mb/s and support many interfaces of the embedded tri-mode Ethernet MAC in the Virtex-5 FPGA.

The PHY daughtercard can be ordered from Xilinx as part number HW-AFX-BERG-EPHY. Contact your local sales office for pricing information. Additional information on the PHY daughtercard is available from the Xilinx website at:

www.xilinx.com/xlnx/xebiz/designResources/ip_product_details.jsp?key=HW-AFX-BERG-EPHY

Chapter 2

Getting Started

This chapter describes the items needed to configure the Virtex-5 FPGA ML555 board. The ML555 board is tested prior to shipment and should work out of the box. The installer is recommended to inspect the board prior to use and confirm proper jumper and switch settings as directed in this user guide.

The ML555 board must be plugged into either a parallel bus expansion slot for PCI systems or a serial system bus expansion slot for PCI Express systems. The DC power provided to the ML555 board from the PCI Express and PCI buses is different. The ML555 system power configuration must be properly configured through board headers and shunts prior to plugging into the system unit. Failure to configure the ML555 DC power system might result in damage to the ML555 board or the system unit.

Contact Xilinx Technical Support with any questions about proper configuration of the ML555 prior to powering up a system at:

http://www.xilinx.com/support/clearexpress/websupport.htm

Documentation and Reference Design CD

The CD included in the Virtex-5 FPGA ML555 board kit contains the board design files, including schematics, PCB layout, and bill of materials. FPGA and CPLD design constraint files are included on the CD. This file provides a signal listing and physical FPGA pin locations (LOC) constraint to get started designing user applications with the Xilinx ISE software. Signal names can be changed to match user preferences if the board schematic signal names are not identical to the top-level user design file names. Open the `ReadMe.txt` file on the CD to review the list of contents.

Initial Board Checks Before Applying Power

Note: These steps **MUST** be performed before plugging in the ML555 board:

1. Set up the Configuration Mode Switch SW5 for Master SelectMAP. See Table 4-1, page 89 and Figure 4-2, page 89.
2. Configure Jumper Block P2 to select configuration CCLK source (FPGA). See Table 4-7, page 100 and Figure 4-8, page 100.
3. Configure Jumper Block P3 to select one of four Platform Flash configuration files or use JTAG programming cable to load user design. See Table 3-37, page 86.
4. Switch SW8: selects the FPGA V_{CCINT} source (PCI or PCI Express bus) as described in "ML555 DC Power System," page 75.
5. Jumper Block P18: enables the 12V to 5V enable for PCI Express operation as described in "ML555 DC Power System," page 75.

The ML555 board now can be plugged into a powered down 3.3V (only) add-in card slot for PCI Express or PCI/PCI-X operation. See the `cd_rom.txt` file on the CD.

Chapter 3

Hardware Description

A high-level block diagram of the Virtex-5 FPGA ML555 board is shown in Figure 3-1, followed by a brief description of each board section. Figure 3-2 is a photograph of the ML555 board with the key interfaces marked.

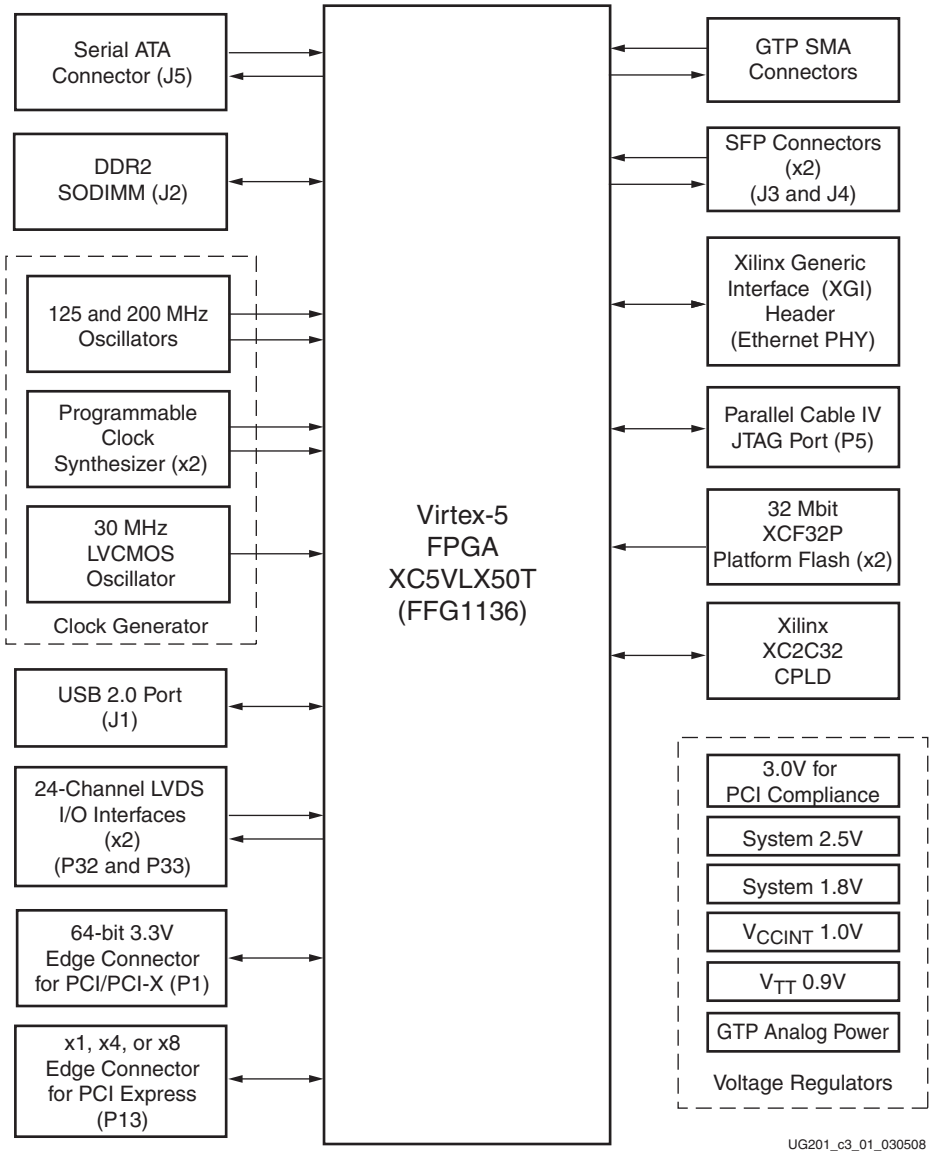

Figure 3-1: **ML555 Board Block Diagram**

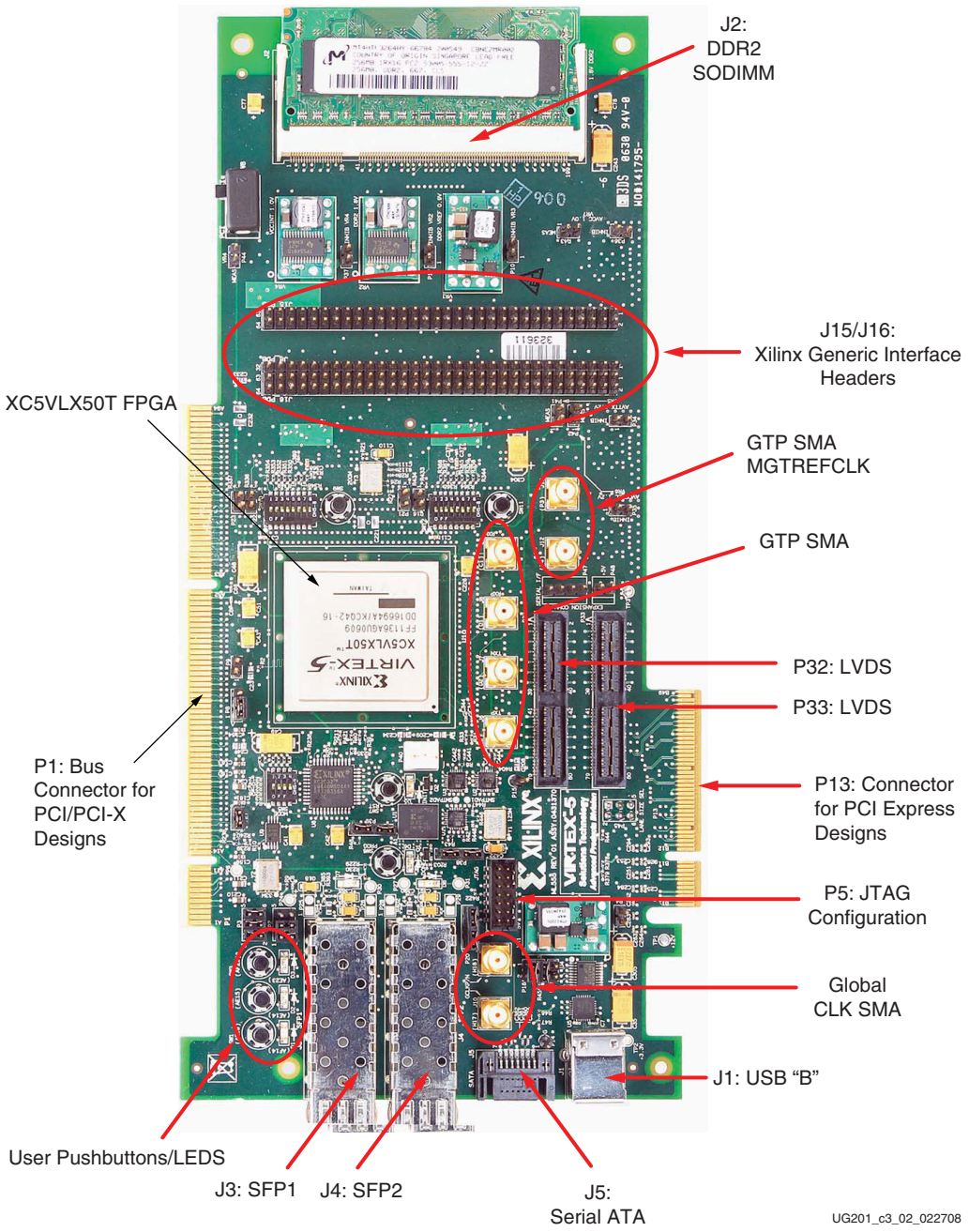

Figure 3-2: **Annotated ML555 Board**

The CD included in the kit contains ML555 board schematics and layout files.

Edge Connector for PCI Express Operation

Caution! PCI and PCI Express system units provide different DC voltages to the add-in card connectors. Before plugging the ML555 board into the system unit, the power configuration header settings must be reviewed to verify that the board will be powered properly. Failure to configure the power system properly could result in damage to the system unit or the ML555 board. Refer to Figure 3-16, page 78 to see how the SW8 switch and the P18 connector are configured for PCI Express power.

Figure 3-3 shows the location of the edge connector and power management headers for PCI Express systems.

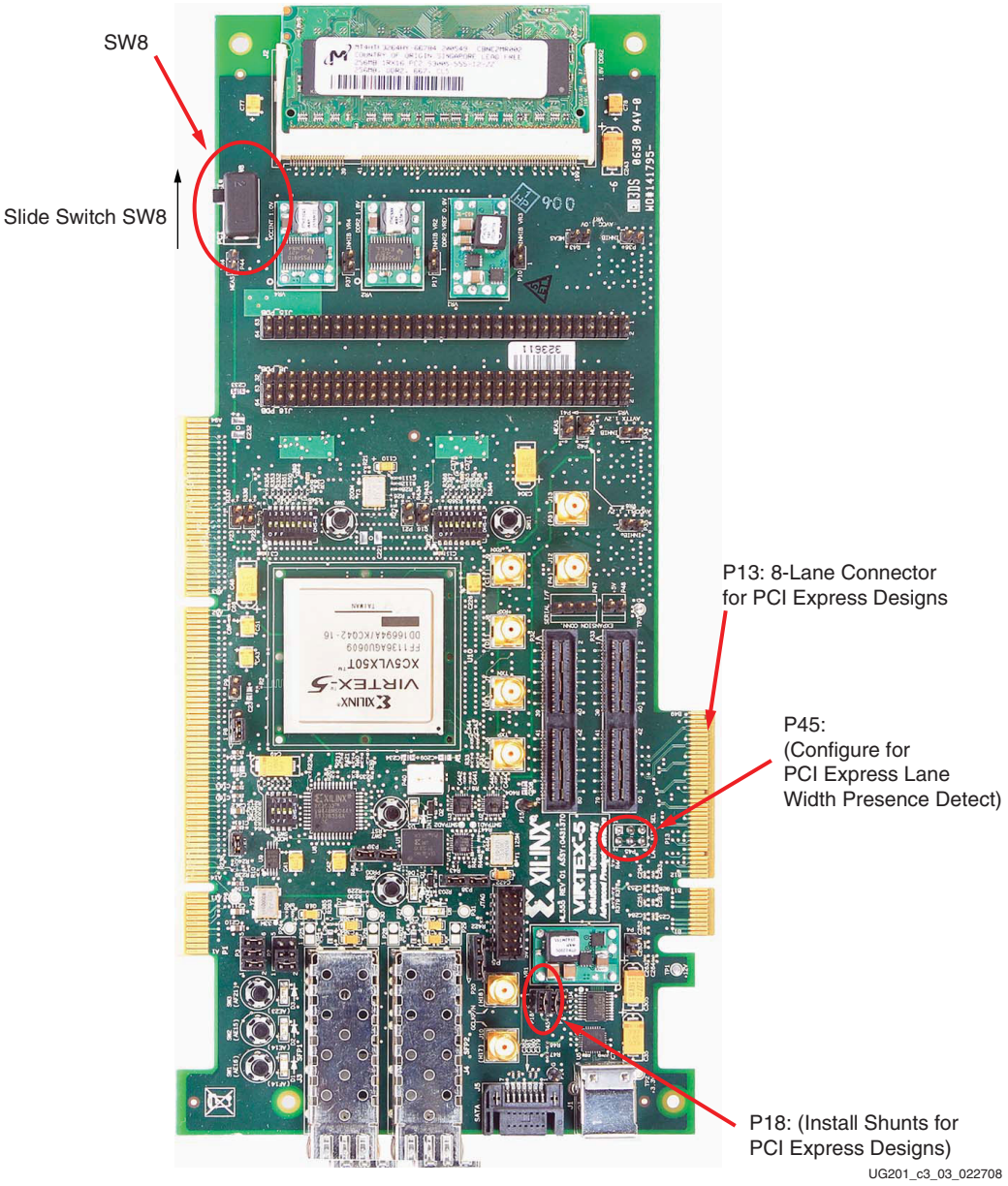

Figure 3-3: **Connector and Power Management Headers for PCI Express Designs**

Table 3-1 shows the connector pin assignment for PCI Express designs. The board supports x1, x4, and x8 endpoint designs. The ML555 board is an endpoint add-in card. Port names are with respect to the system board host.

Table 3-1: **P13 Edge Connector Socket Pinout for PCI Express Designs**

P13 A Side	Signal	P13 B Side	Signal
A1	PCIE_PRSNT1_B(1)	B1	+12 VOLTS
A2	+12 VOLTS	B2	+12 VOLTS
A3	+12 VOLTS	B3	+12 VOLTS
A4	GND	B4	GND
A5	JTAG_TCK(2)	B5	SMCLK(2)
A6	JTAG_TDI(2)	B6	SMDAT(2)
A7	JTAG_TDO(2)	B7	GND
A8	JTAG_TMS(2)	B8	+3.3 VOLTS
A9	+3.3 VOLTS	B9	JTAG_TRST_B(2)
A10	+3.3 VOLTS	B10	+3.3 VOLTSAUX(2)
A11	PCIE_PERST(6)	B11	PCIE_WAKE_B(2)
	KEY		KEY
A12	GND	B12	RESERVED
A13	PCIE_REFCLKP(3)	B13	GND
A14	PCIE_REFCLKN(3)	B14	PETP0(4)
A15	GND	B15	PETN0(4)
A16	PERP0(5)	B16	GND
A17	PERN0(5)	B17	PCIE_PRSNT2_B(1)
A18	GND	B18	GND
A19	RESERVED	B19	PETP1
A20	GND	B20	PETN1
A21	PERP1	B21	GND
A22	PERN1	B22	GND
A23	GND	B23	PETP2
A24	GND	B24	PETN2
A25	PERP2	B25	GND
A26	PERN2	B26	GND
A27	GND	B27	PETP3
A28	GND	B28	PETN3
A29	PERP3	B29	GND

Table 3-1: **P13 Edge Connector Socket Pinout for PCI Express Designs *(Continued)***

P13 A Side	Signal	P13 B Side	Signal
A30	PERN3	B30	RESERVED
A31	GND	B31	PCIE_PRSNT2_B(1)
A32	RESERVED	B32	GND
A33	RESERVED	B33	PETP4
A34	GND	B34	PETN4
A35	PERP4	B35	GND
A36	PERN4	B36	GND
A37	GND	B37	PETP5
A38	GND	B38	PETN5
A39	PERP5	B39	GND
A40	PERN5	B40	GND
A41	GND	B41	PETP6
A42	GND	B42	PETN6
A43	PERP6	B43	GND
A44	PERN6	B44	GND
A45	GND	B45	PETP7
A46	GND	B46	PETN7
A47	PERP7	B47	GND
A48	PERN7	B48	PCIE_PRSNT2_B(1)
A49	GND	B49	GND

Notes:

1. PCIE_PRSNT1_B can be connected to one of three PCIE_PRSNT2_B signals by connecting a shunt on connector P45. See Table 3-2 for application information.
2. No connect on the ML555 board.
3. The ML555 board layout provides two methods of interfacing the PCIE_REFCLK to the FPGA. The default method is to AC couple the 100 MHz PCIE_REFCLK directly to the GTP_DUAL tile X0Y2 MGTREFCLK input pins. An alternative method is to remove two 0Ω resistors and install an ICS874003-02 PCI Express Jitter attenuator module, which provides a 100, 125, or 250 MHz reference clock to the GTP transceiver. The jitter attentuator has two LVDS outputs that connect to the GTP and FPGA global clock inputs. One of the jitter attentuator LVDS outputs is connected to the MGTREFCLK inputs of GTP_DUAL tile X0Y2 for PCI Express lanes 0 and 1. The PCIE_REFCLK is also connected to the FPGA global clock network on pins J16 and J17. Internal FPGA clock buffers distribute this clock to other GTP_DUAL tiles for PCI Express operation. The architecture of the FPGA permits an external MGTREFCLK to be driven a maximum of three GTP_DUAL tiles up or down. See "Serial Bus Clocking with Optional ICS874003-02 Clock Jitter Attenuator (PCI Express Operation)," page 60 for additional information.
4. The PETPX and PETNX pins connect to the PCI Express transmitter differential pair on the system board and the PCI Express receiver on the add-in card.
5. The PERPX and PERNX pins connect to the PCI Express receiver differential pair on the system board and the PCI Express transmitter on the add-in card.
6. PCIE_PERST connects to FPGA pin AE14.

The PCI Express Card Electromechanical Specification requires add-in cards to implement variable-length edge finger pads and tie PRSNT1_B and PRSNT2_B signals together on the