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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Virtex-5 FPGA ML561 Memory Interfaces Development Board

User Guide

UG199 (v1.2.1) June 15, 2009

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
02/12/07	1.0	Initial Xilinx release.
08/09/07	1.1	Revised Read and Write Strobe in Table 5-4, page 49. Added Chapter 7, “ML561 Hardware-Simulation Correlation.”
04/19/08	1.2	Revised Figure 3-11, page 37 and Table 3-19, page 38. Corrected FPGA driver for Read Data and Read Strobe in Table 5-4, page 49. Updated Data and Strobe entries in Table 5-5, page 49. Updated manufacturers and links in Appendix B, “Bill of Materials.”
06/15/09	1.2.1	Clarified VIH(max) voltage in “Terminology.”

Table of Contents

Appendix B: Bill of Materials

Appendix C: LCD Interface

About This Guide

This user guide describes the Virtex®-5 FPGA ML561 Memory Interfaces Development Board. Complete and up-to-date documentation of the Virtex-5 family of FPGAs is available on the Xilinx website at http://www.xilinx.com/virtex5.

Guide Contents

This manual contains the following chapters:

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- Virtex-5 FPGA User Guide

  Chapters in this guide cover the following topics:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM

  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources
  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources
- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platforms.
- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.
- Virtex-5 FPGA Embedded Processor Block for PowerPC® 440 Designs

  This reference guide is a description of the embedded processor block available in the Virtex-5 FXT platform.
- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.
- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.
- Virtex-5 FPGA XtremeDSP Design Considerations User Guide

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E.
- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.
- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.
- Virtex-5 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-5 Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Documentation" for details. Refer to "Clock Management Technology (CMT)" in Chapter 2 for details.
Red text	Cross-reference link to a location in another document	See Figure 5 in the *Virtex-5 FPGA Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

Terminology

This section defines terms used in Chapter 7, "ML561 Hardware-Simulation Correlation," of this document.

Data Valid Window (DVW)

DVW is the data valid window opening measured by the VIH and VIL masks. The smaller of the two values are listed as absolute time as well as in terms of the percentage of UI (Unit Interval), or bit time.

Extrapolation

The ultimate goal of a design is to ascertain quality of signal at the receiver I/O Buffer (IOB). This measurement can only be simulated. When the hardware measurements are correlated with the simulation at the probe point, the extra probe capacitance is removed from the IBIS schematics, and the simulation is repeated at two extreme corners (slow-weak and fast-strong). Removal of probe capacitance is important to represent the actual hardware. If the SI characteristics of these simulations are proved to be within the acceptable range with sufficient margin, then the performance requirements for data signal interface of the corresponding memory operation at the target clock frequency are proved to have been met.

Hardware Measurements

These measurements are the actual real-time measurements of an eye diagram and a segment of the test pattern (PRBS6) waveform captured on ML561 hardware at the designated probe point using an Agilent scope.

Inter-Symbol Interference (ISI)

As the frequency of operation increases, the signal delay is affected by the data pattern that precedes the current data bit. This is called the inter-symbol interference (ISI) effect. All testing is performed with a pseudo-random bitstream (PRBS) of order 6, that is, PRBS6. ISI is the jitter represented by the eye at all four voltage thresholds. The worst of the following two sum values are listed in this table:

- Sum of ISI at VIH(ac)-min and VIH(dc)-min
- Sum of ISI at VIL(ac)-max and VIL(dc)-max

Noise Margin

This is the noise margin available at the receiver. Measurements are taken at the AC voltage levels as the minimum vertical opening of the eye in the vicinity of the center of the bit period. Ideally, the input voltage needs to remain above the DC voltage specifications. However, by considering the AC voltage specifications for the nominal voltage level for VREF, these measurements are more conservative values that also include the effects of VREF variations.

- VIH margin: Difference between the top of the eye opening and VIH(ac)-min
- VIL margin: Difference between VIL(ac)-max and the bottom of the eye opening

These measurements are performed in stand-alone fashion for the signal under test. Thus no consideration of crosstalk or Simultaneously Switching Output (SSO) effects are accounted for.

Overshoot / Undershoot Margin

Overshoot margin is the difference between the maximum allowable VIH per JEDEC specification and the maximum amplitude of the measured eye. Similarly, undershoot margin is the difference between the minimum amplitude of the measured eye and the minimum allowable VIL value per JEDEC specification. For both SSTL18 and 1.8V HSTL specifications:

- VIH(max) < (VDDQ + 300 mV) = (1.8 + 0.3)V = 2.1V
- VIL(min) > -300 mV = 0.3V

Note: VIH(max) must not exceed 1.9V for all Micron Parts.

Simulation Correlation

The BoardSim utility of the HyperLynx simulator is used to extract the IBIS schematics of the same signal net for which hardware measurements are made. To replicate the hardware measurement probe set up at the probe point, a 0.5 pF probe capacitance is added based on Agilent probe loading specifications to the extracted IBIS schematics of the memory signal. For the FPGA devices soldered on the ML561 board under test, the process corner (slow, typical, or fast) is not known. Thus simulation is performed for all three corners (slow-weak, typical, and fast-strong), and the results of the case that best fits with hardware measurement is selected for tabulation.

VIH(ac)-min

This term is the minimum input level at which the receiver must recognize input logic High.

VIH(dc)-min

When the input signal reaches VIH(ac)-min, the receiver continues to interpret the input as a logic High as long as the signal remains above this voltage. (This parameter is basically the hysteresis for a logic ‘1’.)

VIL(ac)-max

This term is the maximum input level at which the receiver must recognize input logic Low.

VIL(dc)-max

When the input signal reaches VIL(ac)-max, the receiver continues to interpret the input as a logic Low as long as the signal remains below this voltage. (This parameter is basically the hysteresis for logic ‘0’.)

Chapter 1

Introduction

This chapter introduces the Virtex®-5 FPGA ML561 reference design. It contains the following sections:

- "About the Virtex-5 FPGA ML561 Memory Interfaces Tool Kit"
- "Virtex-5 FPGA ML561 Memory Interfaces Development Board"

About the Virtex-5 FPGA ML561 Memory Interfaces Tool Kit

The Virtex-5 FPGA ML561 Memory Interfaces Tool Kit provides a complete development platform to interface with external memory devices for designing and verifying applications based on the Virtex-5 LXT FPGA platform. This kit allows designers to implement high-speed applications with extreme flexibility using IP cores and customized modules. The Virtex-5 LXT FPGA, with its column-based architecture, makes it possible to develop highly flexible memory interface applications.

The Virtex-5 FPGA ML561 Memory Interfaces Tool Kit includes the following:

- Virtex-5 FPGA ML561 Memory Interfaces Development Board (XC5VLX50T-FFG1136 FPGA)
- 5V/6.5 A DC power supply
- Country-specific power supply line cord
- RS-232 serial cable, DB9-F to DB9-F
- Documentation and reference design CD-ROM

Optional items that also support development efforts include:

- Xilinx® ISE® software
- JTAG cable
- Xilinx Parallel IV cable

For assistance with any of these items, contact your local Xilinx distributor or visit the Xilinx online store at www.xilinx.com.

The heart of the Virtex-5 FPGA ML561 Memory Interfaces Tool Kit is the Virtex-5 FPGA ML561 Development Board. This manual provides comprehensive information on Rev A3 and later revisions of this board.

Virtex-5 FPGA ML561 Memory Interfaces Development Board

A high-level functional block diagram of the Virtex-5 FPGA ML561 Memory Interfaces Development Board is shown in Figure 1-1.

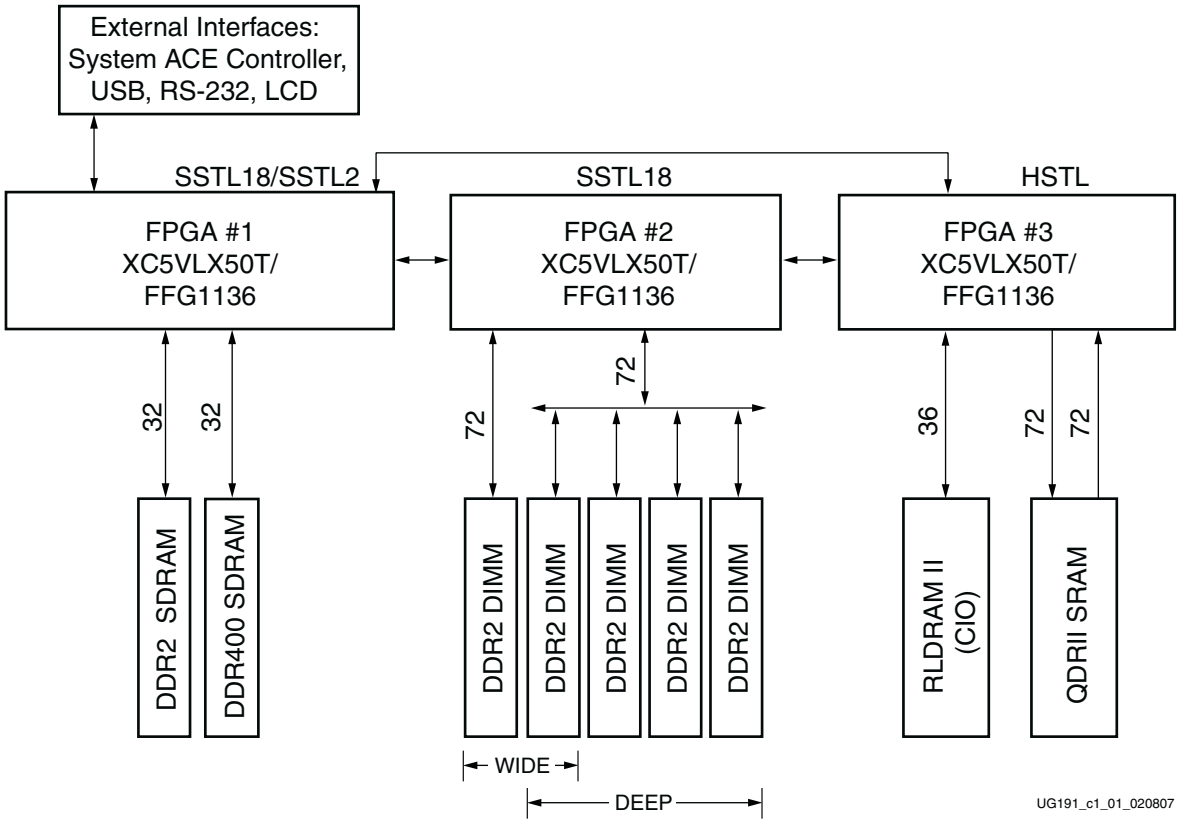

Figure 1-1: **Virtex-5 FPGA ML561 Development Board Block Diagram**

The Virtex-5 FPGA ML561 Development Board includes the following major functional blocks:

- Three XC5VLX50T-FFG1136 FPGAs (see DS100, *Virtex-5 Family Overview*)
- DDR400 components: 128 MB (32M x 32 bits) at 200 MHz clock speed. See XAPP851, *DDR SDRAM Controller Using Virtex-5 FPGA Devices*.
- DDR2 DIMM: Five PC2-5300 DIMM sockets for up to 2 GB (128M x 144 bits). See XAPP858, *High-Performance DDR2 SDRAM Interface in Virtex-5 Devices*.
- DDR2-667 components: 64 MB (16M x 32 bits) at 333 MHz clock speed
- QDRII memory: 16 MB (2M x 72 bits) at up to 300 MHz clock speed. See XAPP853, *QDR II SRAM Interface for Virtex-5 Devices*.
- RLDRAM II memory: 64 MB (16M x 36 bits) at up to 300 MHz clock speed. See XAPP852, *RLDRAM II Memory Interface for Virtex-5 FPGAs*.
- One DB9-M RS-232 port and one USB 2.0 port
- A System ACE™ CompactFlash (CF) Configuration Controller that allows storing and downloading of up to eight FPGA configuration image files
- On-board power regulators with ±5% output margin test capabilities

Figure 1-2 shows the Virtex-5 FPGA ML561 Development Board and indicates the locations of the resident memory devices.

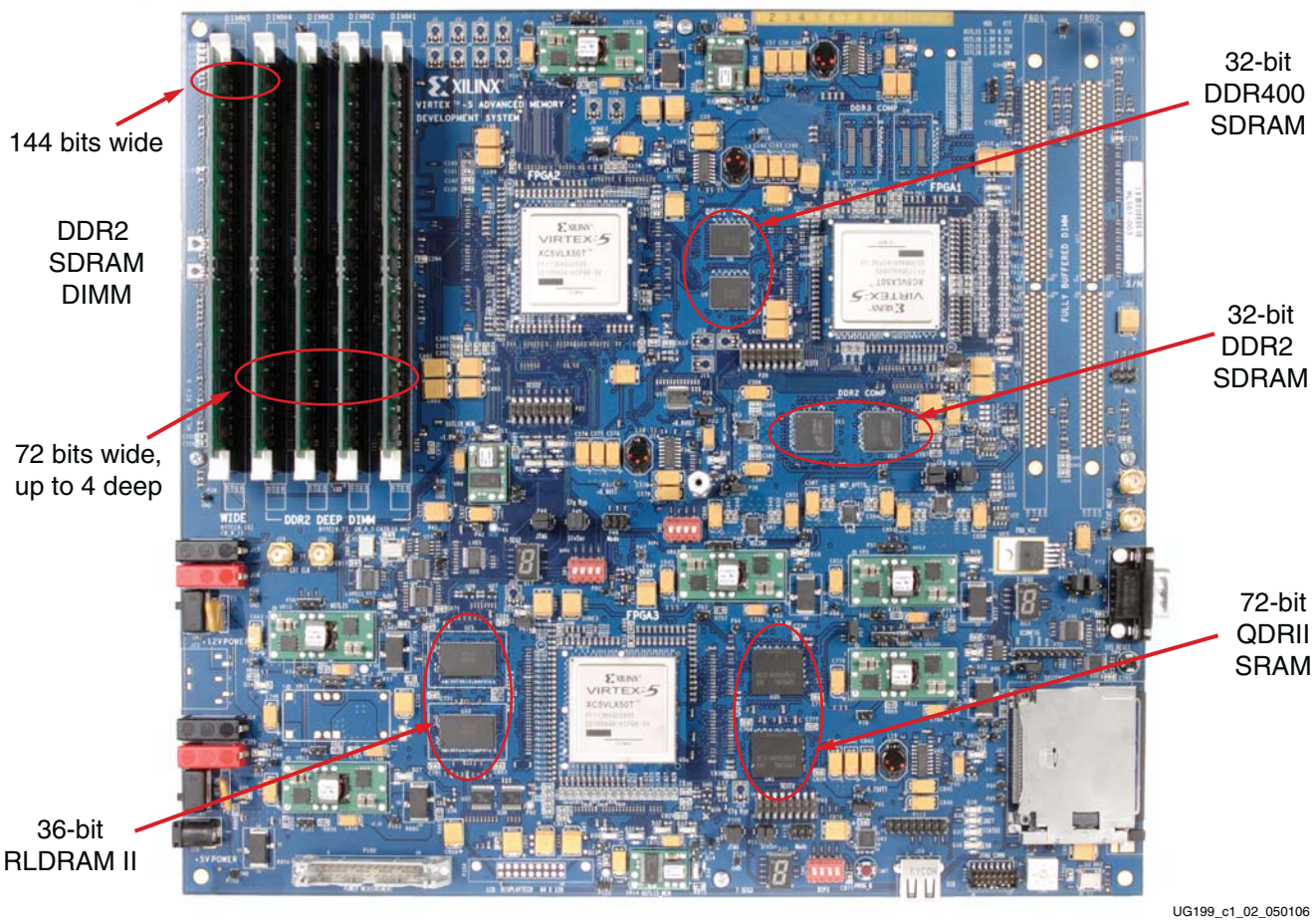

Figure 1-2: **Virtex-5 FPGA ML561 Development Board**

Chapter 2

Getting Started

This chapter describes the items needed to configure the Virtex-5 FPGA ML561 Memory Interfaces Development Board. The Virtex-5 FPGA ML561 Development Board is tested at the factory after assembly and should be received in working condition. It is set up to load a bitstream from the CompactFlash card at socket J27 through the System ACE controller (U45).

This chapter contains the following sections:

- "Documentation and Reference Design CD"
- "Initial Board Check Before Applying Power"
- "Applying Power to the Board"

Documentation and Reference Design CD

The CD included in the Virtex-5 FPGA ML561 Memory Interfaces Tool Kit contains the design files for the Virtex-5 FPGA ML561 Development Board, including schematics, board layout, and reference design files. Open the `ReadMe.rtf` file on the CD to review the list of contents.

Initial Board Check Before Applying Power

Perform these steps before applying board power:

1. Set up the Configuration Mode jumpers (P27, P46, and P112) for JTAG configuration.

   See "Configuration Modes" on page 51 for all available modes for the Virtex-5 FPGA ML561 Development Board.

2. Confirm that the JTAG chain jumpers P38, P44, and P109 are connecting pins 1 to 2 and pins 3 to 4. This way, all three devices are in the chain. Otherwise, the ISE iMPACT software will not find all three devices to configure. For more information see "JTAG Chain" on page 52.
3. Make sure that no inhibit jumpers are present on any of the power supply regulator modules. For more information, see "Voltage Regulators" on page 34.
4. The Virtex-5 FPGA ML561 Development Board has a 200 MHz on-board oscillator, which provides a copy of a differential LVPECL clock to each of the three FPGAs through a differential clock buffer (ICS853006). There is also a connection to a pair of SMA connectors (J19, J20) to provide a differential LVDS clock from an off-board signal generator. Another differential clock buffer (ICS853006) provides a copy of this clock to each of the three FPGAs. These clocks are available after configuration for the design to use for various system clocks.

5. Insert the CompactFlash card included in the kit into socket J27 on the Virtex-5 FPGA ML561 Development Board. To select the startup file, check that SW8 is set to position 0.

Applying Power to the Board

The Virtex-5 FPGA ML561 Development Board is now ready to power on. The Virtex-5 FPGA ML561 Development Board is shipped with a country-specific AC line cord for the universal input 5V desktop power supply. Follow these steps to power up the Virtex-5 FPGA ML561 Development Board:

1. Confirm that the ON-OFF switch, SW5, is in the OFF position.
2. Plug the 5V desktop power supply into the 5V DC input barrel jack J28 on the Virtex-5 FPGA ML561 Development Board. Plug the desktop power supply AC line cord into an electrical outlet supplying the appropriate voltage.
3. Turn SW5 to the ON position. The power indicators for all regulator modules should come on, indicating output from the regulators. The System ACE status LED D37 comes on when the System ACE controller (U45) extracts the BIT configuration file from the CompactFlash card to the FPGA. If no CompactFlash card is installed in the card socket J27 on the Virtex-5 FPGA ML561 Development Board, the red System ACE error LED D38 flashes.
4. If a CompactFlash card is not installed in socket J27, a JTAG cable must be used to configure the FPGAs. To use a Parallel IV cable or other JTAG pod, download the FPGA configuration bitstream into each FPGA. After the DONE LED (D28) comes on, the FPGAs are configured and ready to use.
5. Push the reset button SW4.

Chapter 3

Hardware Description

This chapter describes the major hardware blocks on the Virtex-5 FPGA ML561 Development Board and provides useful design consideration. It contains the following sections:

- "Hardware Overview"
- "Memory Details"
- "External Interfaces"
- "Power Regulation"
- "Board Design Considerations"

Hardware Overview

The ML561 Development/Evaluation system reference design is implemented with three XC5VLX50T-FFG1136 devices from the Virtex-5 FPGA family to demonstrate high-speed external memory application interfaces. The memory technologies supported by the Virtex-5 FPGA ML561 Development Board are DDR2 SDRAM, DDR400 SDRAM, QDRII SRAM, and RLDRAM II SDRAM.

Figure 3-1 provides a view of all the major components on ML561 board. It shows the placement of the three Virtex-5 FPGAs, and the position of the associated major interfaces for each FPGA.

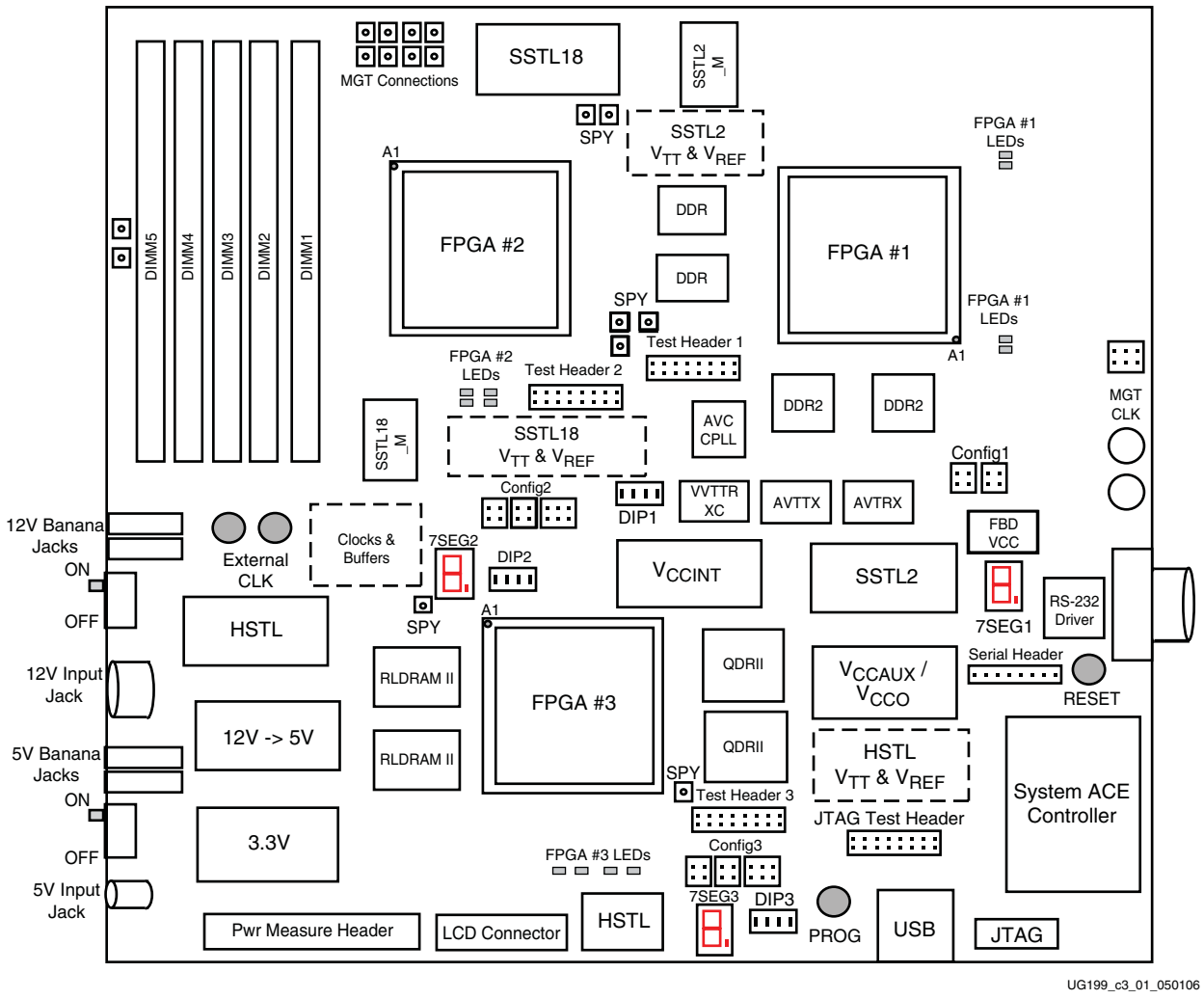

Figure 3-1: **ML561 XC5VLX50T-FFG1136 Board Placement Diagram**

FPGA

The ML561 uses three Virtex-5 XC5VLX50T-FFG1136 devices, each in a 1136-pin, 35 mm x 35 mm BGA package. Figure 1-1, page 12 shows the memory devices associated with the three FPGAs. Refer to Appendix A, "FPGA Pinouts," for a complete pinout of all Virtex-5 devices on the board. Refer to Appendix B, "Bill of Materials," for a list of major components on the Virtex-5 FPGA ML561 Development Board, including their reference designators and links to their corresponding data sheets.

Memories

Table 3-1 lists the types of memories that the ML561 board supports.

Table 3-1: **Summary of ML561 Memory Interfaces**

Memory Type	Maximum Speed	Data Rate	Data Width	I/O Standard	Data/Strobe Ratios
DDR400 SDRAM	200 MHz	400 Mbps	32	SSTL2	8:1
DDR2 DIMM	333 MHz	667 Mbps	144	SSTL18	8:1
DDR2 SDRAM	333 MHz	667 Mbps	32	SSTL18	8:1
QDRII SRAM	300 MHz	1.2 Gbps	72	HSTL18	18:1, 36:1
RLDRAM II	300 MHz	600 Mbps	36	HSTL18	9:1, 18:1

When a larger data/strobe ratio is implemented, for example, a x36 QDRII device, the smaller configurations can also be demonstrated by programming the FPGA for a smaller data width, such as a 9:1 data/strobe ratio for the QDRII device.

DDR400 SDRAM Components

The Virtex-5 FPGA ML561 Development Board has two 200 MHz Micron MT46V32M16BN-5B (16-bit) DDR400 SDRAM components that provide a 32-bit interface. Each 16-bit device is packaged in a 60-ball FBGA package, with a common address and control bus and separate clocks and DQS/DQ signals.

DDR2 DIMM

The Virtex-5 FPGA ML561 Development Board contains five PC-5300 240-pin DIMM sockets for a maximum data width of 144 bits or a maximum depth of four DIMMs. The sockets are arranged in a row leading away from the FPGA so they can share common address and control signals. DIMM1 through DIMM4 share DQ/DQS signals to form a deep 72-bit memory interface, while DIMM5 has separate DQ/DQS signals.

For the deep DDR2 interface, the sockets are to be populated starting at socket DIMM4. Table 3-2 illustrates how the sockets should be populated based on the interface wanted.

Table 3-2: **Populating DDR2 DIMM Sockets**

DIMM Interface	DIMM Sockets Populated	Interface Width
One Deep	5 or 4	72-bit
Two Deep	4 and 3	72-bit
Three Deep	4, 3, and 2	72-bit
Four Deep	4, 3, 2, and 1	72-bit
Two Wide	5 and 4	144-bit

Populating the DIMMs in this order is necessary due to the placement of the termination on the signals being shared. More detail on termination is given in "Board Design Considerations," page 36.

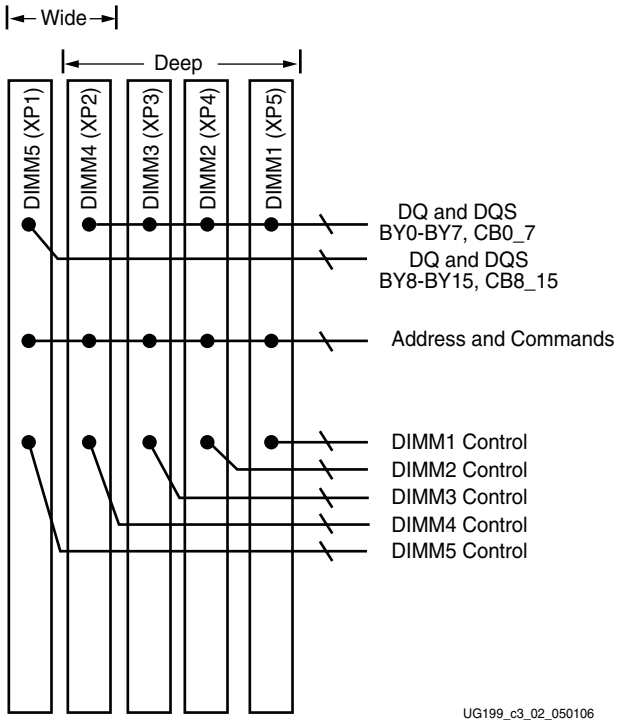

Figure 3-2: **DDR2 Deep and Wide DIMM Sockets**

DDR2 SDRAM Components

The ML561 board contains two 333 MHz Micron MT47H32M16CC-3 (16-bit) DDR2 SDRAM components that provide a 32-bit interface to FPGA #1. Each 16-bit device is packaged in an 84-ball FBGA package, with a common address and control bus and separate clocks and DQS/DQ signals.

QDRII SRAM

The ML561 board contains a 300 MHz QDRII SRAM interface with a 72-bit Read interface and a 72-bit Write interface using two Samsung K7R643684M-FC30 components (x36). They are packaged in a 165-ball FBGA package with a body size of 15 x 17 mm. These two components share the same address/control signals but have separate clock and data signals.

RLDRAM II Devices

The ML561 contains a 300 MHz 36-bit RLDRAM II interface using two Micron MT49H16M18BM-25 devices (x18) packaged in a 144-ball PBGA package. They share a common address and control bus but have separate clocks and DQS/DQ signals.

Memory Details

DDR400 and DDR2 Component Memories

The FPGA #1 device on the Virtex-5 FPGA ML561 Development Board is connected to DDR and DDR2 component memories, as shown in Figure 3-3.

Figure 3-3 summarizes the distribution of DDR and DDR2 discrete component interface signals among the different banks of the FPGA #1 device.

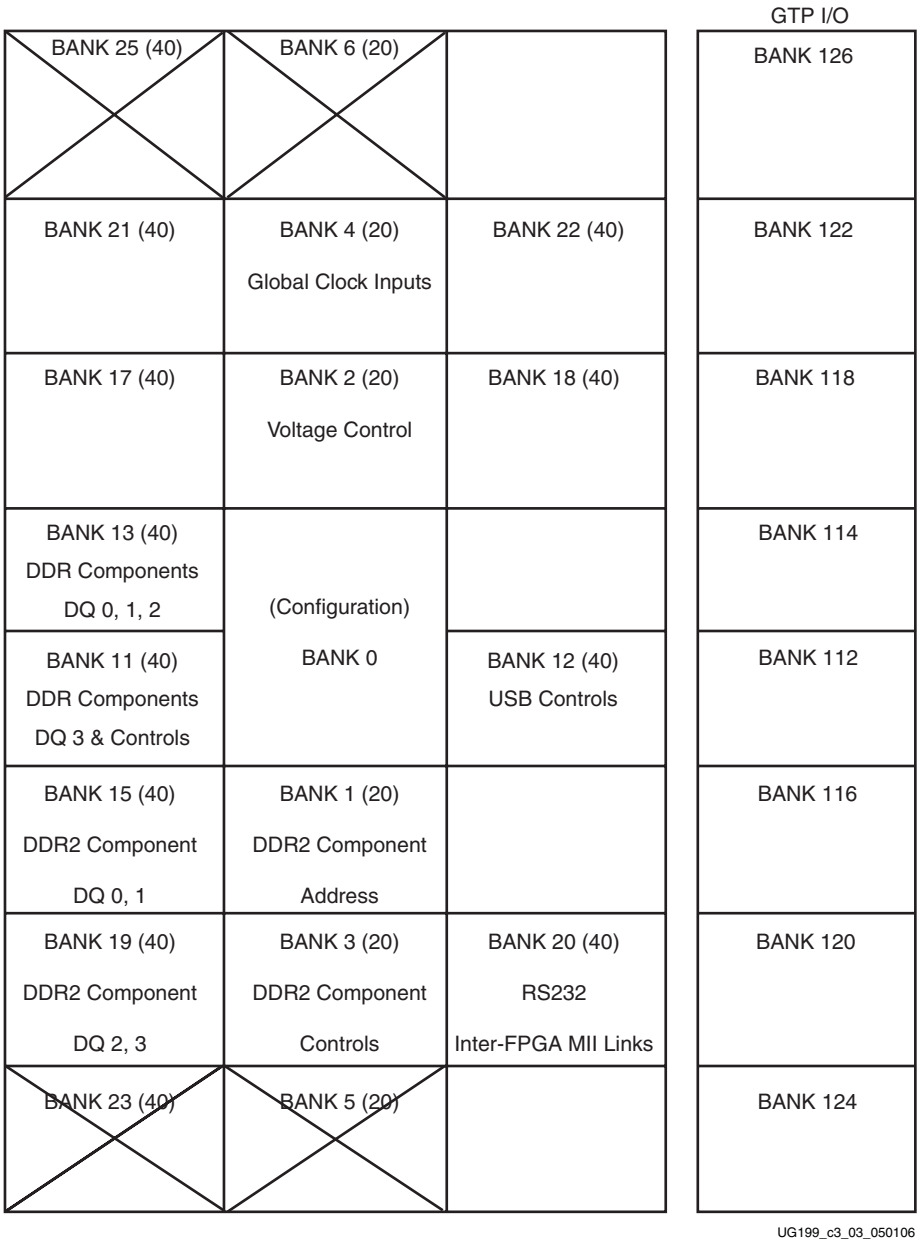

Figure 3-3: **FPGA #1 Banks for DDR400 and DDR2 Component (Top View)**

Table 3-3 describes all signals associated with DDR400 Component memories.

Table 3-3: **DDR400 Component Signal Summary**

Board Signal Name(s)	Bits	Description
DDR1_A[13:0]	14	DDR400 Component Address
DDR1_CK[2:1]_[P,N]	4	DDR400 Component Differential Clock
DDR1_[RAS,CAS,WE]_N, DDR1_CKE, DDR1_BA[1:0], DDR1_BY[0_1,2_3]_CS_N, DDR1_DM_BY[3:0]	12	DDR400 Component Control Signals
DDR1_DQ_BY0_B[7:0], DDR1_DQS_BY0_P	9	DDR400 Data and Strobe: Byte 0
DDR1_DQ_BY1_B[7:0], DDR1_DQS_BY1_P	9	DDR400 Data and Strobe: Byte 1
DDR1_DQ_BY2_B[7:0], DDR1_DQS_BY2_P	9	DDR400 Data and Strobe: Byte 2
DDR1_DQ_BY3_B[7:0], DDR1_DQS_BY3_P	9	DDR400 Data and Strobe: Byte 3

Notes:

1. DDR1_CKE signal has a weak 4.7KΩ pull-down resistor to meet the memory power-up requirements.

Table 3-4 describes all signals associated with DDR2 Component memories. For a complete list of FPGA #1 signals and their pin locations, refer to Appendix A, "FPGA Pinouts."

Table 3-4: **DDR2 Component Signal Summary**

Board Signal Name(s)	Bits	Description
DDR2_A[12:0]	13	DDR2 Component Address
DDR2_CK[1:0]_[P,N]	4	DDR2 Component Differential Clock
DDR2_ODT[1:0], DDR2_[RAS,CAS,WE]_N, DDR2_CKE, DDR2_BA[1:0], DDR2_CS[1:0]_N, DDR2_DM_BY[3:0]	14	DDR2 Component Control Signals
DDR2_DQ_BY0_B[7:0], DDR2_DQS_BY0_[P,N]	10	DDR2 Data and Strobe: Byte 0
DDR2_DQ_BY1_B[7:0], DDR2_DQS_BY1_[P,N]	10	DDR2 Data and Strobe: Byte 1
DDR2_DQ_BY2_B[7:0], DDR2_DQS_BY2_[P,N]	10	DDR2 Data and Strobe: Byte 2
DDR2_DQ_BY3_B[7:0], DDR2_DQS_BY3_[P,N]	10	DDR2 Data and Strobe: Byte 3

Notes:

1. DDR2_CKE and DDR2_ODT[1:0] signals have a weak 4.7KΩ pull-down resistor to meet the memory power-up requirements.

XAPP851, *DDR SDRAM Controller Using Virtex-5 FPGA Devices*, XAPP858, *High-Performance DDR2 SDRAM Interface in Virtex-5 Devices*, and the corresponding demos are included on the CD shipped with the ML561 Tool Kit. For a complete list of FPGA #1 signals and their pin locations, refer to Appendix A, "FPGA Pinouts."

DDR2 SDRAM DIMM

The FPGA #2 device on the Virtex-5 FPGA ML561 Development Board is connected to DDR2 memories. The DDR2 memory interface includes a 144-bit wide DIMM connection to up to five 240-pin DDR2 DIMM sockets.

For the 144-bit wide DIMM datapath, the data bytes are spread across multiple banks of the FPGA #2 device. Figure 3-4 summarizes the distribution of DDR2 DIMM interface signals among the different banks of the FPGA #2 device.

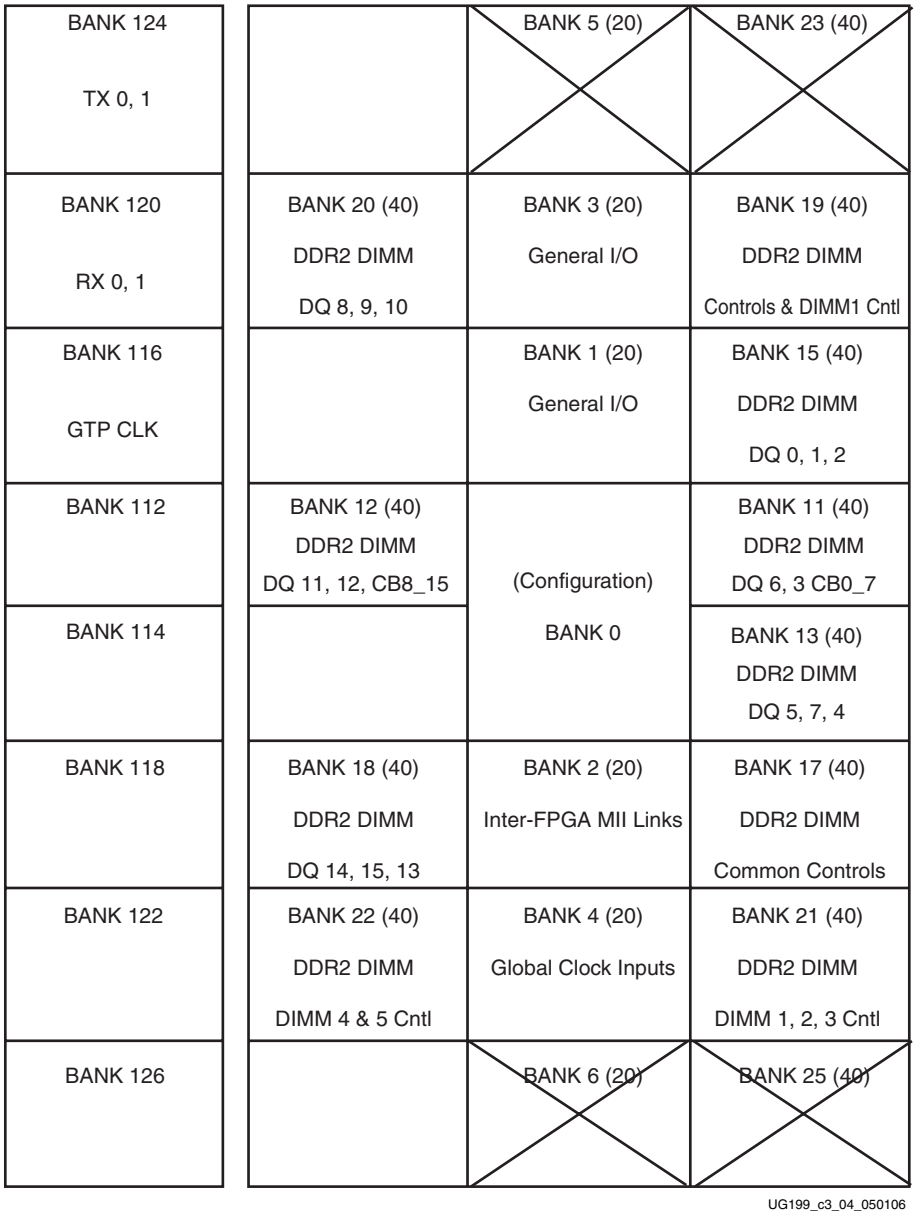

Figure 3-4: **FPGA #2 Banks for DDR2 DIMM (SSTL18) Interfaces (Top View)**

Table 3-5 describes all the signals associated with DDR2 DIMM component memories. For the Deep DIMM interface to four DIMMs, the individual dedicated control signals are listed at the bottom of Table 3-5.

Table 3-5: **DDR2 DIMM Signal Summary**

Board Signal Name(s)	Bits	Description
DDR2_DIMM_A[15:0]	16	DDR2 DIMM Address
DDR2_DIMM[5:1]_CK[2:0]_[P,N]	30	DDR2 DIMM Differential Clocks: Three copies per DIMM
DDR2_DIMM_[RAS,CAS,WE,RESET]_N, DDR2_DIMM[5:1]_CKE[1:0], DDR2_DIMM_BA[2:0], DDR2_DIMM[5:1]_CS[1:0]_N, DDR2_DIMM[5:1]_ODT[1:0]	37	DDR2 DIMM Common Control Signals
DDR2_DIMM[1:5]_CS[1:0]_N, DDR2_DIMM[1:5]_CKE[1:0], DDR2_DIMM[1:5]_ODT[1:0]	20	DDR2 DIMM Dedicated Control Signals
DDR2_DIMM_LB_BK[11,13,15]_[IN,OUT]	6	Deep DIMMs (DIMM1 through DIMM4) Loopback Signals
DDR2_DIMM_LB_BK[12,18,20]	3	Wide DIMM (DIMM5) Loopback Signals (Total of six FPGA pins)
DDR2_DIMM[1:5]_CNTL_PAR, DDR2_DIMM[1:5]_CNTL_PAR_ERR, DDR2_DIMM[1:5]_NC_019, DDR2_DIMM[1:5]_NC_102	20	Miscellaneous Place Holder Signals to the Five DIMMs
DDR2_DIMM_DQ_BY[0:15]_B[7:0], DDR2_DIMM_DQS_BY[0:15]_L_[P,N], DDR2_DIMM_DM_BY[0:15]	176	DDR2 DIMM Data, Strobes, and Data Mask: Bytes 0 through 15
DDR2_DIMM_DQ_CB0_7_B[7:0], DDR2_DIMM_DQS_CB0_7_L_[P,N], DDR2_DIMM_DM_CB0_7	11	DDR2 DIMM Data, Strobes, and Data Mask: Check Byte 0
DDR2_DIMM_DQ_CB8_15_B[7:0], DDR2_DIMM_DQS_CB8_15_L_[P,N], DDR2_DIMM_DM_CB8_15	11	DDR2 DIMM Data, Strobes, and Data Mask: Check Byte 1
DDR2_DIMM[1:5]_SA[2:0]	15	Serial PROM Address
DDR2_DIMM_[SCL,SDA]"	2	Serial PROM interface CLK and Data

Notes:

1. DDR2_DIMM_CKE and DDR2_DIMM_ODT signals are connected to a 4.7KΩ pull-down resistor to meet the memory power-up requirements.

XAPP858, *High-Performance DDR2 SDRAM Interface in Virtex-5 Devices* and its corresponding demo are included on the CD shipped with the ML561 Tool Kit.

QDRII and RLDRAM II Memories

Figure 3-5 summarizes the distribution of QDRII and RLDRAM II component interface signals among the different banks of the FPGA #3 device.

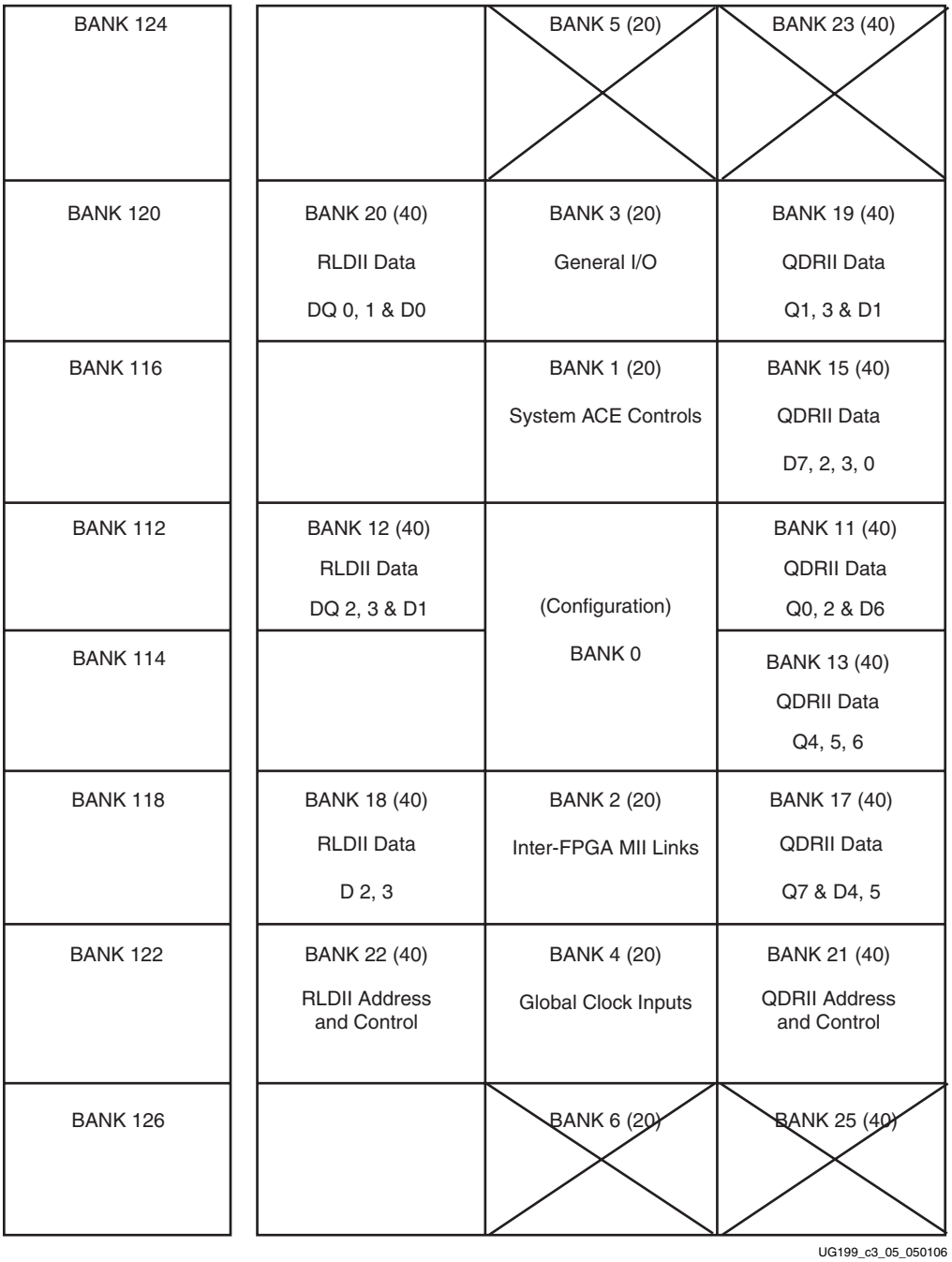

Figure 3-5: **FPGA #3 Banks for QDRII SRAM and RLDRAM II Interfaces (Top View)**