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Video Input/Output Daughter Card

User Guide

UG235 (v1.2.1) October 31, 2007

XILINX®

Revision History

Video Input/Output Daughter Card
UG235 (v1.2.1) October 31, 2007

The following table shows the revision history for this document.

	Version	Revision
01/25/06	1.0	Initial Xilinx release.
02/13/06	1.1	Added two sentences to pages 17 and 43.
02/23/07	1.2	Corrected 3 pins and column 6 heading in Table A-2.
10/31/07	1.2.1	Defined the following acronyms on p. 48: EAV, CRC, NTSC, and PAL.

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Appendix B: VSK I/O Connector Location Pictures

About This Guide

This guide describes the Video Input and Output Daughter Card (VIODC), a standard video interface card that is compatible with the Xilinx ML401, ML402, and ML403 development platforms.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "VIODC Overview" – provides an overview of the VIODC, interfaces, and I/Os.
- Chapter 2, "VIODC to ML402 Card Interface" – describes the VIODC to ML402 card interface.
- Chapter 3, "Component and S-Video Interfaces" – describes the High Definition (HD) and Standard Definition (SD) component video and S-video interfaces.
- Chapter 4, "DVI/VGA Input Interface" – provides an overview of the VGA and DVI input interface.
- Chapter 5, "DVI/VGA Output Interface"– provides an overview of the VGA and DVI output interface.
- Chapter 6, "SDI Interface"– provides an overview of the SDI video interface.
- Chapter 7, "Image Sensor Camera Interface"– describes the Irvine Sensors LVDS RGB camera interface.
- Chapter 8, "Attaching the VIODC to the ML40x Development Board" – provides information necessary for proper attachment of the VIODC to a ML40*x* development board.
- Appendix A, "Reference Information"– contains VIODC pinout information.
- Appendix B, "VSK I/O Connector Location Pictures" – shows I/O connection locations.

Additional Resources

To find additional documentation, see the Xilinx website at:

http://www.xilinx.com/literature/index.htm.

To search the Answer Database of silicon, software, and IP questions and answers, or to create a technical support Web Case, see the Xilinx website at:

http://www.xilinx.com/support.

Conventions

This document uses the following conventions. An example illustrates each convention.

Typographical

The following typographical conventions are used in this document:

Convention	Meaning or Use	Example
`Courier font`	Messages, prompts, and program files that the system displays	`speed grade: - 100`
`Courier bold`	Literal commands that you enter in a syntactical statement	**`ngdbuild`** *design_name*
Helvetica bold	Commands that you select from a menu	**File → Open**
	Keyboard shortcuts	**Ctrl+C**
Italic font	Variables in a syntax statement for which you must supply values	**`ngdbuild`** *design_name*
	References to other manuals	See the *Development System Reference Guide* for more information.
	Emphasis in text	If a wire is drawn so that it overlaps the pin of a symbol, the two nets are *not* connected.
Square brackets [ ]	An optional entry or parameter. However, in bus specifications, such as **`bus[7:0]`**, they are required.	**`ngdbuild`** [*`option_name`*] *`design_name`*
Braces { }	A list of items from which you must choose one or more	**`lowpwr =`**{**`on`**|**`off`**}
Vertical bar |	Separates items in a list of choices	**`lowpwr =`**{**`on`**|**`off`**}

Vertical ellipsis
.
.
.
	Repetitive material that has been omitted	`IOB #1: Name = QOUT'`
		`IOB #2: Name = CLKIN'`
		.
		.
		.

Horizontal ellipsis ...	Repetitive material that has been omitted	**`allow block`** *block_name loc1 loc2 ... locn;*

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Resources" for details. Refer to "Title Formats" in Chapter 1 for details.
Red text	Cross-reference link to a location in another document	See Figure 2-5 in the *Handbook.*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest speed files.

Chapter 1

VIODC Overview

Introduction

The Video Input and Output Daughter Card (VIODC) is a standard video interface card for Xilinx development platforms. It is compatible with ML401, ML402, and ML403 boards and other future Xilinx development platforms. The VIODC is shown in Figure 1-1 mounted on a ML402 platform. The VIODC provides access to high definition (HD) and standard definition (SD) video streams, as well as computer graphics video interfaces, such as VGA over DVI and SDI interfaces.

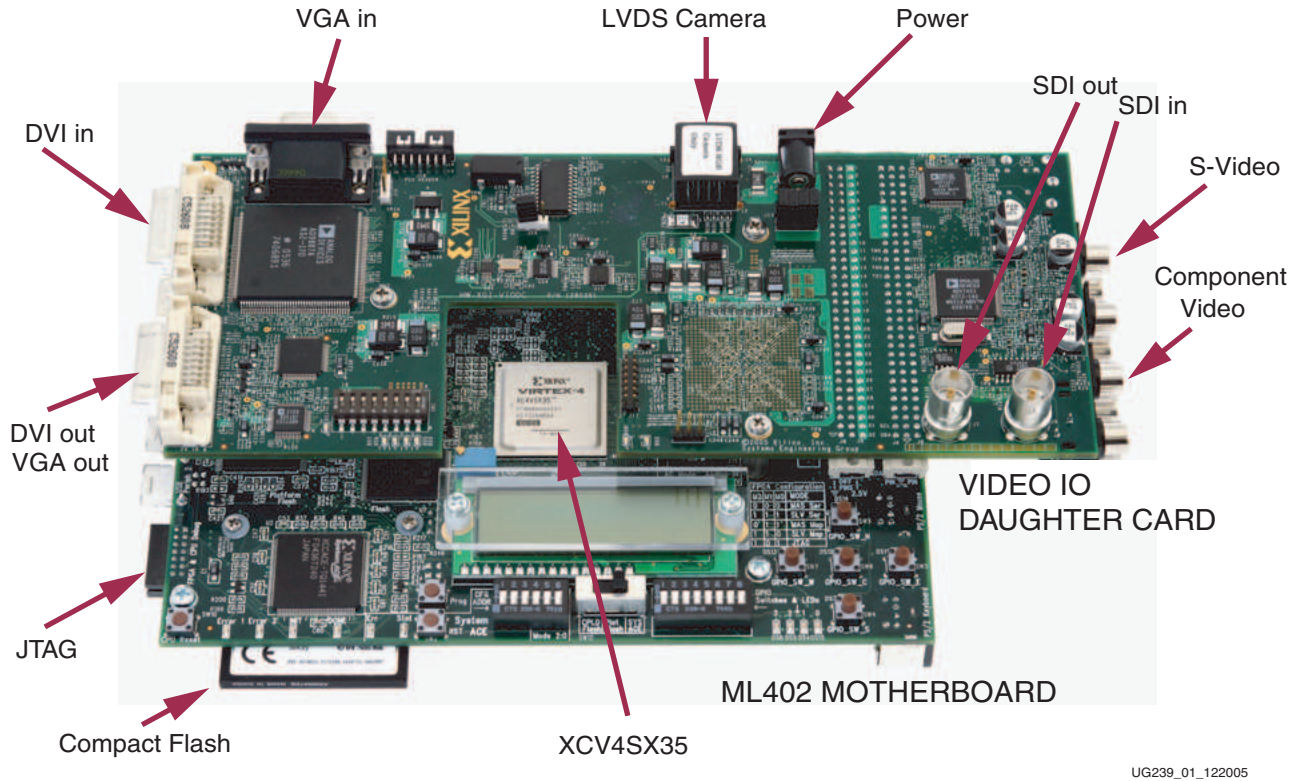

Figure 1-1: **VIODC Attached to an ML402 Platform**

Figure 1-2 shows a block diagram of the VIODC card. The VIODC consists of a number of video interface ICs connected to a Xilinx XCV2P7 FPGA. The VIODC is a daughter card which plugs onto a Xilinx ML40x FPGA platform via the XGI connector. The XGI connector provides a 64-signal bus between the ML40*x* and the VIODC. Collectively these signals are called the VIOBUS in this document.

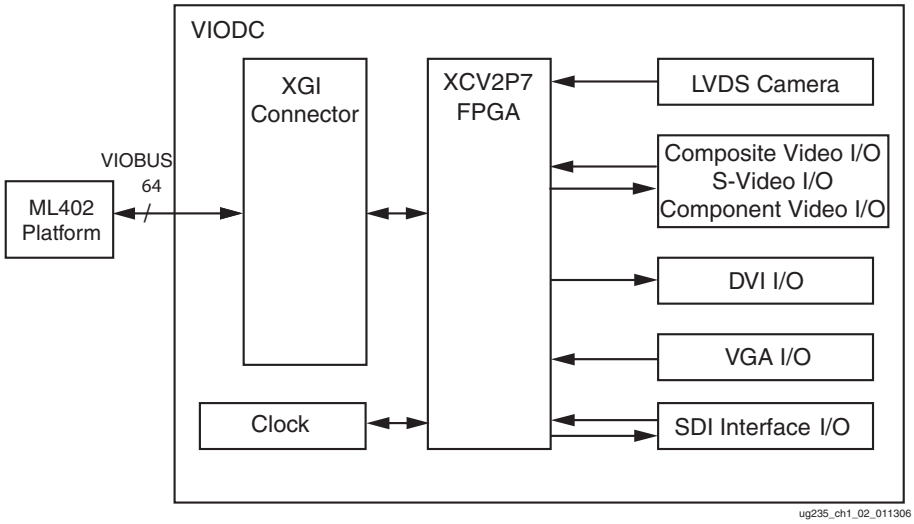

Figure 1-2: **VIODC Block Diagram**

Video Interface Support

The VIODC supports the following video interfaces:

- **LVDS Camera Input Port** – The LVDS camera input port supports the Irvine Sensors LVDS RGB camera with a Micron MT9V022 1/3 inch CMOS image sensor. The camera provides 752 x 480 pixels at 60 Hz progressive scan. It features low noise and very high dynamic range. The interface is implemented using LVDS signaling over standard Cat-6 Ethernet cables. Note that the LVDS camera interface is not compatible with Ethernet.
- **S-Video and Composite Video** – The VSK supports S-Video inputs and outputs. These interfaces can be configured to support NTSC, PAL, and virtually any other SD video format. The S-video input interface is supported by the ADV7403 decoder IC and output by the ADV7321 encoder IC. In addition to the encoder and decoder, analog filters are used to limit the video bandwidth.
- **Component Video I/O** – The component video I/O use standard RCA connectors to provide HD video the VSK. Component video is encoded as YPbPr video channels. The component video input on the supports 1080I, 720P, and 525P video standards. The Component video interface devices on the VSK support 10-bit digital video. Component video input is supported by the ADV7403 IC decoder IC and output by the ADV7321 encoder IC and analog filter sections.
- **DVI Digital Video I/O** – The VSK supports DVI video inputs and outputs. DVI is commonly used to interface to flat panel displays and computer graphics cards. The VSK DVI interfaces supports up to a pixel clock of up to 165 MHz. In addition to computer graphics, DVI is also used to carry HD video and is commonly found in high-end consumer video equipment, such as plasma displays, and can be found on some DVD players. The DVI ports can also be connected to HDMI interfaces by using a DVI/HDMI adapter. A TP410 IC is used to support DVI output and an AD9887 IC provides DVI input.
- **VGA Interface** – VGA input and outputs are is available on the VIODC card. The VGA output is routed to the analog output pins of the DVI output connector. It is sourced by an ADV7123 10-bit DAC. VGA input is captured by the AD9887 IC.

- **SDI Video Interface** – A complete SDI video interface capable of supporting both SD and HD video rates is available on the VSK. The SDI standard is a high-speed serial interface used to carry digital video over coax cable. It is generally used in a studio environment. The SDI system includes cable equalizers and Genlock circuitry. (The VSK is a demonstration platform only. For HD-SDI verification and compliance, Xilinx recommends using the Cook Technologies SDV board).
- **Clock Generator** – The clock generator section is used to generate standard video clock frequencies. It is based on an ICS 1523 clock generator IC.
- **XCV2P7 FPGA** – The VSK also includes a Xilinx XCV2P7 FPGA, which is used to interface to the various video interfaces, as well as the ML402 main board. It features Multi-Gigabit Transceivers (MGTs), which are used to support the SDI interface. It also enables the VIODC to be used in a stand-alone fashion.
- **XGI Connector**– The XGI connector is a standard connector interface used on XiIinx ML40*x* FPGA development platforms. The XGI connector is used to connect to the VIODC to a standard FPGA development platform, such as the ML402. The signals consist of 32 single-ended LVCMOS25 signals and 32 signals that can be configured as either 32 LVCMOS25 signals or 16 LVDS signal pairs. The LVDS pairs are length matched and routed as pairs on the PCB. In addition, 5V power is passed up to the VIODC over the XGI connector.
- **VIOBUS** – The Video Starter Kit (VSK) uses the VIODC as a Video I/O interface. For compatibility with the VSK, the 64 XGI signals have been specified as a bus named the VIOBUS. In this use, the signals on the VIODC XGI connector have been specified as a set of buses that transmit a 27-bit digital video channel from the VIODC to the FPGA development platform and a 27-bit bus to transmit a similar digital video channel from the ML40*x* to the VIODC. Each video channel consists of a 24-bit digital video bus, HSYNC, VSYNC and a clock enable signal. The pinout for the VIOBUS can be found in Appendix A, "Reference Information." This implementation of the interface runs synchronous to the interface clock supplied by the ML402 board. The VIOBUS also specifies an LVDS clock, a reset signal, an I2C interface, and a 4-pin serial bus.

Chapter 2

VIODC to ML402 Card Interface

When the VIODC is used as part of the Video Starter Kit (VSK) from Xilinx, the 64-pin XGI connector connects the VIODC to a ML402 card to communicate with the VIODC card. When the VIODC is used with the VSK, the 64 XGI signals are allocated to a bus named the VIOBUS, which serves the following functions:

- Transfers video data between the ML402 card and the VIODC card.
- Provides a clock to the VIODC card.
- Provides reset to the VIODC card.
- Provides a low-pin count serial bus to access registers on the VIODC.
- Provides an I2C bus (an industry standard 2-pin serial data bus used to communicate and configure ICs) to access registers on the VIODC video interface FPGA.

VIOBUS Clocking

The VIOBUS uses a simple synchronous interface running at 100 MHz (Figure 2-1).

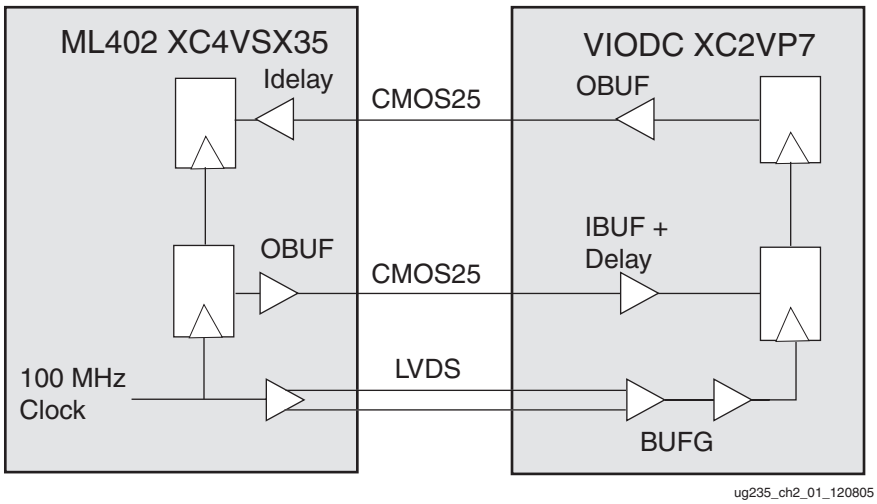

Figure 2-1: **VIOBUS Clocking**

A clock is passed from the ML402 FPGA to the VIODC using differential signaling. All data signals are single ended. The VIODC transmits data back to the ML402 FPGA using the received clock. Data returning back from the VIODC is clocked into the ML402 FPGA using the internal 100 MHz clock.

Future VIODC bus interfaces may implement a differential bus using the 16 differential pairs available on HDR2 and more sophisticated clocking.

VIOBUS Signal Definitions

Table 2-1: **VIOBUS Signal Definitions**

Signal	Description	nbits	Type	Target Speed	Source FPGA	XGI Pins
VIO Data Bus (a moderate-speed single-ended bus)						
vio_up[25:0]	Data bus to the VIODC	26	LVCMOS25	100 MHz	ML402	hdr1[20:2], hdr2[2:32]
vio_up_ena	Pixel enable for vio_up[25:0]	1	LVCMOS25	100 Mhz	ML402	hdr1[22]
vio_dn[25:0]	Data bus from the VIODC	26	LVCMOS25	100 MHz	VIODC	hdr1[42:24], hdr2[64:34]
vio_dn_ena	Pixel enable for vio_up[25:0]	1	LVCMOS25	100 MHz	VIODC	hdr1[44]
Sport Serial Bus (used to configure registers in the VIODC FPGA)						
vio_sport_up	Sport write data (16-bit data, 16-bit address)	1	LVCMOS25	10 MHz	ML402	hdr1[54]
vio_sport_dn	Sport return data	1	LVCMOS25	10 MHz	VIODC	hdr1[52]
vio_sport_sync	Sport sync pulse	1	LVCMOS25	10 MHz	ML402	hdr1[50]
vio_sport_clk	Sport clock	1	LVCMOS25	10 MHz	ML402	hdr1[48]
I2C Serial Bus (used to configure registers in the video devices)						
vio_i2c_sda_up	I2C write data	1	LVCMOS25	400 kHz	ML402	hdr1[60]
vio_i2c_sda_dn	I2C return data	1	LVCMOS25	400 kHz	VIODC	hdr1[58]
vio_i2c_scl_up	I2C clock signal	1	LVCMOS25	400 kHz	ML402	hdr1[56]
Miscellaneous						
vio_reset	Active High reset to VIODC	1	LVCMOS25	10 MHz	ML402	hdr1[46]
Clock						
vio_up_clk_lvds_P,N		1	LVDS25	400 MHz	ML402	hdr1[64:62]]

Refer to the VIOBUS pinout in Appendix A, "Reference Information" for signal locations.

Chapter 3

Component and S-Video Interfaces

Overview

The VIODC board supports input and output for S-video, composite, and component video. Figure 3-1 is a simplified block diagram of input and output.

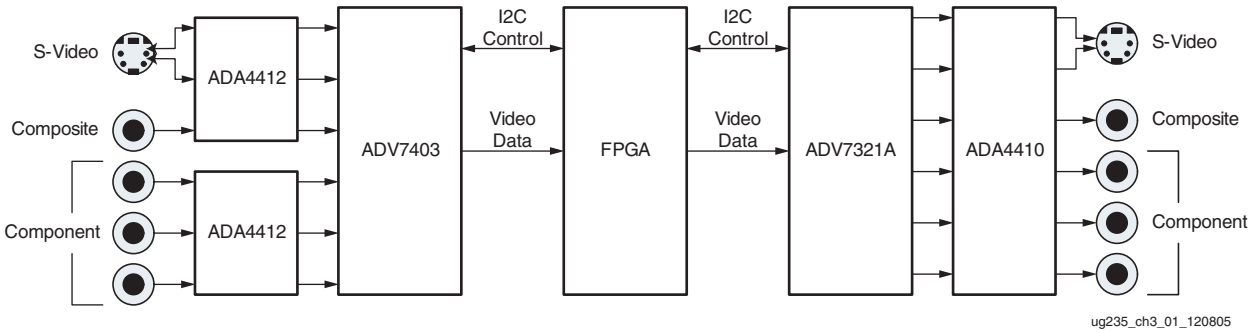

Figure 3-1: **S-Video, Composite, and Component Video Input and Output Block Diagram**

Input signals are conditioned by a combination of passive components and the ADA4412 device. The conditioned input signals are converted to digital signals by the ADV7403 video decoder device. Digital video output data stream from the FPGA is converted to analog signals by the ADV7321 video encoder device. The analog output signals are conditioned by the ADA4410 device.

The video decoder, ADV7403 from Analog Devices, is responsible for converting analog video signals into a representative digital video data stream. The video encoder, ADV7321A also from Analog Devices, is responsible for the generation of S-Video, composite, and component analog video signals from a digital video data stream. Both devices offer an I^2C control serial bus for control and ancillary data.

ADV7403 Video Decoder

The ADV7403 is a high quality, single chip, multiple format video decoder and graphics digitizer. This multiple format decoder automatically supports the conversion of PAL, NTSC, and SECAM standards in the form of composite or S-video into a digital ITU-R BT.656 format. The component processor is capable of decoding/digitizing a wide selection of video formats in any color space. Component video standards supported include: 525i, 625i, 525p, 625p, 720p, 1080i and many other HD standards, as well as graphic digitization from VGA to SXGA. Converted input signals are output to the output pixel port, which is connected directly to the FPGA. Under user control, the output pixel port is configurable to conform to multiple different standards. Selection of the format is done through commands written to the device over the I^2C bus and affects the pins

definitions. For complete details, refer to the Analog Devices data sheet found at www.analog.com

ADV7321 Video Encoder

The Analog Devices ADV7321 video encoder device is a single monolithic chip that performs multiple format digital-to-analog video encoder functions. Both standard and high definition input formats are supported including: SMPTE 293M (525p), BTA T-1004 EDTV2 (525p), CCIR-656, and SMPTE 274M. Multiple output standards for both SD and HD are also supported including: YPrPb HDTV (EIA 770.3), RGB, RGBHV, YPrPb progressive scan (EIA-770.1, EIA-770.2) and component YPrPb (SMPTE/EBU N10). 4:2:2 or 4:4:4 data format is supported for HDTV. For all standards, external horizontal, vertical and blanking signals or EAV/SAV timing codes control the insertion of appropriate synchronization signals into the digital data stream and, therefore, the analog output signal.

The ADV7321 provides user configuration options through an I^2C bus, which enables access to a large number of configuration registers. Under user control, the device pins are reconfigured to match the operation selected. For instance, SD 8-bit mode configuration only, the data input port S7-S0 would be used to transfer in a multiplexed fashion the digital video data stream into the device. The Y and C buses would not be used. Refer to Analog Devices ADV7321 data sheet for further details.

Video Signal Input and Output Conditioning

Each of the video input and output signals must be conditioned to ensure that the physical interfaces meet impedance and electrical specification for each individual video standard. Figure 3-3 illustrates the input and output conditioning circuits used for S-video, composite and component input and output signals.

S-Video Input and Output

S-Video Input

Connector J20 provides input and output of S-Video compatible signals. For the input, the Y (intensity) and C (color) signals are each conditioned and input into the ADV7403 video decoder to create a digital video data stream output, which is transferred to the Xilinx XC2VP4 FPGA for handling. Generation of S-Video output starts with a digital video stream coming from the FPGA, written into the ADV7321A video encoder to product the Y/C analog outputs, which are conditioned and output to the J20 S-Video connector.

S-Video Input Signal Conditioning

S-Video input signals are first conditioned using two identical circuits illustrated in Figure 3-2. This circuit contains both passive and active components, including the Analog Devices ADA4412 device. This conditioning circuit insures that the input signal impedance matches the S-Video (IEC 60933-5) specification and signal levels required by the ADV7403.

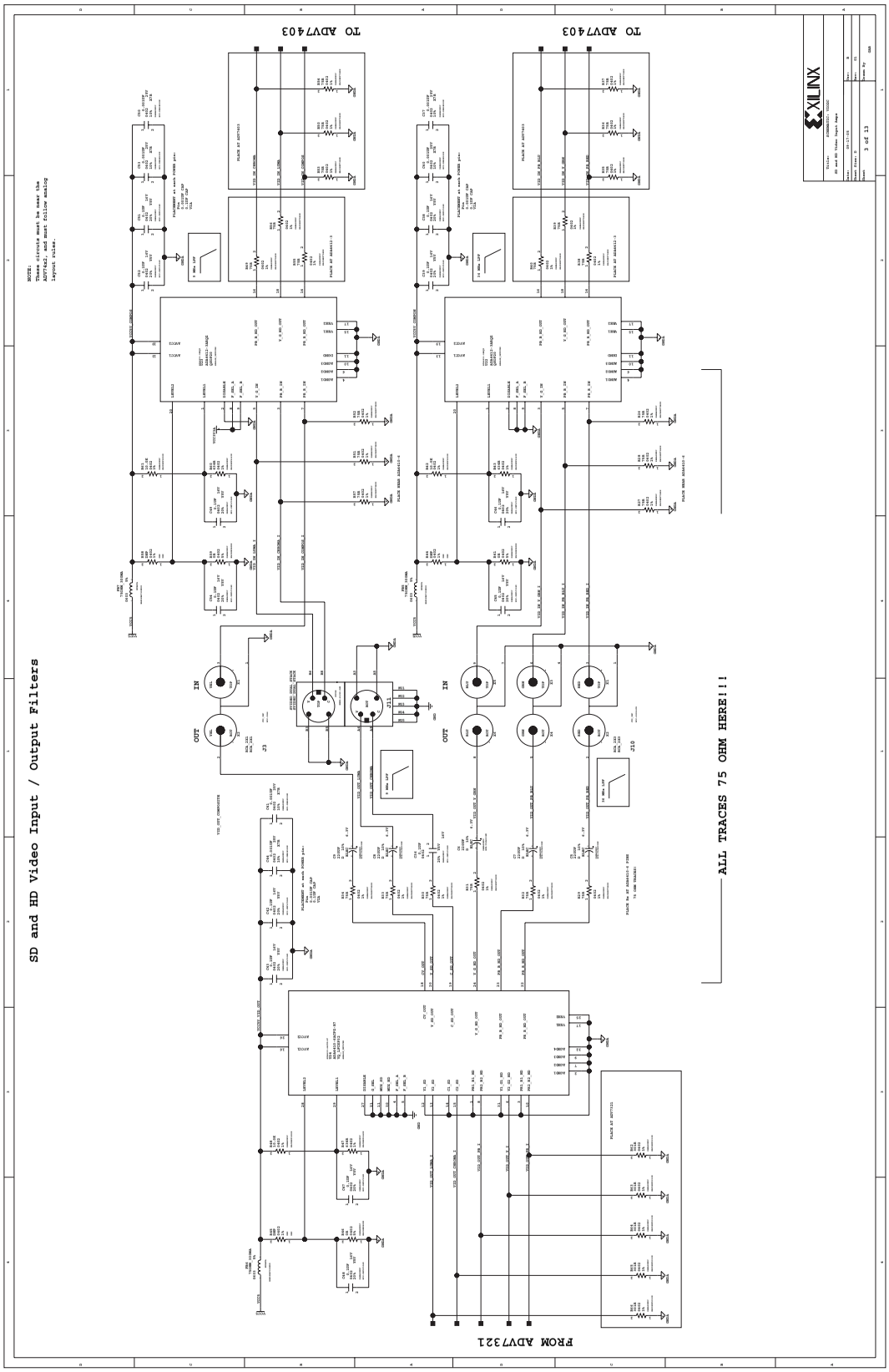

Figure 3-2: **S-Video, Composite, and Component Input and Output Signal Conditioning Circuit**

ADV7403 S-Video Input

The Y (intensity) and C (color) conditioned signals are input into the A12 and A10 of the ADV7403 twelve input analog multiplexer, which routes each of the selected input signals to one of the ADCs for conversion. Fully automatic detection and selection of all worldwide standards, (PAL, NTSC and SECAM) is provided as well as vertical blanking processing for Teletext, Closed Caption and wide screen signaling. For full details regarding the ADV7403 device refer to the Analog Devices datasheet.

The digital data stream generated from the conversion of the S-Video signals is available to the FPGA through a 41-bit data bus and 5-bit control. An I2C bus available on the ADV7403 provides control, status and ancillary data and is directly connected to the FPGA. For S-Video configuration there are 6 different interface configurations that use some of the lower 30 pins. The default configuration is to output YCrCb data on the 8-bit portion of the data bus from P19 to P12.

S-Video Output

Generation of S-Video output video from a digital video data stream is accomplished by the ADV7321 device. Video data is written from the XC2VP4 FPGA into the ADV7321 device, which converts from digital-to-analog values using DAC D and E. The analog output signals are conditioned to meet specification with the conditioned output going through connector J20.

ADV7321 S-Video Output

Data, video timing control and operations control bus connections between the FPGA and ADV7321 video encoder provide the digital video data stream and information needed to convert to generate analog S-Video Y/C signals. The FPGA writes the digital video data stream and control into the ADV7321, which then produces the appropriate analog output with complete video timing. The format of the data written is selectable the analog output is first conditioned and then placed on the output S-Video connector J20.

S-Video Output Signal Conditioning

Figure 3-2 details the implementation of the S-Video output conditioning circuit following the ADV7321 Y/C analog signal generation. This conditioning circuit is composed of both active and passive components, with the ADA4410 device providing active circuits and is designed to meet the specification IEC 60933-5 requirements for S-Video.

Composite Video Input and Output

Composite video is the format of an analog television (picture only) signal before it is combined with a sound signal and modulated onto an RF carrier. It is usually in a standard format such as NTSC, PAL, or SECAM. It is a composite of three source signals called Y, U and V with sync pulses. Y represents the brightness or *luminance* of the picture and includes synchronizing pulses, so that by itself it could be displayed as a monochrome picture. U and V between them carry the color information.

Composite video input and output is supported on the VIODC card through RCA type jack J18, this dual RCA jack has the composite video input on X1 and output on X2 and are color coded yellow. Input signals are conditioned and then presented to the ADV7403 for conversion to digital video data stream. The ADV7403 device automatically detects the video standard (PAL, NTSC, SECAM) and converts to the appropriate data stream with control information. The resulting data stream and control information is transferred to the

FPGA for further processing. A digital video data stream with control is converted to a composite video stream by the ADV7321A device and associated signal conditioning circuits. The data stream and control is supplied by the FPGA.

Composite Video Input

Composite video input on connector J18 X1 is first conditioned and then converted to the digital video data stream, which is passed to the XC2VP4 for further processing. The ADV7403 device is configurable under user control to select the format of the devices pixel output port. In SD composite video mode up to 3 10-bit data busses can be used to transfer the video data.

Composite Video Input Conditioning Circuit

To insure compatibility with the specification an input conditioning circuit is inserted before the ADV7403 analog input. Impedance matching for the input signal and level matching for the analog input are assured. Figure 3-2 details the implementation of this circuit.

ADV7403 Composite Video Input

The conditioned composite video input signal is input on the 11th input of the 12 input analog multiplexer. When configured properly by the user the input will be routed to an analog-to-digital converter and automatic format detection logic to generate the digital video data stream. Configuration of the ADV7403 device is through the I2C control bus and appropriate writes to a number of registers. As part of the configuration process the user will select the format of the output data. For programming details please refer to the Analog Devices ADV7403 data sheet.

Composite Video Output

Generation of composite video output starts with a digital video data stream being written from the XC2VP4 into the ADV7321A video encoder, which produces an analog output that is conditioned and presented on connector J18 X2.

ADV7321A Composite Video Output

The XC2VP4 Xilinx FPGA provides both the digital video data stream and the configuration to the ADV7321A. Configuration of the ADV7321A defines the interface connections and active pins for the connection from the XC2VP4 and to the ADV7321A. For composite video the input format can be configured for either 8/10-bit ITU-BT.656/601 or 16/20-bit YCrCb with embedded HS, VS and FIELD codes. The input digital video data stream is then converted to an analog composite video output signal that includes all timing and control signaling.

Composite Video Conditioning Circuit

The analog output of the ADV7321A is processed by a conditioning circuit that insures that the composite output signal meets composite video drive specifications. Figure 3-2 details the composite video output circuit.