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Innovasic®
Semiconductor
Extended Life Semiconductor Solutions

IA82527
Serial Communications Controller—CAN Protocol
Data Sheet

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1. Introduction

The Innovasic Semiconductor IA82527 Controller Area Network (CAN) Serial Communications Controller is a form, fit, and function replacement for the original Intel® 82527 Serial Communications Controller.

These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, MILES™ captures the clone design in such a way that production of the clone can continue even as silicon technology advances.

The IA82527 Serial Communications Controller replaces the obsolete Intel 82527 device, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools, thereby avoiding expensive redesign efforts.

1.1 General Description

CAN protocol uses a multi-master CSMA/CR (Carrier Sense, Multiple Access with Collision Resolution) bus to transfer message objects between network nodes.

The IA82527 support CAN Specification 2.0 Part A and B, standard and extended message frames, and has the capability to transmit, receive, and perform message filtering on standard and extended message frames.

The IA82527 can store 15 message objects of 8-byte data length. Each message object can be configured as either transmit or receive except for message object 15, which is receive-only. Message object 15 also provides a special acceptance mask designed to filter message identifiers that are received.

The IA82527 also provides a programmable acceptance mask that allows users to globally mask any identifier bits of the incoming message. This global mask can be used for both standard and extended message frames.

The IA82527 is capable of operating at 5.0 or 3.3 volts. This datasheet discusses both modes of operation. Where applicable, characteristics specific to either 3.3 or 5.0 volt operation are identified separately throughout this datasheet.

The IA82527 is manufactured in a reliable 5-volt process technology and is available in 44-lead PLCC or PQFP RoHS packages for the automotive temperature range (-40°C to 125°C).

1.2 Features

The primary features of the IA82527 are as follows:

- CAN Protocol Support
  - Specification 2.0, Part A and Part B
  - Standard ID Data and Remote Frames
  - Extended ID Data and Remote Frames

- CAN Bus Interface
  - Configurable Input Comparator
  - Configurable Output Driver
  - Programmable Bit Rate

- Global Mask, Programmable
  - Standard Message Identifier
  - Extended Message Identifier

- Message Objects
  - 14 Transmit/Receive Buffers
  - 1 Double Buffered Receive Buffer with Programmable Mask

- Flexible Status Interface

- CPU Interface Options
  - 16-Bit Multiplexed Intel Architecture
  - 8-Bit Multiplexed Intel Architecture
  - 8-Bit Multiplexed Non-Intel Architecture
  - 8-Bit Non-Multiplexed Non-Intel Architecture
  - Serial (SPI)

- I/O Ports (2)
  - 8-Bit
  - Bidirectional

- Flexible Interrupt Structure

- Programmable Clock Output

A detailed description of the IA82527, including the features listed above, is provided in Chapter 4, Functional Description.

2. Packaging, Pin Descriptions, and Physical Dimensions

2.1 Packages and Pinouts

The Innovasic Semiconductor IA82527 CAN Serial Communications Controller is available in the following RoHS packages:

- 44-Pin Plastic Leaded Chip Carrier (PLCC), equivalent to original Intel PLCC package
- 44-Pin Plastic Quad Flat Pack (PQFP), equivalent to original Intel QFP package

2.1.1 PLCC Package

The pinout for the PLCC Package is as shown in Figure 1. The corresponding pinout is provided in Table 1.

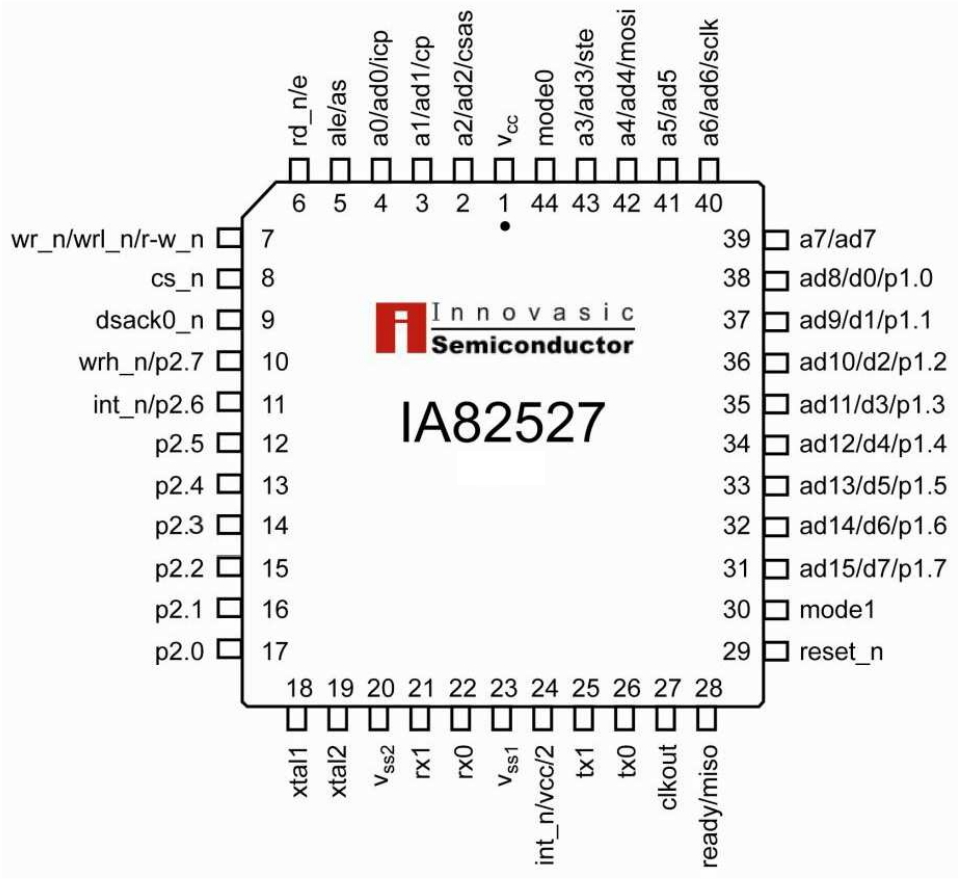


Figure 1. PLCC Package Diagram

Table 1. PLCC Pin List

Pin	Name
1	v_{cc}
2	a2/ad2/csas
3	a1/ad1/cp
4	a0/ad0/icp
5	ale/as
6	rd_n/e
7	wr_n/wrl_n/r-w_n
8	cs_n
9	dsack0_n
10	wrh_n/p2.7
11	int_n/p2.6

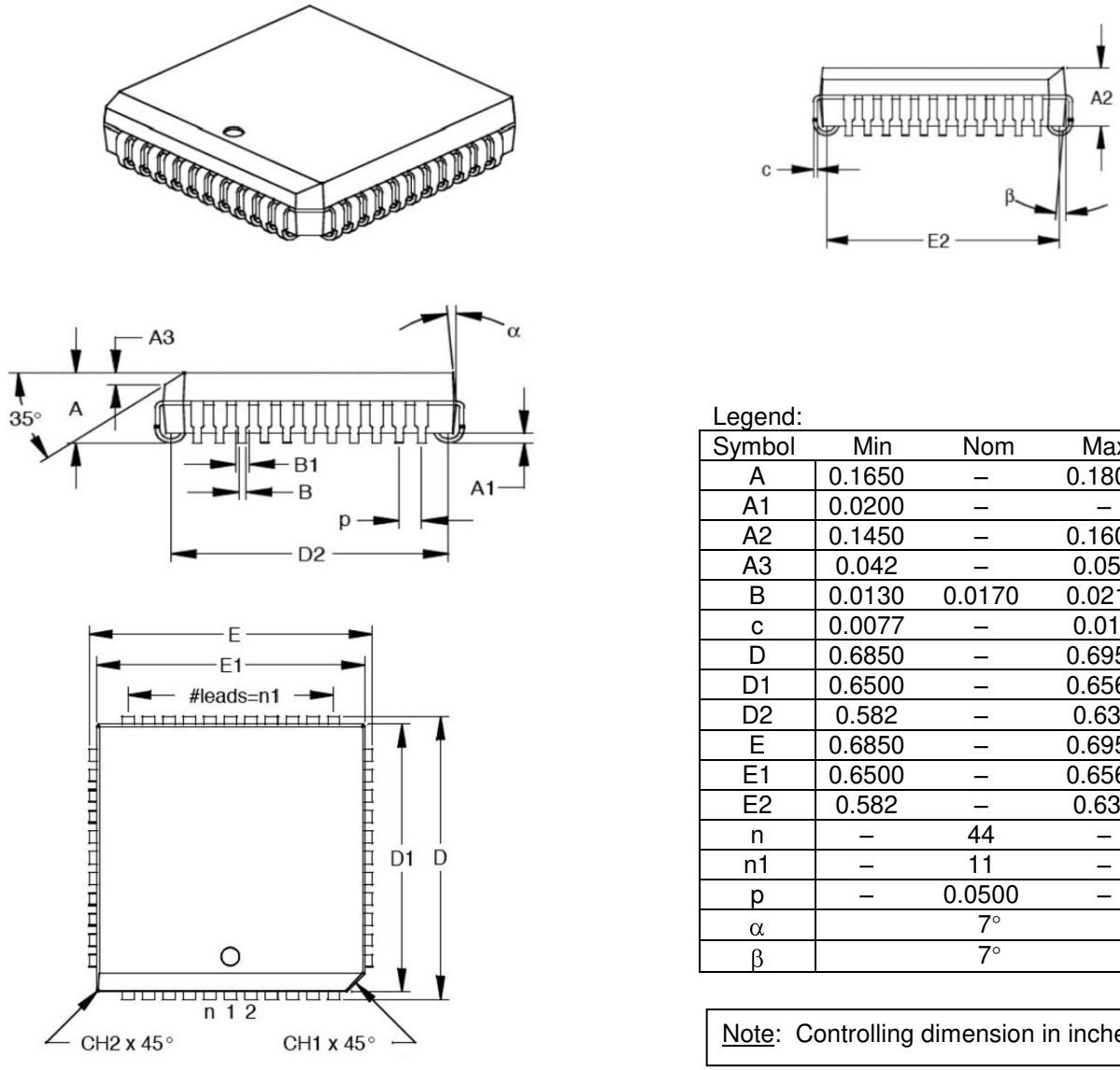
Pin	Name
12	p2.5
13	p2.4
14	p2.3
15	p2.2
16	p2.1
17	p2.0
18	xtal1
19	xtal2
20	v_{ss2}
21	rx1
22	rx0

Pin	Name
23	v_{ss1}
24	int_n/v_{cc}/2
25	tx1
26	tx0
27	clkout
28	ready/miso
29	reset_n
30	mode1
31	ad15/d7/p1.7
32	ad14/d6/p1.6
33	ad13/d5/p1.5

Pin	Name
34	ad12/d4/p1.4
35	ad11/d3/p1.3
36	ad10/d2/p1.2
37	ad9/d1/p1.1
38	ad8/d0/p1.0
39	a7/ad7
40	a6/ad6/sclk
41	a5/ad5
42	a4/ad4/mosi
43	a3/ad3/ste
44	mode0

2.1.2 PLCC Physical Dimensions

The physical dimensions for the PLCC are as shown in Figure 2.



Legend:

Symbol	Min	Nom	Max
A	0.1650	–	0.1800
A1	0.0200	–	–
A2	0.1450	–	0.1600
A3	0.042	–	0.056
B	0.0130	0.0170	0.0210
c	0.0077	–	0.015
D	0.6850	–	0.6950
D1	0.6500	–	0.6560
D2	0.582	–	0.638
E	0.6850	–	0.6950
E1	0.6500	–	0.6560
E2	0.582	–	0.638
n	–	44	–
n1	–	11	–
p	–	0.0500	–
α		7°	
β		7°	

Note: Controlling dimension in inches.

Figure 2. PLCC Physical Dimensions

2.1.3 PQFP Package

The pinout for the PQFP Package is as shown in Figure 3. The corresponding pinout is provided in Table 2.

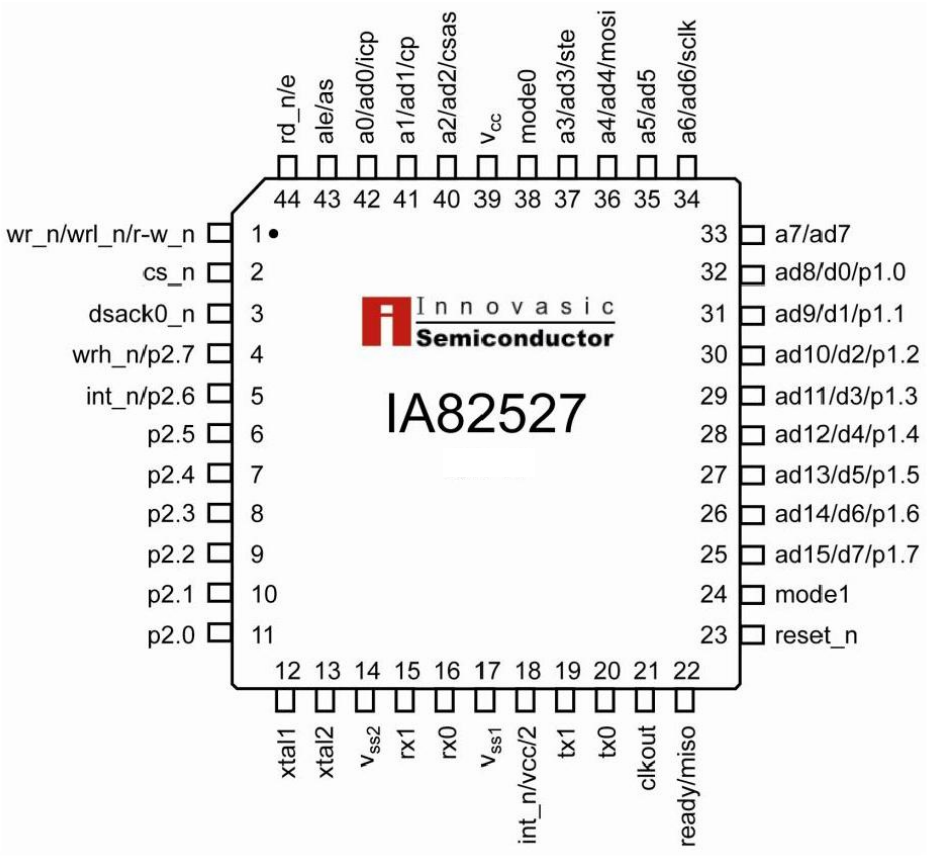


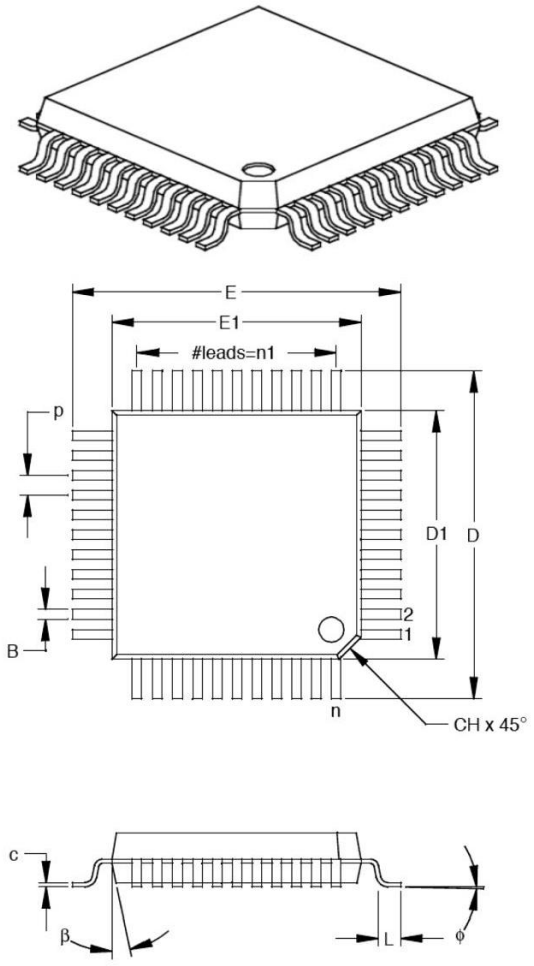
Figure 3. PQFP Package Diagram

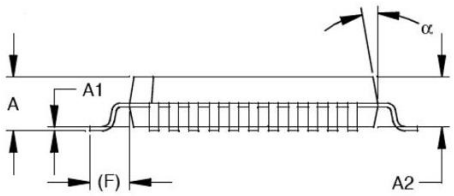
Table 2. PQFP Pin List

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	wr_n/wrl_n/r-w_n	12	xtal1	23	reset_n	34	a6/ad6/sclk
2	cs_n	13	xtal2	24	mode1	35	a5/ad5
3	dsack0_n	14	v_{ss2}	25	ad15/d7/p1.7	36	a4/ad4/mosi
4	wrh_n/p2.7	15	rx1	26	ad14/d6/p1.6	37	a3/ad3/ste
5	int_n/p2.6	16	rx0	27	ad13/d5/p1.5	38	mode0
6	p2.5	17	v_{ss1}	28	ad12/d4/p1.4	39	v_{cc}
7	p2.4	18	int_n/v_{cc}/2	29	ad11/d3/p1.3	40	a2/ad2/csas
8	p2.3	19	tx1	30	ad10/d2/p1.2	41	a1/ad1/cp
9	p2.2	20	tx0	31	ad9/d1/p1.1	42	a0/ad0/icp
10	p2.1	21	clkout	32	ad8/d0/p1.0	43	ale/as
11	p2.0	22	ready/miso	33	a7/ad7	44	rd_n/e

2.1.4 PQFP Physical Dimensions

The physical dimensions for the PQFP are as shown in Figure 4.





Legend:

Symbol	Min	Nom	Max
n	–	44	–
n1	–	11	–
p	–	0.031	–
A	–	–	0.096
A2	–	0.079	–
A1	–	0.010	–
L	0.019	0.025	0.031
(F)	–	0.047	–
E	0.478	0.488	0.498
D	0.478	0.488	0.498
E1	0.390	0.394	0.398
D1	0.390	0.394	0.398
c	0.005	0.007	0.009
B	0.011	0.014	0.017
CH	–	0.030	–
α	5°	–	16°
β	5°	–	16°
ϕ	0°	–	10°

Note: Controlling dimension in inches.

Figure 4. PQFP Physical Dimensions

2.2 Pin/Signal Descriptions

Descriptions of the pin and signal functions for the IA82527 Serial Communications Controller are provided in Table 3.

Several of the IA82527 pins have different functions depending on the operating mode of the device. Each of the different signals supported by a pin is listed and defined in Table 3, indexed alphabetically in the first column of the table. Additionally, the name of the pin associated with the signal as well as the pin numbers for both the PLCC and PQFP packages are provided in the "Pin" column. If the signal and pin names are the same, no entry is provided in the "Pin-Name" column.

Table 3. Pin/Signal Descriptions

Signal	Pin			Description
	Name	PLCC	PQFP	
a0	a0/ad0/icp	4	42	**a**ddress bits **7–0**. Input. Mode 3. When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), these lines provide the 8-bit address bus input to the device.
a1	a1/ad1/cp	3	41	
a2	a2/ad2/csas	2	40	
a3	a3/ad3/ste	43	37	
a4	a4/ad4/mosi	42	36	
a5	a5/ad5	41	35	
a6	a6/ad6/sclk	40	34	
a7	a7/ad7	39	33	
ad0	a0/ad0/icp	4	42	**a**ddress/**d**ata bits **15–0**. Input/Output. Mode 1. When the IA82527 is configured to operate in the 16-bit multiplexed Intel architecture mode (Mode 1), these lines provide the 16-bit address bus (input) and the 16-bit data bus (input/output) for the device.
ad1	a1/ad1/cp	3	41	
ad2	a2/ad2/csas	2	40	
ad3	a3/ad3/ste	43	37	
ad4	a4/ad4/mosi	42	36	
ad5	a5/ad5	41	35	
ad6	a6/ad6/sclk	40	34	
ad7	a7/ad7	39	33	
ad8	ad8/d0/p1.0	38	32	
ad9	ad9/d1/p1.1	37	31	
ad10	ad10/d2/p1.2	36	30	
ad11	ad11/d3/p1.3	35	29	
ad12	ad12/d4/p1.4	34	28	
ad13	ad13/d5/p1.5	33	27	
ad14	ad14/d6/p1.6	32	26	
ad15	ad15/d7/p1.7	31	25	

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
ale	ale/as	5	43	**a**ddress **l**atch **e**nable. Input. Active High. Mode 0 and Mode 1. When the IA82527 is configured to operate in either the 8-bit multiplexed Intel architecture mode (Mode 0) or the 16-bit multiplexed Intel architecture mode (Mode 1), this signal latches the address into the device during the address phase of the bus cycle.
as	ale/as	5	43	**a**ddress **s**trobe. Input. Active High. Mode 2. When the IA82527 is configured to operate in the 8-bit multiplexed non-Intel architecture mode (Mode 2), this signal latches the address into the device during the address phase of the bus cycle. If the IA82527 is configured to operate in Mode 3 (8-bit non-multiplexed non-Intel architecture), this pin must be tied high.
clkout	clkout	27	21	**cl**oc**k out**. Output (push-pull). This output provides a programmable clock frequency. The frequency is set via the Clockout Register (1FH) and can range from the frequency of the **xtal** (crystal) input to xtal/n, where n can be an integer value from 2 through 15. This output allows the IA82527 to clock other devices such as the host CPU. **For 3.3V operation the crystal or external oscillator must run at <=12 MHz to produce clock output.**
cp	a1/ad1/cp	3	41	**c**lock **p**hase. Input. Serial Interface Mode. When this input is a logic 0, data is sampled on the rising edge of sclk. When this input is a logic 1, data is sampled on the falling edge of sclk.
cs_n	cs_n	8	2	**c**hip **s**elect. Input. Active Low (Modes 0–3); Selectable Active Level (Serial Interface Mode). When the IA82527 is configured to operate in one of the parallel interface modes (Modes 0–3) or the Serial Interface Mode, this input, during its active state, selects the device allowing CPU access. For Serial Interface Mode operation, the active state is selectable (i.e., either high or low) via the IA8257 csas pin.
csas	a2/ad2/csas	2	40	**c**hip **s**elect **a**ctive **s**tate. Input. Serial Interface Mode. When this input is a logic 0, the cs_n input is configured to function active low. When this input is a logic 1, the cs_n input is configured to function active high.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
d0	ad8/d0/p1.0	38	32	**d**ata bits **7–0**. Input/Output. Mode 3. When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), these lines provide the 8-bit data bus to the device.
d1	ad9/d1/p1.1	37	31	
d2	ad10/d2/p1.2	36	30	
d3	ad11/d3/p1.3	35	29	
d4	ad12/d4/p1.4	34	28	
d5	ad13/d5/p1.5	33	27	
d6	ad14/d6/p1.6	32	26	
d7	ad15/d7/p1.7	31	25	
dsack0_n	dsack0_n	9	3	**d**ata and **s**ize **ack**nowledge **0**. Output. Active Low (open drain with active pull-up). Mode 3 (asynchronous operation). When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), this signal functions as follows: when the CPU reads from the IA82527, **dsack0_n** active low indicates that the data is valid; when the CPU writes to the IA82527, **dsack0_n** active low indicates that the data has been received. Note: The active pull-up circuitry drives **dsack0_n** high for 10ns to raise it to a 3.0V voltage level. After that, an external pull up is required to pull **dsack0_n** the remainder of the way to V_{SS}.
e	rd_n/e	6	44	**e**nable. Input. Active High. Mode 3 (synchronous). When the IA82527 is configured to operate in the 8-bit non-multiplexed non-Intel architecture mode (Mode 3), this signal functions as follows: when the CPU reads from or writes to the IA82527, **e** active high indicates that the address is valid.
icp	a0/ad0/icp	4	42	**i**dle **c**lock **p**olarity. Input. Serial Interface Mode. When this input is a logic 0, the polarity for the idle state of sclk is low. When this input is a logic 1, the polarity for the idle state of sclk is high.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
int_n	int_n/ $V_{CC}/2$	24	18	**int**errupt. Output (open collector). Active Low. On the IA82527, two pins can provide the interrupt (**int_n**) output; however, depending on the setting of the MUX bit in the CPU Interface Register (02H), only one of the pins will serve as the source of **int_n** as follows: • PLCC Package: – When the MUX bit of the CPU Interface Register is 0, pin 24 functions as the **int_n** output and pin 11 functions as **p2.6**. – When the MUX bit of the CPU Interface Register is 1, pin 11 functions as the **int_n** output and pin 24 functions as $V_{cc}/2$. • PQFP Package: – When the MUX bit of the CPU Interface Register is 0, pin 18 functions as the **int_n** output and pin 5 functions as **p2.6**. – When the MUX bit of the CPU Interface Register is 1, pin 5 functions as the **int_n** output and pin 18 functions as $V_{cc}/2$.
	int_n/p2.6	11	5	
miso	ready/miso	28	22	**m**aster **i**n **s**lave **o**ut. Output (open drain). Serial Interface Mode. When the IA82527 is configured to operate with a serial interface, **miso** is the serial data output.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
mode0	mode0	44	38	**mode**N (N = **1** or **0**). Input. The logic levels at the **mode0** and **mode1** inputs determine the operating mode (i.e., interface type) of the IA82527 as follows: mode1 mode0 Interface Type 0 0 8-bit multiplexed Intel 0 1 16-bit multiplexed Intel 1 0 8-bit multiplexed non-Intel 1 1 8-bit Non-multiplexed non-Intel The **mode1** and **mode0** inputs are also used to establish the Serial Interface Mode as follows: when the IA82527 is reset, if • **mode1** = 0 • **mode0** = 0 • rd_n = 0 • wr_n = 0 the Serial Interface Mode will be selected. The **mode1** and **mode0** pins are internally connected to weak pull-downs. These pins will be pulled low during reset if unconnected. Following reset, these pins will float.
mode1	mode1	30	24	
mosi	a4/ad4/mosi	42	36	**m**aster **o**ut **s**lave **i**n. Input. Serial Interface Mode. When the IA82527 is configured to operate with a serial interface, **mosi** is the serial data input.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
p1.0	ad8/d0/p1.0	38	32	**p**ort **1**, bit N (N = **7**–**0**). Input/Output (general-purpose). Mode 0, Mode 2, and Serial Interface Mode. Port 1 bits **p1.7**–**p1.0** can be individually programmed as inputs or outputs. Programming is accomplished by writing to the P1CONF Register (9FH). The 8 bits of the P1CONF Register, P1CONF7–P1CONF0, correspond directly to pins **p1.7**–**p1.0**. Writing a 0 to a bit in the P1CONF Register causes the corresponding pin to be configured as a high-impedance input. Writing a 1 to a bit in the P1CONF Register causes the corresponding pin to be configured as a push-pull output. All Port 1 pins have weak pull-ups until the port is configured by writing to the P1CONF Register. The default value of the P1CONF Register following a reset is 00H. Data is read from Port 1 via the P1IN Register (BFH). A logic 0 for any bit in this register means that a logic 0 was read from the corresponding pin; a logic 1 for any bit means that a logic 1 was read from the corresponding pin. The default value of the P1IN Register following a reset is FFH. Data is written to Port 1 via the P1OUT Register (DFH). Writing a logic 0 to any bit in this register means that a logic 0 is written to the corresponding pin; writing a logic 1 to any bit means that a logic 1 is written to the corresponding pin. The default value of the P1OUT Register following a reset is 00H.
p1.1	ad9/d1/p1.1	37	31	
p1.2	ad10/d2/p1.2	36	30	
p1.3	ad11/d3/p1.3	35	29	
p1.4	ad12/d4/p1.4	34	28	
p1.5	ad13/d5/p1.5	33	27	
p1.6	ad14/d6/p1.6	32	26	
p1.7	ad15/d7/p1.7	31	25	

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
p2.0	p2.0	17	11	**p**ort **2**, bit N (N = **7**–**0**). Input/Output. Port 2 bits **p2.7**–**p2.0**, can be individually programmed as inputs or outputs. Programming is accomplished by writing to the P2CONF Register (AFH). The 8 bits of the P2CONF Register, P2CONF7–P2CONF0, correspond directly to pins **p2.7**–**p2.0**. Writing a 0 to a bit in the P2CONF Register causes the corresponding pin to be configured as a high-impedance input. Writing a 1 to a bit in the P2CONF Register causes the corresponding pin to be configured as a push-pull output. All Port 2 pins have weak pull-ups until the port is configured by writing to the P2CONF Register. The default value of the P1CONF Register following a reset is 00H. Data is read from Port 2 via the P2IN Register (CFH). A logic 0 for any bit in this register means that a logic 0 was read from the corresponding pin; a logic 1 for any bit means that a logic 1 was read from the corresponding pin. The default value of the P2IN Register following a reset is FFH. Data is written to Port 2 via the P2OUT Register (EFH). Writing a logic 0 to any bit in this register means that a logic 0 is written to the corresponding pin; writing a logic 1 to any bit means that a logic 1 is written to the corresponding pin. The default value of the P2OUT Register following a reset is 00H. Two bits of Port 2 (P2.7 and P2.6) have alternate functions based on CPU interface mode. See Section 4.1.3 I/O Ports.
p2.1	p2.1	16	10	
p2.2	p2.2	15	9	
p2.3	p2.3	14	8	
p2.4	p2.4	13	7	
p2.5	p2.5	12	6	
p2.6	int_n/p2.6	11	5	
p2.7	wrh_n/p2.7	10	4	
rd_n	rd_n/e	6	44	**read**. Input. Active Low. Mode 0 and Mode 1. When **rd_n** is asserted (low), it causes the IA82527 to drive the data from the location being read onto the data bus.
ready	ready/miso	28	22	**ready**. Output (open drain). Active High. Mode 0 and Mode 1. When ready is asserted (high), it signals the completion of a bus cycle. The ready output is provided to force system CPU wait states as required.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
reset_n	reset_n	29	23	**reset**. Input. Active Low. When the **reset_n** signal is asserted (low), the IA82527 is initialized. There are two reset situations: Cold reset is a power-on reset. As V_{CC} is driven to a valid level (power on), the **reset_n** signal must be driven low for a minimum of 1 ms measured from a valid V_{CC} level. No falling edge on the reset_n pin is required during a cold reset. For warm reset, V_{CC} remains at a valid level (i.e., power is already on and remains on) while **reset_n** is driven low for a minimum of 1 ms.
r-w_n	wr_n/wrl_n/r-w_n	7	1	**r**ead-**w**rite. Input. Active High (read)-Active Low (write). Mode 2 and Mode 3. When **r-w_n** is high, it signals a read cycle. When **r-w_n** is low, it signals a write cycle.
rx0	rx0	22	16	Receive (**rx**), lines **0** and **1**. Input. Pins **rx0** and **rx1** are the inputs to the IA82527 from the CAN bus lines. These pins connect internally to the receiver input comparator. Serial data from the CAN bus can be received using both **rx0** and **rx1** or by using only **rx0** as follows: • When the CoBy Bit in the Bus Configuration Register (2FH) is a 0, **rx0** and **rx1** are connected to the input comparator **rx0** is connected to the non-inverting input and **rx1** is connected to the inverting input). A recessive level is read when **rx0** > **rx1**. A dominant level is read when **rx1** > **rx0**. • When the CoBy Bit in the Bus Configuration Register (2FH) is a 1, input comparison is disabled, and **rx0**, which is still connected to the non-inverting input of the comparator, is the CAN bus line input. For this configuration, the DcR0 bit of the Bus Configuration Register must be a 0. After a cold reset (power on), the default configuration is the use of both **rx0** and **rx1** for the CAN bus input.
rx1	rx1	21	15	
sclk	a6/ad6/sclk	40	34	**s**erial **cl**oc**k**. Input. Serial Interface Mode. The **sclk** pin is the serial clock input to the IA82527 (slave device). The clock signal is provided by the master device.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
ste	a3/ad3/ste	43	37	**s**ynchronization **t**ransmission **e**nable. Input. Serial interface Mode. The logic level at the **ste** pin enables the transmission of the synchronization bytes through the IA82527 miso pin while the master device transmits the Address and Control Byte as follows: • When a logic 0 is placed on the **ste** pin, the synchronization bytes sent through the miso pin are 00H and 00H. • When a logic 1 is placed on the **ste** pin, the synchronization bytes sent through the miso pin are AAH and 55H. The IA82527 sends the synchronization bytes after the cs_n signal has been asserted
tx0	tx0	26	20	Transmit (**tx**), lines **0** and **1**. Output (push-pull). Pins **tx0** and **tx1** are the outputs from the IA82527 to the CAN bus lines. During a recessive bit, **tx0** is high and **tx1** is low. During a dominant bit, **tx0** is low and **tx1** is high.
tx1	tx1	25	19	
V_{CC}	V_{CC}	1	39	Power (**V_{CC}**). This pin provides power for the IA82527 device. It must be connected to a +5V DC power source.
$V_{CC}/2$	int_n/ $V_{CC}/2$	24	18	Reference Voltage, ISO Physical Layer (**$V_{CC}/2$**). Output. The **$V_{CC}/2$** pin provides a reference voltage for the ISO low-speed physical layer: • 2.38V DC (minimum) to 2.60V DC (maximum) (V_{CC} = +5.0V; $I_{OUT} \leq 75$ µA) • 1.46V DC (minimum) to 1.688V DC (maximum) (V_{CC} = +3.3V; $I_{OUT} \leq 75$ µA) This pin only functions as **$V_{CC}/2$** when the MUX bit of the CPU Interface Register (02H) is 1.
V_{SS1}	V_{SS1}	23	17	Ground, Digital (**V_{SS1}**). This pin provides the digital ground (0V) for the IA82527. It must be connected to a V_{SS} board plane.
V_{SS2}	V_{SS2}	20	14	Ground, Analog (**V_{SS2}**). This pin provides the ground (0V) for the IA82527 analog comparator. It must be connected to a V_{SS} board plane.
wr_n	wr_n/wrl_n/r-w_n	7	1	**wr**ite. Input. Active Low. Mode 0. When **wr_n** is asserted (low), it signals a write cycle.

Table 3. Pin/Signal Descriptions *(Continued)*

Signal	Pin			Description
	Name	PLCC	PQFP	
wrh_n	wrh_n/p2.7	10	4	**wr**ite **h**igh byte. Input. Active Low. Mode 1. When **wrh_n** is asserted (low), it signals a write cycle for the high byte of data (bits 15–8).
wrl_n	wr_n/wrl_n/r-w_n	7	1	**wr**ite **l**ow byte. Input. Active Low. Mode 1. When **wrl_n** is asserted (low), it signals a write cycle for the low byte of data (bits 7–0).
xtal1	xtal1	18	12	Crystal (**xtal**) **1**. Input. The **xtal1** pin is the input connection for an external crystal that drives the IA82527 internal oscillator. (When an external crystal is used, it is connected between this pin and the **xtal2** pin—see next table entry.) If an external oscillator or clock source is used to drive the IA82527 instead of a crystal, the **xtal1** pin is the input for this clock source.
xtal2	xtal2	19	13	Crystal (**xtal**) **2**. Output (push-pull). The **xtal2** pin is the output connection for an external crystal that drives the IA82527 internal oscillator. (When an external crystal is used, it is connected between this pin and the **xtal1** pin—see previous table entry.) If an external oscillator or clock source is used to drive the IA82527 instead of a crystal, **xtal2** must be left unconnected (i.e., must be floated). Additionally, the **xtal2** output must not be used as a clock source for other system components.

3. Maximum Ratings, Thermal Characteristics, and DC Parameters

For the Innovasic Semiconductor IA82527 Serial Communications Controller, the absolute maximum ratings, thermal characteristics, and DC parameters are provided in Tables 4 through 6, respectively.

Additionally, the DC parameters of the ISO Physical Layer are provided in Table 7.

Table 4. Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	−55°C to +150°C
Case Temperature under Bias	−40°C to +125°C
Supply Voltage with Respect to V_{ss}	−0.3V to +7.0V
Voltage on Pins other than Supply with Respect to V_{ss}	−0.3V to V_{DD} +0.3V

Table 5. Thermal Characteristics

Symbol	Characteristic	Value	Units
T_A	Ambient Temperature	-40°C to 125°C	°C
P_D	Power Dissipation	MHz × ICC × V/1000	W
Θ_{Ja}	44-Pin PLCC Package	30	°C/W
	44-Pin PQFP Package	38.4	
T_J	Average Junction Temperature	$T_A + (P_D \times \Theta_{Ja})$	°C