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IA8044/IA8344
SDLC Communications Controller
Data Sheet

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1.   Introduction

The Innovasic Semiconductor IA8044 and IA8344 are "plug-and-play" drop-in replacements and are form, fit, and function compatible parts to the Intel® 8044 and 8344 (see Chapter 4, Innovasic/Intel Part Number Cross-Reference Tables). These devices are produced using Innovasic's Managed IC Lifetime Extension System (MILES™). This cloning technology, which produces replacement ICs beyond simple emulations, ensures complete compatibility with the original device, including any "undocumented features." Additionally, the MILES™ process captures the clone design in such a way that production of the clone can continue even as silicon technology advances. The IA8044 and IA8344 replace the obsolete Intel 8044 and 8344, allowing users to retain existing board designs, software compilers/assemblers, and emulation tools—thus avoiding expensive redesign efforts.

The IA8044 and IA8344 are Fast Single-Chip 8-Bit Microcontrollers with an integrated SDLC/HDLC serial interface controller. They are fully functional 8-Bit Embedded Controllers that execute all ASM51 instructions and have the same instruction set as the Intel 80C51. The IA8044 and IA8344 can access the instructions from two types of program memory, serve software and hardware interrupts, and provide interface for serial communications and a timer system. The IA8044 and IA8344 are fully compatible with the Intel® 8X44 series.

This data sheet documents all necessary engineering information about the IA8044 and IA8344 including functional and I/O descriptions, electrical characteristics, and applicable timing.

1.1   Features

- Form, fit, and function compatible with the Intel 8044 and 8344
- Packaging options available in both leaded and RoHS versions:
    - 40-Pin Plastic Dual In-Line Package (PDIP) (see IA8044 40-Lead PDIP Package Diagram)
    - 44-Pin Plastic Leaded Chip Carrier (PLCC) (see IA8344 44-Pin PLCC Package Diagram)

- 8-bit control unit (see Functional Block Diagram)
- 8-bit arithmetic-logic unit with 16-bit multiplication and division
- 12-MHz clock
- Four 8-bit input/output ports
- Two 16-bit timer/counters
- Serial interface unit with SDLC/HDLC compatibility
- 2.4-Mbps maximum serial data rate
- Two-level priority interrupt system
- 5 interrupt sources
- Internal clock prescaler and phase generator
- 192 bytes of read/write data memory space
- 64-Kbyte external program memory space

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- 64-Kbyte external data memory space
- 4-Kbyte internal ROM (IA8044 only)

1.2 Variants

- IA8044
  - 4-Kbyte internal ROM with R0117 version 2.3 firmware
  - 192-byte internal RAM
  - 64-Kbyte external program and data space

- IA8344
  - 192-byte internal RAM
  - 64-Kbyte external program and data space

2. Packaging, Pin Descriptions, and Physical Dimensions

The Innovasic Semiconductor IA8044 and IA8344 serial controllers are available in the following packages:

- 40-Pin Plastic Dual In-Line Package (PDIP), equivalent to original PDIP package (see Physical Package Dimensions)

- 44-Lead Plastic Leaded Chip Carrier (PLCC), equivalent to original PLCC package (see Physical Package Dimensions)

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2.1   PDIP Package

The pinout for the IA8044 and IA8344 40 PDIP package is as shown in Figure 1. Although Figure 1 shows "IA8X44," each device has a complete part number marked on its face (see Chapter 8, Innovasic/Intel Part Number Cross-Reference Tables). The corresponding pinout is provided in Table 1.

P1.0	(1)	(40) VCC
P1.1	(2)	(39) P0.0 (AD0)
P1.2	(3)	(38) P0.1 (AD1)
P1.3	(4)	(37) P0.2 (AD2)
P1.4	(5)	(36) P0.3 (AD3)
P1.5	(6)	(35) P0.4 (AD4)
(RTS) P1.6	(7)	(34) P0.5 (AD5)
(CTS) P1.7	(8)	(33) P0.6 (AD6)
RST	(9)	(32) P0.7 (AD7)
(RXD) P3.0	(10)	(31) EA
(TXD) P3.1	(11)	(30) ALE
(INT0) P3.2	(12)	(29) PSEN
(INT1) P3.3	(13)	(28) P2.7 (A15)
(T0) P3.4	(14)	(27) P2.6 (A14)
(SCLK/T1) P3.5	(15)	(26) P2.5 (A13)
(WR) P3.6	(16)	(25) P2.4 (A12)
(RD) P3.7	(17)	(24) P2.3 (A11)
XTAL2	(18)	(23) P2.2 (A10)
XTAL1	(19)	(22) P2.1 (A9)
VSS	(20)	(21) P2.0 (A8)

IA8X44 PDIP
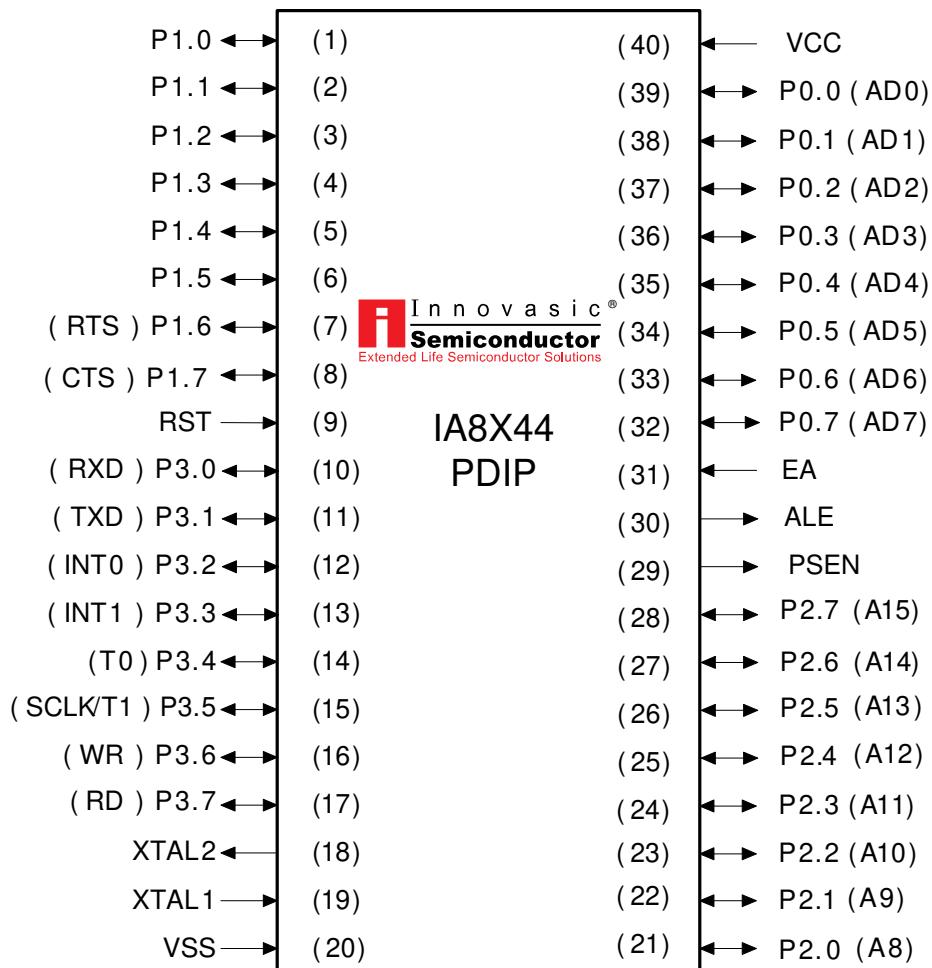
Figure 1. IA8044 and IA8344 40-Lead PDIP Package Diagram

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Table 1. IA8044 and IA8344 40-Lead PDIP Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	P1.0	11	P3.1 (TXD)	21	P2.0 (A8)	31	EA
2	P1.1	12	P3.2 (INT0)	22	P2.1 (A9)	32	P0.7 (AD7)
3	P1.2	13	P3.3 (INT1)	23	P2.2 (A10)	33	P0.6 (AD6)
4	P1.3	14	P3.4 (T0)	24	P2.3 (A11)	34	P0.5 (AD5)
5	P1.4	15	P3.5 (SCLK/T1)	25	P2.4 (A12)	35	P0.4 (AD4)
6	P1.5	16	P3.6 (WR)	26	P2.5 (A13)	36	P0.3 (AD3)
7	P1.6 (RTS)	17	P3.7 (RD)	27	P2.6 (A14)	37	P0.2 (AD2)
8	P1.7 (CTS)	18	XTAL2	28	P2.7 (A15)	38	P0.1 (AD1)
9	RST	19	XTAL1	29	PSEN	39	P0.0 (AD0)
10	P3.0 (RXD)	20	VSS	30	ALE	40	VCC

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2.2   PDIP Physical Dimensions

The physical dimensions for the 40 PDIP are as shown in Figure 2.

Legend:

Symbol	Typical (in Inches)
A	0.155
A1	0.010
B	0.018
B1	0.050
C	0.010
D	2.055
e	0.100
E	0.600
E1	0.545
eB	0.650
L	0.130
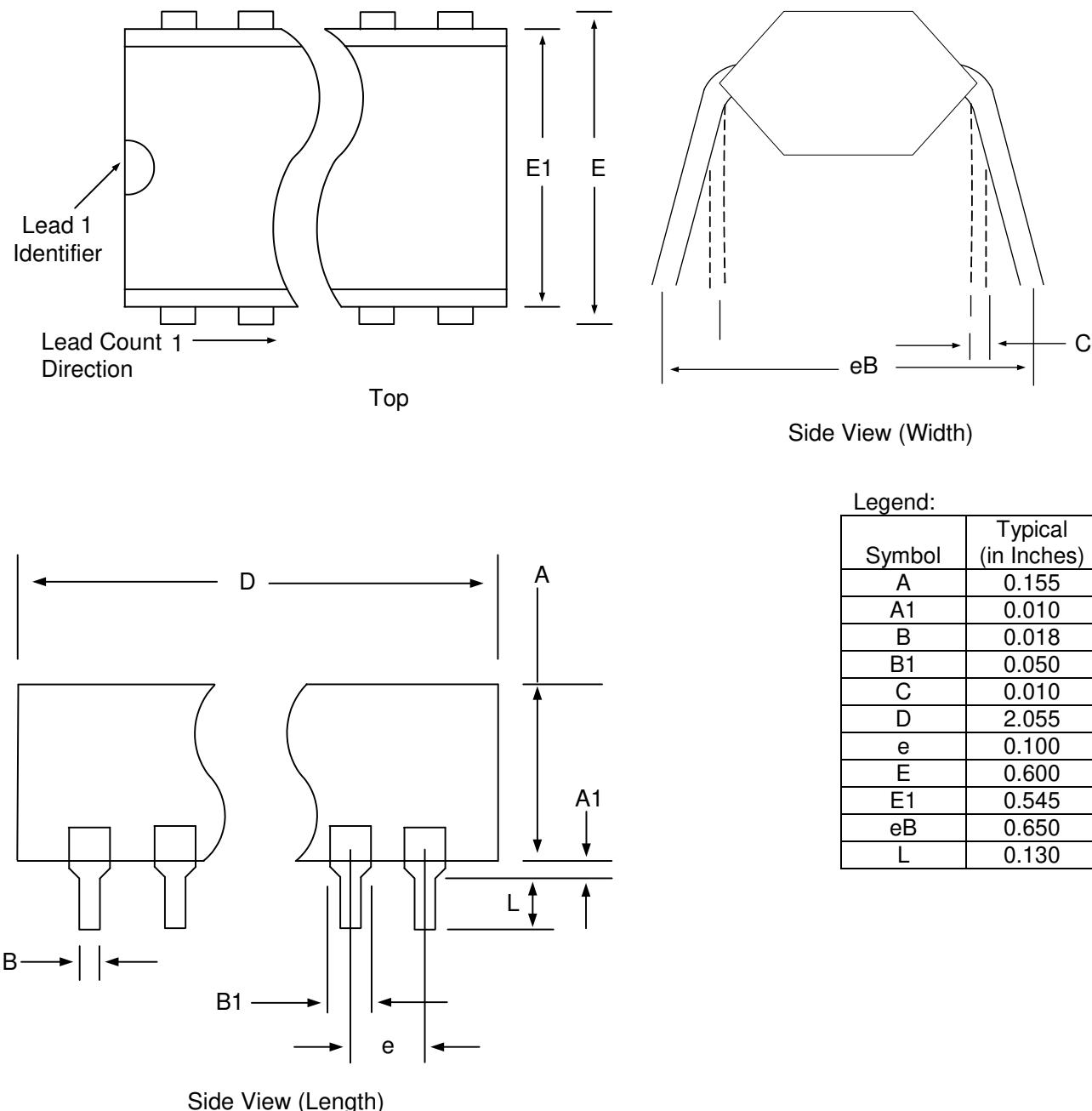
Figure 2. PDIP Physical Package Dimensions

2.3   PLCC Package

The pinout for the IA8044 and IA8344 44 PLCC package is as shown in Figure 3. Although
Figure 3 shows "IA8X44," each device has a complete part number marked on its face (see
Chapter 8, Innovasic/Intel Part Number Cross-Reference Tables). The corresponding pinout is
provided in Table 2.

Figure 3. IA8044 and IA8344 44-Pin PLCC Package Diagram

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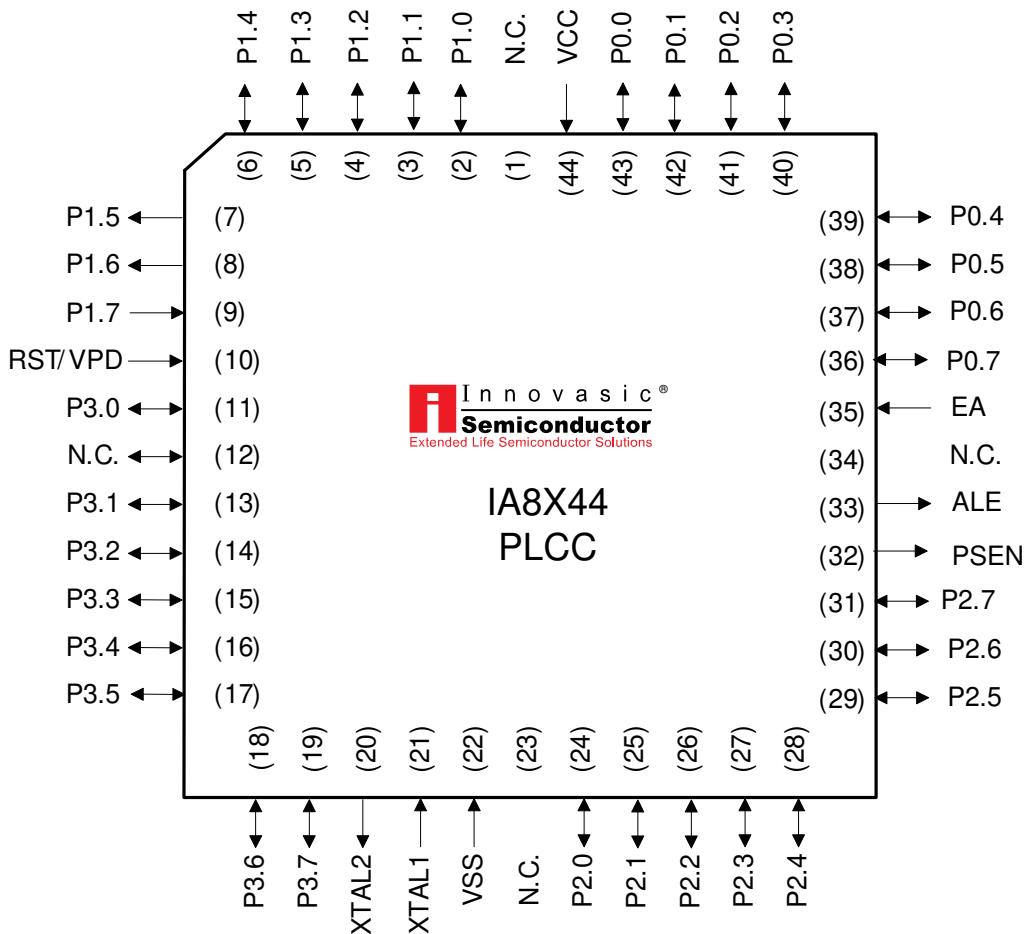
Table 2. IA8044 and IA8344 44-Pin PLCC Pin Listing

Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	N.C.	12	N.C.	23	N.C.	34	N.C.
2	P1.0	13	P3.1	24	P2.0	35	EA
3	P1.1	14	P3.2	25	P2.1	36	P0.7
4	P1.2	15	P3.3	26	P2.2	37	P0.6
5	P1.3	16	P3.4	27	P2.3	38	P0.5
6	P1.4	17	P3.5	28	P2.4	39	P0.4
7	P1.5	18	P3.6	29	P2.5	40	P0.3
8	P1.6	19	P3.7	30	P2.6	41	P0.2
9	P1.7	20	XTAL2	31	P2.7	42	P0.1
10	RST/VPD	21	XTAL1	32	PSEN	43	P0.0
11	P3.0	22	VSS	33	ALE	44	VCC

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2.4   PLCC Physical Dimensions

The physical dimensions for the 44 PLCC are as shown in Figure 4.
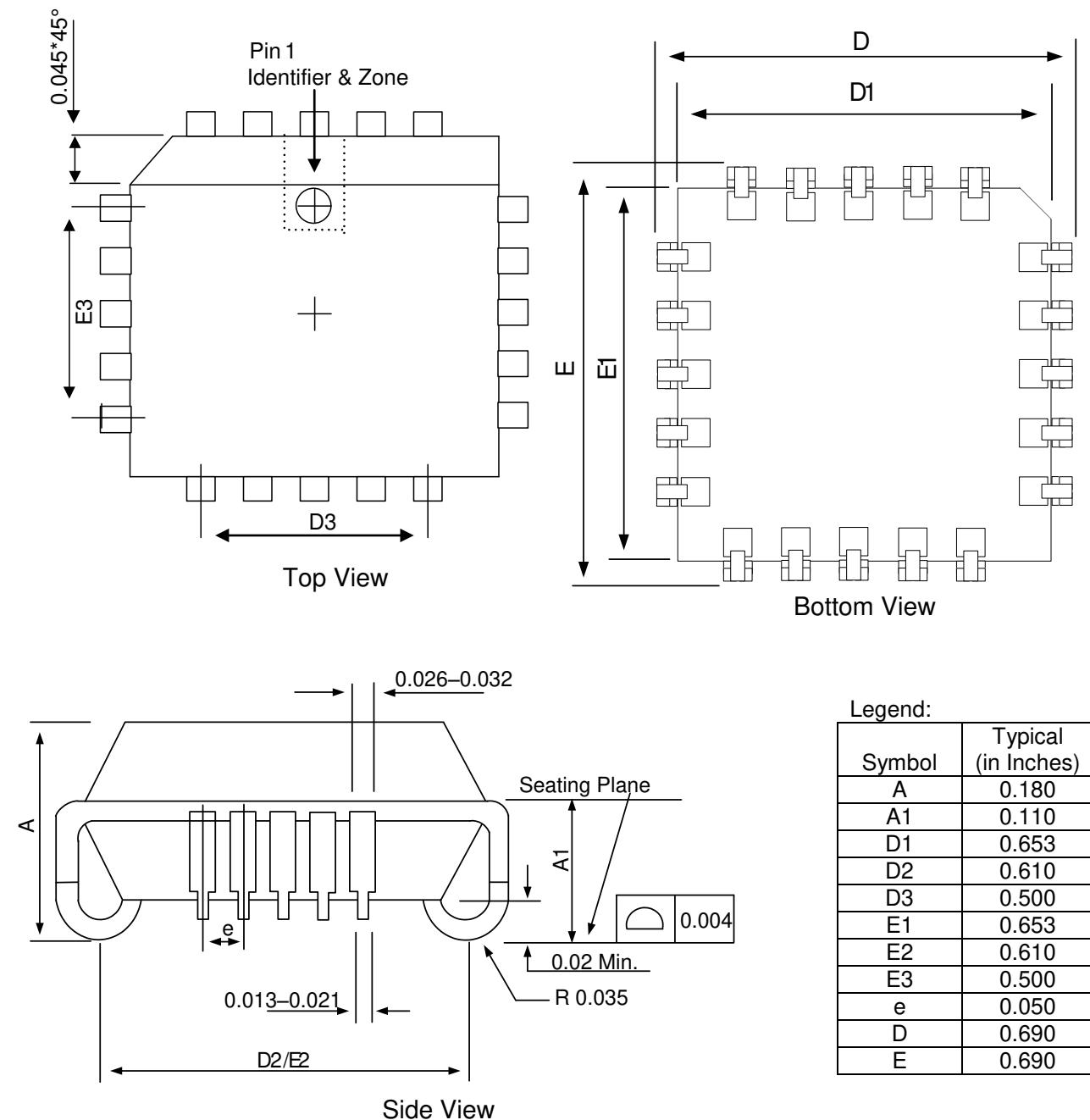
Figure 4. PLCC Physical Package Dimensions

Legend:

Symbol	Typical (in Inches)
A	0.180
A1	0.110
D1	0.653
D2	0.610
D3	0.500
E1	0.653
E2	0.610
E3	0.500
e	0.050
D	0.690
E	0.690

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3. Maximum Ratings and DC Characteristics

The IA8044/IA8344 absolute maximum ratings and DC characteristics are provided in Tables 3 and 4, respectively.

Table 3. IA8044 and IA8344 Absolute Maximum Ratings

Parameter	Rating
Ambient temperature under bias	−40°C to +85°C
Storage temperature	−40°C to +150°C
Power supply (V_{DD})	−0.3 to +6VDC
Voltage on any pin to VSS	−0.3 to (V_{DD} +0.3)[a]
Power dissipation	2W

[a]This device does not contain EPROM or its related programming circuitry. Therefore, this limit must be adhered to especially for input pin EA, which is used as the programming voltage pin in the Intel device. Exceeding the listed maximum voltage will cause damage to the device.

Table 4. IA8044 and IA8344 DC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIL	Input Low Voltage	–	–	0.8	V
VIH	Input High Voltage	2.0	–	–	V
VOL	Output Low Voltage (IOL= 4mA)	–	–	0.4	V
VOH	Output High Voltage (IOH= 4mA)	3.5	–	–	V
RPU	Pull-Up Resistance (Ports 1, 2, 3)	–	50	–	KW
RPD	Pull-Down Resistance (RST)	–	50	–	KW
IIL	Input Low Current (Ports 1, 2, 3)	−200	–	1	µA
IIL1	Input Low Current (PO, EA)	−1	–	1	µA
IIH	Input High Current (RST)	−1	–	200	µA
IIH1	Input High Current (PO, EA)	−1	–	1	µA
IOZ	Tri-state Leakage Current (Port 0)	−10	–	10	µA
ICC	Power Supply Current (@ 12 MHz)	–	–	50	mA
CIO	Pin Capacitance	–	4	–	pF

4. Functional Description

4.1 Functional Block Diagram

A functional block diagram of the IA8044 and IA8344 is shown in Figure 5. Descriptions of the functional modules are provided in the following subsections.

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I/O for Memory, SIU, DMA, Interrupts, and Timers
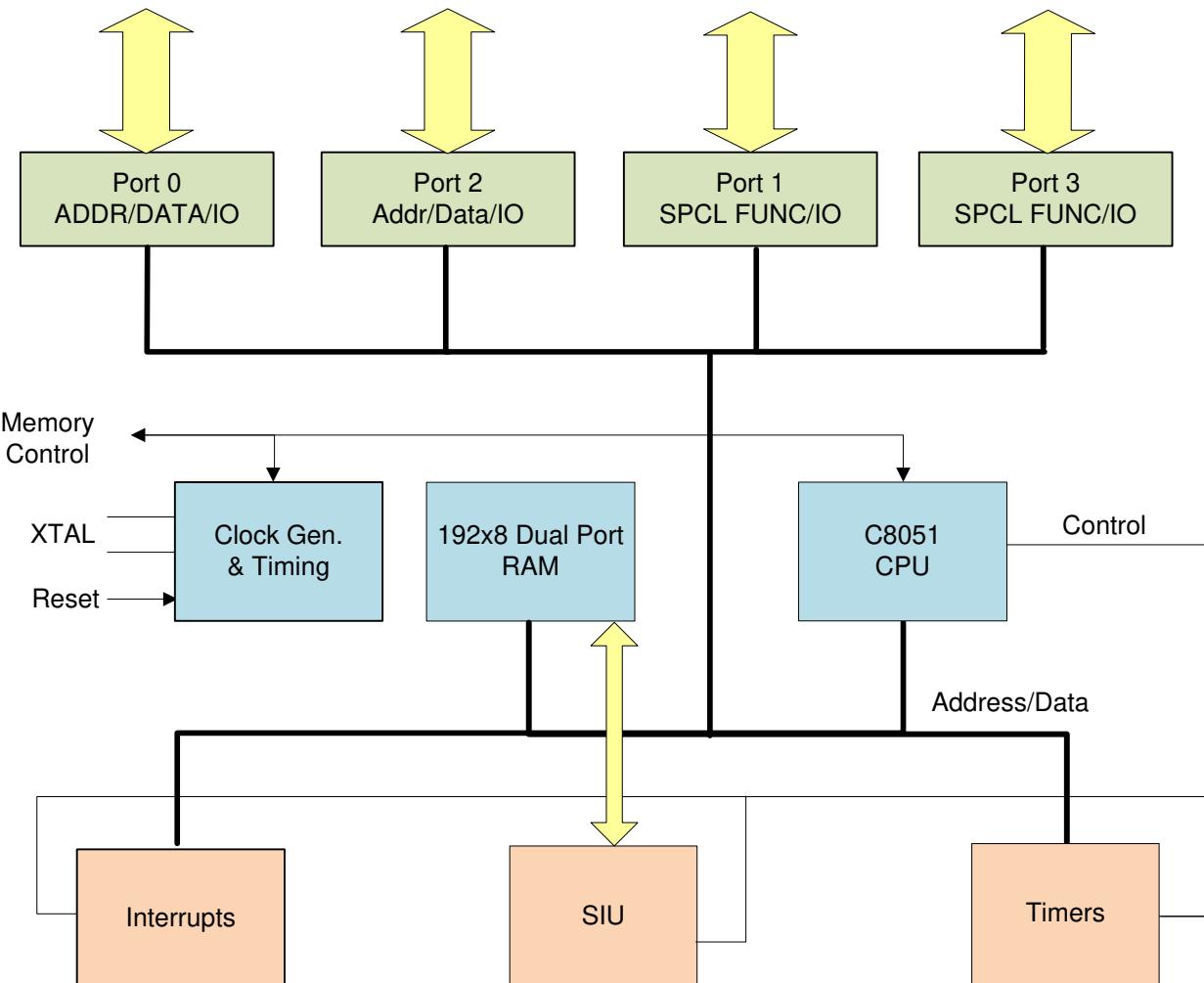
Figure 5. Functional Block Diagram

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4.2 Input/Output Characteristics

Table 5 describes the I/O characteristics for each signal on the IC. The signal names correspond to those on the pinout diagrams provided**.** The table provides the I/O description of the IA8044 and the IA8344.

Table 5. Input/Output Characteristics of IC Signals

| Name	Type	Description
RST	I	Reset—This pin will cause the chip to reset when held high for two machine cycles while the oscillator is running.
ALE	O	Address Latch Enable—Used to latch the address on the falling edge for external memory accesses.
PSEN	O	Program Store Enable—When low, acts as an output enable for external program memory.
EA	I	External Access—When held low, EA will cause the IA8044/IA8344 to fetch instructions from external memory.
P0.7–P0.0	I/O	Port 0—8-bit I/O port and low order multiplexed address/data byte for external accesses.
P1.7–P1.0	I/O	Port 1—8-bit I/O port. Two bits have alternate functions, P1.6 (RTS) and P1.7 (CTS).
P2.7–P2.0	I/O	Port 2—8-bit I/O port. It also functions as the high order address byte during external accesses.
P3.7–P3.0	I/O	Port 3—8-bit I/O port. Port 3 bits also have alternate functions as described below. P3.0 (RXD)—Receives data input for SIU or direction control for P3.1 dependent upon data link configuration. P3.1 (TXD)—Transmits data output for SIU or data input/output dependent upon data link configuration. Also enables diagnostic mode when cleared. P3.2 (INT0)—Interrupt 0 input or gate control input for Counter 0. P3.3 (INT1)—Interrupt 1 input or gate control input for Counter 1. P3.4 (T0)—Input to Counter 0. P3.5 (SCLK/T1)—SCLK input to SIU or input to Counter 1. P3.6 (WR)—External memory write signal. P3.7 (RD)—External memory read signal.
XTAL1	I	Crystal Input 1—Connects to VSS when external clock is used on XTAL2. May be connected to a crystal (with XTAL2) or may be driven directly with a clock source (XTAL2 not connected).
XTAL2	O	Crystal Input 2—May be connected to a crystal (with XTAL1) or may be driven directly with an inverted clock source (XTAL1 tied to ground).
VSS	P	Ground.
VCC	P	+5V power.

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4.3   Memory Organization

4.3.1   Program Memory

Program Memory includes interrupt and Reset vectors. The interrupt vectors are spaced at 8-byte intervals, starting from 0003H for External Interrupt 0.

Table 6. Reset Vectors

Location	Service
0003H	External Interrupt 0
000BH	Timer 0 overflow
0013H	External Interrupt 1
001BH	Timer 1 overflow
0023H	SIU Interrupt

These locations may be used for program code, if the corresponding interrupts are not used (disabled). The program memory space is 64K, from 0000H to FFFFH. The lowest 4K of program code (0000H to 0FFFH) can be fetched from external or internal program memory. This selection is made by strapping pin "EA" (External Address) to GND or VCC. If during reset "EA" is held low, all the program code is fetched from external memory. If during reset "EA" is held high, the lowest 4K of program code (0000H to 0FFFH) is fetched from internal memory (ROM). Program memory addresses above 4K (0FFFH) will cause the program code to be fetched from external memory regardless of the setting of "EA."

4.3.2   External Data Memory

The IA8044/IA8344 Microcontroller core incorporates the Harvard architecture, with separate code and data spaces. The code from external memory is fetched by "psen" strobe, while data is read from RAM by Bit [7] of P3 (read strobe) and written to RAM by Bit [6] of P3 (write strobe). The External Data Memory space is active only by addressing through use of the MOVX instruction and the 16-bit Data Pointer Register (DPTR). A smaller subset of external data memory (8-bit addressing) may be accessed by using the MOVX instruction with register indexed addressing.

4.3.3   Internal Data Memory

As presented in Figure 6, the Internal Data Memory address is always one byte wide. The memory space is 192 bytes large (00H to BFH), and can be accessed by either direct or indirect addressing. The special function registers (SFRs) occupy the upper 128 bytes. This SFR area is available only by direct addressing. Internal memory that overlaps the SFR address space is only accessible by indirect addressing.

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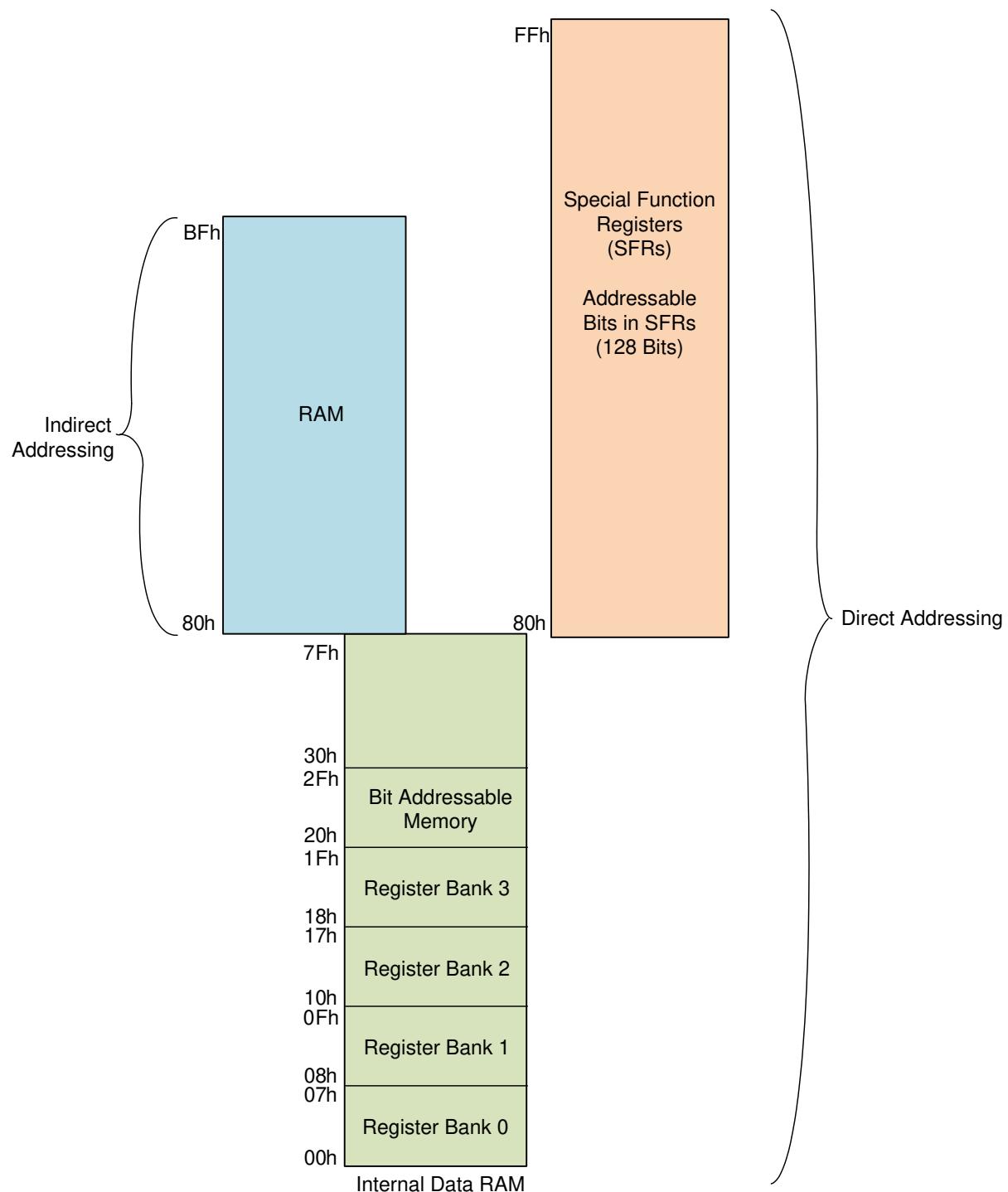
Figure 6. Internal Data Memory Addresses 00h to FFh

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4.3.4   Bit Addressable Memory

Both the internal RAM and the SFRs have locations that are bit addressable in addition to the byte addressable locations (see Tables 7 and 8).

Table 7. SFR Bit Addressable Locations

Byte Address	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]	Register
F0h	F7h	F6h	F5h	F4h	F3h	F2h	F1h	F0h	B
E0h	E7h	E6h	E5h	E4h	E3h	E2h	E1h	E0h	ACC
D8h	DFh	DEh	DDh	DCh	DBh	DAh	D9h	D8h	NSNR
D0h	D7h	D6h	D5h	D4h	D3h	D2h	D1h	D0h	PSW
C8h	CFh	CEh	CDh	CCh	CBh	CAh	C9h	C8h	STS
B8h	–	–	–	BCh	BBh	BAh	B9h	B8h	IP
B0h	B7h	B6h	B5h	B4h	B3h	B2h	B1h	B0h	P3
A8h	AFh	–	–	ACh	ABh	AAh	A9h	A8h	IE
A0h	A7h	A6h	A5h	A4h	A3h	A2h	A1h	A0h	P2
90h	97h	96h	95h	94h	93h	92h	91h	90h	P1
88h	8Fh	8Eh	8Dh	8Ch	8Bh	8Ah	89h	88h	TCON
80h	87h	86h	85h	84h	83h	82h	81h	80h	P0

Table 8. Internal RAM Bit Addressable Locations

Byte Address	Bit [7]	Bit [6]	Bit [5]	Bit [4]	Bit [3]	Bit [2]	Bit [1]	Bit [0]
30h-BFh	Upper Internal RAM Locations							
2Fh	7Fh	7Eh	7Dh	7Ch	7Bh	7Ah	79h	78h
2Eh	77h	76h	75h	74h	73h	72h	71h	70h
2Dh	6Fh	6Eh	6Dh	6Ch	6Bh	6Ah	69h	68h
2Ch	67h	66h	65h	64h	63h	62h	61h	60h
2Bh	5Fh	5Eh	5Dh	5Ch	5Bh	5Ah	59h	58h
2Ah	57h	56h	55h	54h	53h	52h	51h	50h
29h	4Fh	4Eh	4Dh	4Ch	4Bh	4Ah	49h	48h
28h	47h	46h	45h	44h	43h	42h	41h	40h
27h	3Fh	3Eh	3Dh	3Ch	3Bh	3Ah	39h	38h
26h	37h	36h	35h	34h	33h	32h	31h	30h
25h	2Fh	2Eh	2Dh	2Ch	2Bh	2Ah	29h	28h
24h	27h	26h	25h	24h	23h	22h	21h	20h
23h	1Fh	1Eh	1Dh	1Ch	1Bh	1Ah	19h	18h
22h	17h	16h	15h	14h	13h	12h	11h	10h
21h	0Fh	0Eh	0Dh	0Ch	0Bh	0Ah	09h	08h
20h	07h	06h	05h	04h	03h	02h	01h	00h
18h-1Fh	Register Bank 3							
10h-17h	Register Bank 2							
08h-0Fh	Register Bank 1							
00h-07h	Register Bank 0							

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4.4   Special Function Registers

Table 9 presents the SFRs of the IA8044 and IA8344.

Table 9. Special Function Registers

Symbol	Register Description	Byte Address (Hex)	Bit Addresses (Hex) (MSB–LSB)
ACC	Accumulator	E0h	E7h–E0h
B	B register	F0h	F7h–F0h
PSW	Program Status Word	D0h	D7h–D0h
SP	Stack Pointer	81h	–
DPH	Data Pointer High Byte	82h	–
DPL	Data Pointer Low Byte	83h	–
P0	Port 0	80h	87h–80h
P1	Port 1	90h	97h–90h
P2	Port 2	A0h	A7h–A0h
P3	Port 3	B0h	B7h–B0h
IP	Interrupt Priority	B8h	BCh–B8h
IE	Interrupt Enable	A8h	AFh,ACh–A8h
TMOD	Timer/Counter Mode	89h	–
TCON	Timer/Counter Control	88h	8Fh–88h
TH0	Timer/Counter 0 high byte	8Ch	–
TL0	Timer/Counter 0 low byte	8Ah	–
TH1	Timer/Counter 1 high byte	8Dh	–
TL1	Timer/Counter 1 low byte	8Bh	–
SMD	Serial Mode	C9h	–
STS	SIU Status and Command	C8h	CFh–C8h
NSNR	SIU Send/Receive Count	D8h	DFh–D8h
STAD	SIU Station Address	CEh	–
TBS	Transmit Buffer Start Address	DCh	–
TBL	Transmit Buffer Length	DBh	–
TCB	Transmit Control Byte	DAh	–
RBS	Receive Buffer Start Address	CCh	–
RBL	Receive Buffer Length	CBh	–
RFL	Receive Field Length	CDh	–
RCB	Receive Control Byte	CAh	–
DMA CNT	DMA Count	CFh	–
FIFO	FIFO contents (3 bytes)	DF,DE,DDh	–
SIUST	SIU State Counter	D9h	–

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4.5   Ports

Ports P0, P1, P2, and P3 are SFRs. The contents of the SFR can be observed on corresponding pins on the chip. Writing a "1" to any of the ports causes the corresponding pin to be at high level (VCC), and writing a "0" causes the corresponding pin to be held at low level (GND).

All four ports on the chip are bi-directional. Each of them consists of a Latch (SFR P0 to P3), an output driver, and an input buffer, so the CPU can output or read data through any of these ports if they are not used for alternate purposes.

Ports P0, P1, P2, and P3 can perform some alternate functions. Ports P0 and P2 are used to access external memory. In this case, port "p0" outputs the multiplexed lower eight bits of address with "ALE" strobe high and then reads/writes eight bits of data. Port P2 outputs the higher eight bits of address. Keeping "ea" pin low (tied to GND) activates this alternate function for Ports P0 and P2.

Port P3 and P1 can perform some alternate functions. The pins of Port P3 are multifunctional. They can perform the additional functions described in Table 10.

Table 10. Additional Functions of Port P3

Pin	Symbol	Function
P3.0	RxD, I/O	In point-to-point or multipoint configurations (SMD.3 = 0) this pin is I/O and signals the direction of data flow on DATA (P3.1). In loop mode (SMD.3 = 1) and diagnostic mode this pin is RxD, Receive Data input.
P3.1	TxD, DATA	In point-to-point or multipoint configurations (SMD.3 = 0) this pin is DATA and is the transmit/receive data pin. In loop mode (SMD.3 = 1) this pin is the transmit data, TxD pin. Writing a "0" to this port buffer bit enables the diagnostic mode.
P3.2	INT0	External Interrupt 0 input. Also gate control input for Counter 0.
P3.3	INT1	External Interrupt 1 input. Also gate control input for Counter 1.
P3.4	T0	Timer/Counter 0 external input. Setting the appropriate bits in the Special Function Registers TCON and TMOD activates this function.
P3.5	T1, SCLK	Timer/Counter 1 external input. Setting the appropriate bits in the SFRs TCON and TMOD activates this function. Can also function as the external clock source for the SIU.
P3.6	WR	External Data Memory write strobe, active LOW. This function is activated by a CPU write access to External Data Memory (i.e., MOVX @DPTR, A).
P3.7	RD	External Data Memory read strobe, active LOW. This function is activated by a CPU read access from External Data Memory (i.e., MOVX A, @DPTR).
P1.6	RTS	Request To Send output, active low.
P1.7	CTS	Clear To Send input, active low.

4.6   Port Registers

4.6.1   Port 0 (P0)

Table 11 presents the values for Port 0 (P0), a general purpose, 8-bit, I/O port and multiplexed low order address and data bus with open-drain output buffers.

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Table 11. Port 0 Register

7	6	5	4	3	2	1	0
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0

4.6.2 Port 1 (P1)

Table 12 presents the values for Port 1 (P1), a general purpose, eight-bit, I/O port with pullups and auxiliary functions.

Table 12. Port 1 Register

7	6	5	4	3	2	1	0
CTS/P1.7	RTS/P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0

- Bit [7]—P1.7/Clear To Send input

- Bit [6]—P1.6/Request To Send output

- Bit [5]—P1.5

- Bit [4]—P1.4

- Bit [3]—P1.3

- Bit [2]—P1.2

- Bit [1]—P1.1

- Bit [0]—P1.0

4.6.3 Port 2 (P2)

Table 13 presents the values for Port 2, a general purpose, 8-bit, I/O port with pullups and high order address bus.

Table 13. Port 2 Register

7	6	5	4	3	2	1	0
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0

4.6.4 Port 3 (P3)

Table 14 presents the values for Port 2, a general purpose, 8-bit I/O port with pullups and auxiliary functions. Bits on this port also function as the SIU data transmit/receive I/O, external interrupt inputs, timer inputs and the read and write strobes for external memory accesses.

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