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ICB1FL03G

Smart Ballast Control IC for Fluorescent Lamp Ballasts

Industrial & Multimarket

Never stop thinking

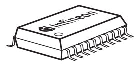
Revision History:	2009-03	V 1.02
Previous Version:	V 1.01	

Page	Subjects (major changes since last revision)

Edition 2009-03

Published by
Infineon Technologies AG
81726 Munich, Germany

Smart Ballast Control IC for Fluorescent Lamp Ballasts



PG-DSO-18-2

Product Highlights

- **Lowest Count of external Components**
- **HV-Driver with coreless Transformer Technology**
- **Improved Reliability and minimized Spread due to digital and optimized analog control functions**

Features PFC

- Discontinuous Conduction Mode PFC
- Integrated Compensation of PFC Control Loop
- Adjustable PFC Current Limitation
- Adjustable PFC Bus Voltage

Features Lamp Ballast Inverter

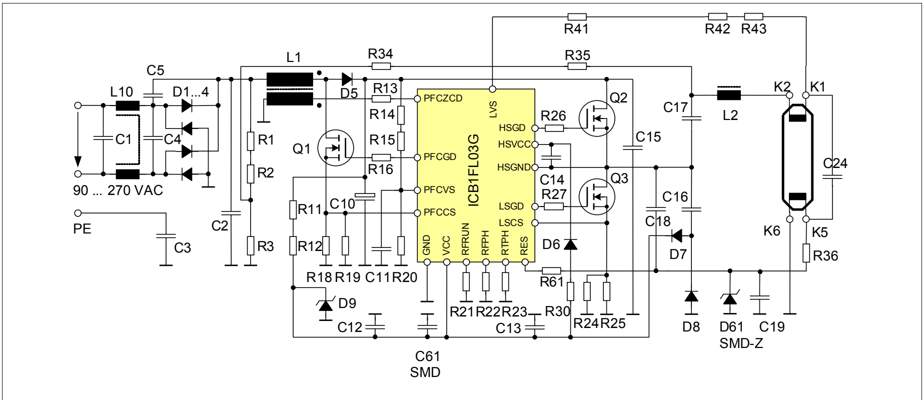
- Supports Restart after Lamp Removal and End-of-Life Detection even in serial Multi-Lamp Topologies
- End-of-Life (EOL) detected by adjustable ± Thresholds of sensed lamp voltage
- Rectifier Effect detected by ratio of ± Amplitude of Lamp Voltage
- Detection of different capacitive Mode Operations
- Adjustable Inverter Overcurrent Shutdown
- Self-adaption of Ignition Time from 40ms to 235ms
- Parameters adjustable by Resistors only
- Pb-free lead plating; RoHS compliant
- Halogen-free mould compound, WEEE compliant

Description

The Smart Ballast IC is designed to control a Fluorescent Lamp Ballast including a Discontinuous Conduction Mode Power Factor Correction (PFC), a lamp Inverter Control and a High Voltage Level Shift Half-Bridge Driver.

The application requires a minimum of external components. There are integrated low pass filters and an internal compensation for the PFC voltage loop control. Preheating time is adjustable by a single resistor only in the range between 0 and 2000ms. In the same way the preheating frequency and run frequency are set by resistors only. The control concept covers requirements for T5 lamp ballasts such as detection of end-of-life and detection of capacitive mode operation and other protection measures in serial multilamp topologies.

ICB1FL03G is easy to use and easy to design and therefore a basis for a cost effective solution for fluorescent lamp ballasts.



Type		Package
ICB1FL03G		PG-DSO-18-2

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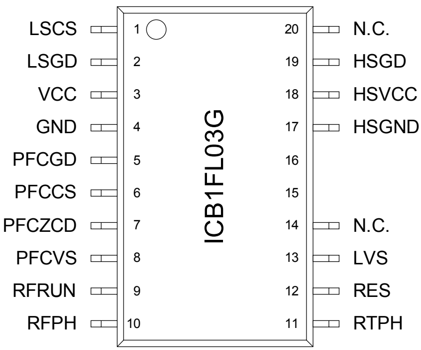
1 Pin Configuration and Description

1.1 Pin Configuration PG-DSO-18-2

Pin	Symbol	Function
1	LSCS	Low side current sense (inverter)
2	LSGD	Low side gate drive (inverter)
3	VCC	Supply voltage
4	GND	Controller ground
5	PFCGD	PFC gate drive
6	PFCCS	PFC current sense
7	PFCZCD	PFC zero current detector
8	PFCVS	PFC voltage sense
9	RFRUN	Set R for run frequency
10	RFPH	Set R for preheating frequency
11	RTPH	Set R for preheating time
12	RES	Restart after lamp removal
13	LVS	Lamp voltage sense
14	n.c.	Not connected
15	n.e.	Not existing
16	n.e.	Not existing
17	HSGND	High side ground
18	HSVCC	High side supply voltage
19	HSGD	High side gate drive
20	HSGND	High side ground



PG-DSO-18-2 (300mil)

1.2 Pin Description

LSCS (Low side current sense, Pin 1)

This pin is directly connected to the shunt resistor which is located between the Source terminal of the low-side MOSFET of the inverter and ground.

Internal clamping structures and filtering measures allow for sensing the Source current of the low-side inverter MOSFET without additional filter components. There is a first threshold of 0,8V, which provides a couple of increasing steps of frequency during ignition mode, if exceeded by the sensed current signal for a time longer than 250ns. If the sensed current signal exceeds a second threshold of 1,6V for longer than 400ns during all operating modes, a latched shut down of the IC will be the result.

LSGD (Low side gate drive, Pin 2)

The Gate of the low-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO (undervoltage lockout) and a limitation of the max. H-level at 11V during normal operation. Turning on the MOSFET softly (with reduced di_{DRAIN}/dt), the Gate drive voltage rises within 220ns from L-level to H-level. The fall time of the Gate drive voltage is less than 50ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode in parallel to a resistor in the Gate drive loop. It is recommended to use a resistor of about 15Ohm between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor. The dead time between LSGD signal and HSGD signal is 1800ns typically.

VCC (Supply voltage, Pin 3)

This pin provides the power supply of the ground related section of the IC. There is a turn-on threshold at 14V and an UVLO threshold at 10,5V. Upper supply voltage level is 17,5V. There is an internal zener diode clamping Vcc at 16V (2mA typically). The zener current is internally limited to 5mA max. For higher current levels an external zener diode is required. Current consumption during UVLO and during fault mode is less than 150µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for Gate drive and logic signal currents.

GND (Ground, Pin 4)

This pin is connected to ground and represents the ground level of the IC for supply voltage, Gate drive and sense signals.

PFCGD (PFC gate drive, Pin 5)

The Gate of the MOSFET in the PFC preconverter designed in boost topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max. H-level at 11V during normal operation. Turning on the MOSFET softly (with a reduced di_{DRAIN}/dt), the Gate drive voltage rises within 220ns from L-level to H-level. The fall time of the Gate voltage is less than 50ns in order to turn off quickly. A resistor of about 15Ω between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor is recommended.

The PFC section of the IC controls a boost converter as a PFC preconverter in discontinuous conduction mode (DCM). Typically the control starts with Gate drive pulses with an on-time of 1µs increasing up to 24µs and a off-time of 40µs. As soon as a sufficient ZCD (zero current detector) signal is available, the operating mode changes from a fixed frequent operation to an operation with variable frequency. During rated and medium load conditions we get an operation with critical conduction mode (CritCM), that means triangular shaped currents in the boost converter choke without gaps when reaching the zero level and variable operating frequency. During light load (detected by the internal error amplifier) we get an operation with discontinuous conduction mode (DCM), that means triangular shaped currents in the boost converter choke with gaps when reaching the zero level and variable operating frequency in order to avoid steps in the consumed line current.

PFCCS (PFC current sense, Pin 6)

The voltage drop across a shunt resistor located between Source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1V for longer than 260ns the PFC Gate drive is turned off as long as the ZCD (zero current detector) enables a new cycle. If there is no ZCD signal available within 40µs after turn-off of the PFC Gate drive, a new cycle is initiated from an internal start-up timer.

PFCZCD (PFC zero current detection, Pin 7)

This pin senses the point of time when the current through the boost inductor becomes zero during off-time of the PFC MOSFET in order to initiate a new cycle. The moment of interest appears when the voltage of the separate ZCD winding changes from positive to negative level which represents a voltage of zero at the inductor windings and therefore the end of current flow from lower input voltage level to higher output voltage level. There is a threshold with hysteresis, for increasing voltage a level of 1,5V, for decreasing voltage a level of 0,5V, that detects the change of inductor voltage. A resistor connected between ZCD winding and sense input limits the sink and source current of the sense pin, when the voltage of the ZCD winding exceeds the internal clamping levels (6,3V and -2,9V @ 4mA) of the IC.

If the sensed level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 40µs after turn-off of the PFC Gate drive.

PFCVS (PFC voltage sense, Pin 8)

The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for rated bus voltage is 2,5V. There are further thresholds at 0,375V (15% of rated bus voltage), 1,83V (73% of rated bus voltage) and 2,725V (109% of rated bus voltage) for detecting open control loop, undervoltage and overvoltage.

RFRUN (Set R for run frequency, Pin 9)

A resistor from this pin to ground sets the operating frequency of the inverter during run mode. Typical run frequency range is 20kHz to 100kHz. The set resistor R_{RFRUN} can be calculated based on the run frequency f_{RUN} according to the equation

$$R_{RFRUN} = \frac{5 \cdot 10^{8}\,\Omega\mathrm{Hz}}{f_{RUN}}$$

RFPH (Set R for preheating frequency, Pin 10)

A resistor from this pin to ground sets together with the resistor at pin 9 the operating frequency of the inverter during preheat mode. Typical preheat frequency range is run frequency (as a minimum) to 150kHz. The set resistor R_{RFPH} can be calculated based on the preheat frequency f_{PH} and the resistor R_{RFRUN} according to the equation:

$$R_{RFPH} = \frac{R_{RFRUN}}{\frac{f_{PH} \cdot R_{RFRUN}}{5 \cdot 10^{8}\,\Omega\mathrm{Hz}} - 1}$$

The total value of both resistors R_{RFPH} and R_{RFRUN} switched in parallel should not be less than 3,3kOhm.

RTPH (Set R for preheating time, Pin 11)

A resistor from this pin to ground sets the preheating time of the inverter during preheat mode. A set resistor range from zero to 18kOhm corresponds to a range of preheating time from zero to 2000ms subdivided in 127 steps.

RES (Restart after lamp removal, Pin 12)

A source current out of this pin via resistor and filament to ground monitors the existence of the low-side filament of the fluorescent lamp for restart after lamp removal. A capacitor from this pin directly to ground eliminates a superimposed AC voltage that is generated as a voltage drop across the low-side filament.

During typical start-up with connected filaments of the lamp a current source I_{RES3} (20µA) is active as long as Vcc> 10,5V and V_{RES}< V_{RESC1} (1,6V). An open Low-side filament is detected, when V_{RES}> V_{RESC1}. Such a condition will prevent the start-up of the IC. In addition the comparator threshold is set to V_{RESC2} (1,3V) and the current source changes to I_{RES4} (17µA). Now the system is waiting for a voltage level lower than V_{RESC2} at the RES-Pin that indicates a connected low-side filament, which will enable the start-up of the IC.

An open high-side filament is detected when there is no sink current $I_{LVSsink}$ (15µA) into the LVS-Pin before the V_{CC} start-up threshold is reached. Under these conditions the current source at the RES-Pin is I_{RES1} (41µA) as long as Vcc> 10,5V and V_{RES}< V_{RESC1} (1,6V) and the current source is I_{RES2} (34µA) when the threshold has changed to V_{RESC2} (1,3V). In this way the detection of the high-side filament is mirrored to the levels on the RES-Pin.

Finally there is a delay function implemented at the RES-Pin. When a fault condition happens e.g. by an end-of-life criteria the inverter is turned-off. In some topologies a transient AC lamp voltage may occur immediately after shut down of the Gate drives which could be interpreted as a lamp removal. In order to generate a delay for the detection of a lamp removal the capacitor at the RES-Pin is charged by the I_{RES3} (20µA) current source up to the threshold V_{RESC1} (1,6V) and discharged by an internal resistor $R_{RESdisch}$, which operates in parallel to the external sense resistor at this pin, to the threshold V_{RESC3} (0,375V). The total delay amounts to 32 of these cycles, which corresponds to a delay time between 30ms to 100ms dependent on capacitor value.

In addition this pin is applied to sense capacitive mode operation by use of a further capacitor connected from this pin to the nod of the high-side MOSFET's Source terminal and the low-side MOSFET's Drain terminal. The sense capacitor and the filter capacitor are acting as a capacitive voltage divider that allows for detecting voltage slopes versus timing sequence and therefore indicating capacitive mode operation. A typical ratio of the capacitive divider is 410V/2,2V which results in the capacitor values e.g. of 10nF and 53pF (56pF).

LVS (Lamp voltage sense, Pin 13)

Before the IC enters the softstart mode this pin has to sense a sink current above 26µA (max) which is fed via resistors from the bus voltage across the high-side filament of the fluorescent lamp in order to monitor the existence of the filament for restart after lamp removal. Together with RES (pin 12) the IC can monitor the lamp removal of totally 2 lamps in series.

During run mode the lamp voltage is sensed by the AC current fed into this pin via resistors. Exceeding one of the two thresholds of either +215µA or -215µA cycle by cycle for longer than 610µs, the interpretation of this event is a failure due to EOL1 (end-of-life). A rectifier effect (EOL2) is assumed if the ratio of the sequence of positive and negative amplitudes is above 1,15 or below 0,85 for longer than 500ms. A failure due to EOL1 or EOL2 changes the operating mode from run mode into a latched fault mode that stops the operation until a reset occurs by lamp removal or by cycle of power.

EOL1 and EOL2 require an AC current with zerocrossings at LVS-Pin for a reliable detection. A DC current at LVS-Pin results in a definite turn-off action acc. to EOL1 only if the sensed current exceeds the threshold $I_{LVSEOLDC}$= +/-175µA (typically).

If the functionality of this pin is not required it can be disabled by connecting this pin to ground.

Not Connected (Pin 14)

This pin is internally not connected.

HSGND (High side ground, Pin 17)

This pin is connected to the Source terminal of the high-side MOSFET, which is also the nod of high-side and low-side MOSFET. This pin represents the floating ground level of the high-side driver and high-side supply.

HSVCC (High side supply voltage, Pin 18)

This pin provides the power supply of the high-side ground related section of the IC. An external capacitor between pin 15 and 16 acts like a floating battery which has to be recharged cycle by cycle via high voltage diode from low-side supply voltage during on-time of the low-side MOSFET. There is an UVLO threshold with hysteresis that enables high-side section at 10,1V and disables it at 8,4V.

HSGD (High side gate drive, Pin 19)

The Gate of the high-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max. H-level at 11V during normal operation. The switching characteristics are the same as described for LSGD (pin 2). It is recommended to use a resistor of about 15Ohm between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor.

The dead time between LSGD signal and HSGD signal is 1800ns typically.

HSGND (High side ground, Pin 20)

This pin is internally connected with pin 17.

2 Block Diagram

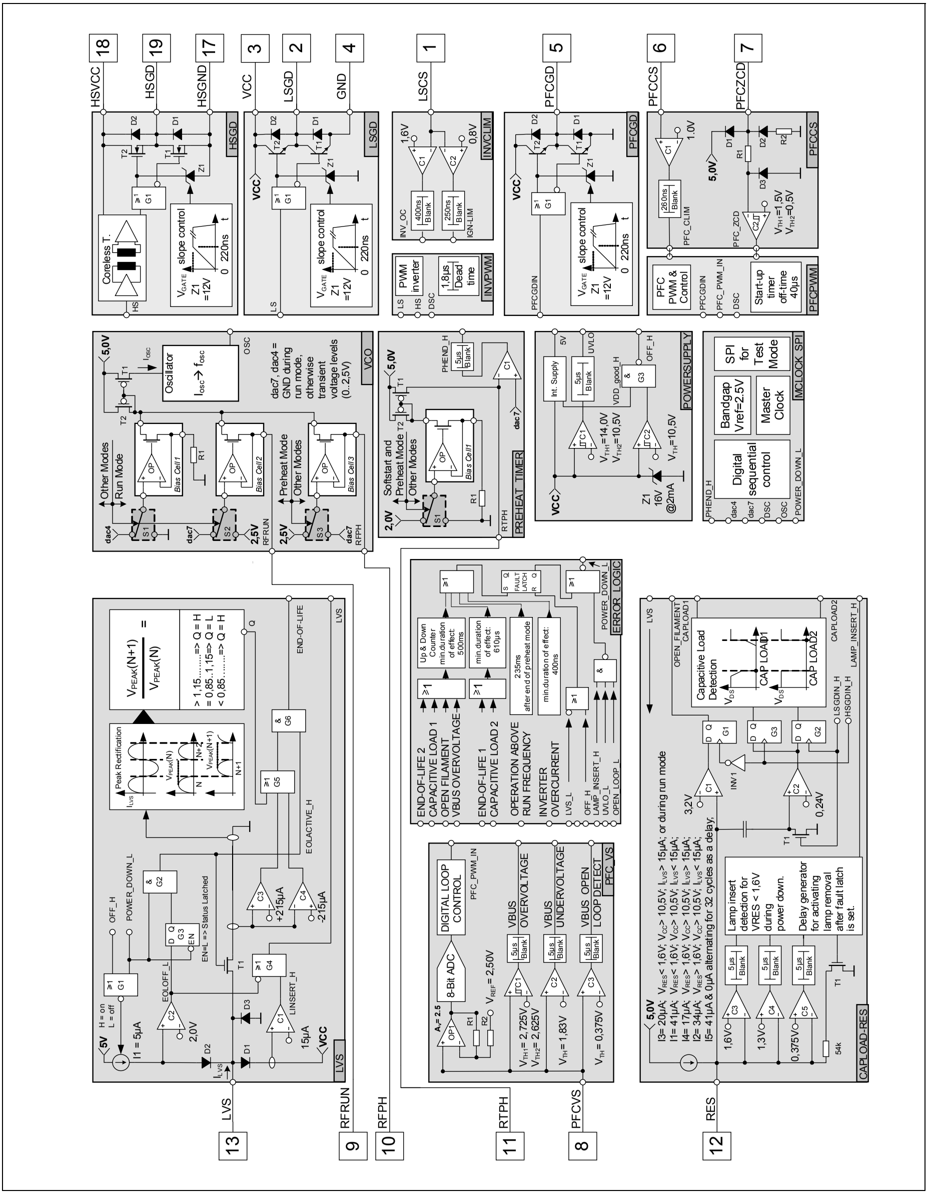


Figure 1 Simplified Blockdiagram of ICB1FL03G

3 Functional Description

3.1 Typical operating levels during start-up

The control of the ballast should be able to start the operation within less than 100ms. Therefore the current consumption of the IC is less than 150µA during UVLO. With a small start-up capacitor (about 1µF) and a power supply, that feeds within 100µs (charge pump of the inverter) the IC can cover this feature.

As long as the Vcc is less than 10,5V, the current consumption is typically 80µA. Above a Vcc voltage level of 10,5V the IC checks whether the lamp(s) are assembled by detecting a current across the filaments. The low-side filament is checked from a source current (20µA typ.) out of pin RES, that produces a voltage drop at the sense resistor, which is connected via low-side filament to ground. An open filament is detected, when the voltage level at pin RES is above 1,6V. The high-side filament (or the high-side of a series topology) is checked by a current (15µA typ.) into the LVS pin. An open high-side filament causes a higher source current (41µA / 34µA typ.) out of pin RES in order to exceed the 1,6V threshold. If the filament is not able to conduct the test current, the control circuit is disabled. The IC is enabled as soon as a sufficient current is detected across the filament or the supply voltage drops below the UVLO threshold (10,5V) e.g. by turn-off and turn-on of mains switch.

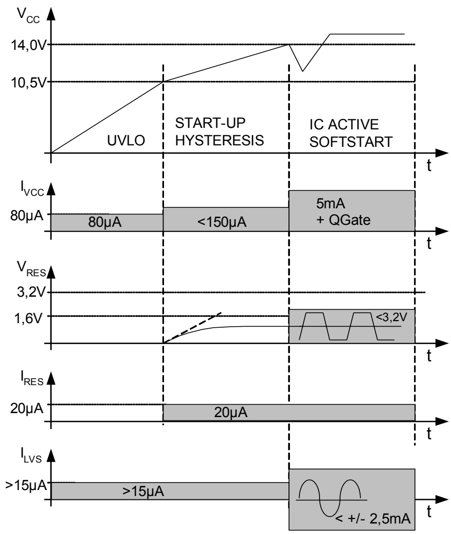


Figure 2 Progress of levels during a typical start-up.

When the previous conditions are fulfilled, and Vcc has reached the start-up threshold (14V), there is finally a check of the Bus voltage. If the level is less than 15% of rated Bus voltage, the IC is waiting in power down mode until the voltage increases. If the level is above 109% of rated Bus voltage there is no Gate drive, but an active IC. The supply voltage Vcc will fall below the UVLO threshold and a new start-up attempt is initiated.

As soon as start-up conditions are fulfilled the IC starts driving the inverter with the start-up frequency of 125kHz. Now the complete control including timers and the PFC control can be set in action. There are current limitation thresholds for PFC preconverter and ballast inverter equipped with spike filters. The PFC current limitation interrupts the on-time of the PFC MOSFET if the voltage drop at shunt resistor exceeds 1V and restarts after next input from ZCD. The inverter current limitation operates with a first threshold of 0,8V which increases the operating frequency during ignition mode if exceeded. A second threshold is provided at 1,6V that stops the whole control circuit and latches this event as a fault.

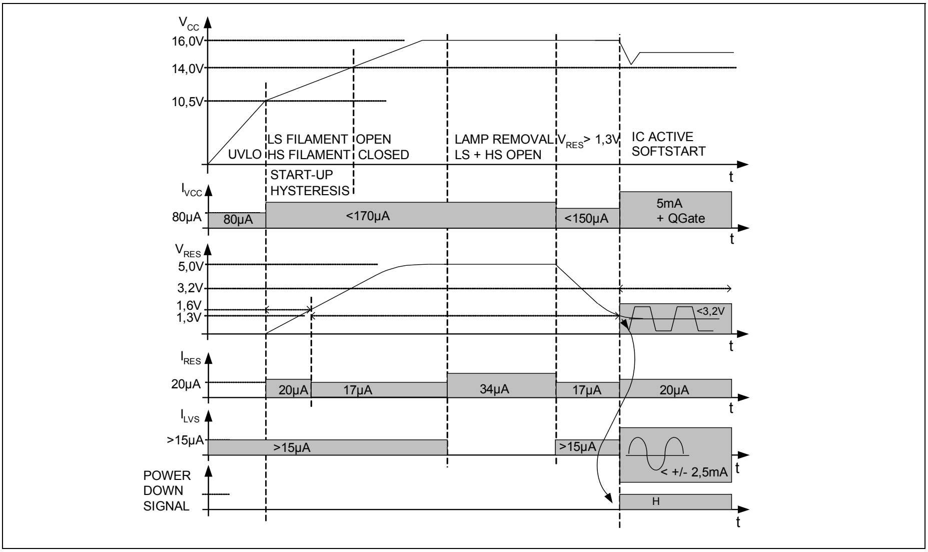


Figure 3 Start-up with LS filament broken and subsequent lamp removal.

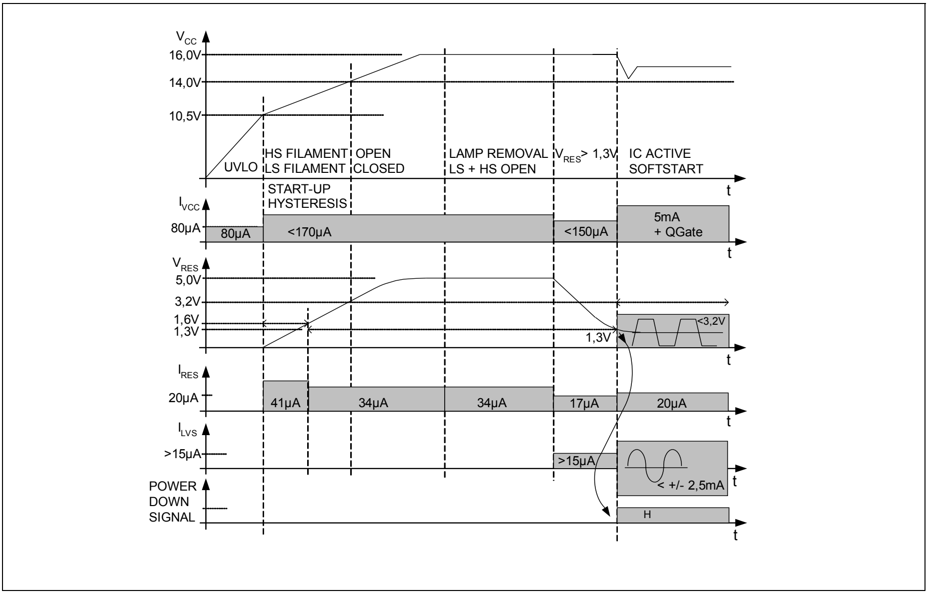


Figure 4 Start-up with HS filament broken and subsequent lamp removal.

3.2 PFC Preconverter

PFC is starting with a fixed frequent operation (ca. 25kHz), beginning with an on-time of 1µs and an off-time of 40µs. The on-time is enlarged every 400µs to a maximum on-time of 23µs. The control switches over into critical conduction mode (CritCM) operation as soon as a sufficient ZCD signal is available. There is an overvoltage threshold at 109% of rated Bus voltage that stops PFC Gate drive as long as the Bus voltage has reached a level of 105% of rated Bus voltage again. The compensation of the voltage control loop is completely integrated. The internal reference level of the Bus voltage sense (PFCVS) is 2,5V with high accuracy.

The PFC control operates in CritCM in the range of 23µs > on-time > 2,3µs. For lower loads the control operates in discontinuous conduction mode (DCM) with an on-time down to 0,5µs and an increasing off-time. With this control method the PFC preconverter covers a stable operation from 100% of load to 0,1% .

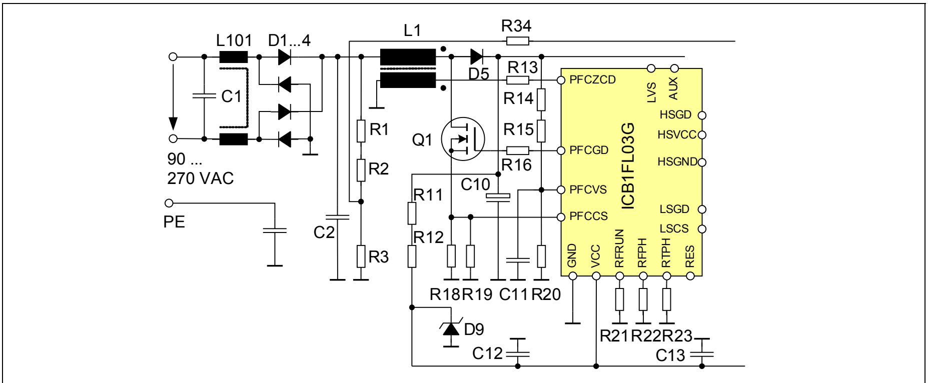


Figure 5 Circuit Diagram of the PFC preconverter section.

Overvoltage, undervoltage and open loop detection at pin PFCVS are sensed by analog comparators. The BUS voltage loop control is provided by a 8bit sigma-delta A/D-Converter with a sampling rate of 400µs and a resolution of 4mV/bit. So a range of +/- 0,5V from the reference level of 2,50V is covered. The digital error signal has to pass a digital notch filter in order to suppress the AC voltage ripple of twice of the mains frequency. A subsequent error amplifier with PI characteristic cares for stable operation of the PFC preconverter.

The zero current detection is sensed by a separate pin PFCZCD. The information of finished current flow during demagnetization is required in CritCM and in DCM as well. The input is equipped with a special filtering including a blanking of typically 500ns and is combined with a large hysteresis between the thresholds of typically 0,5V and 1,5V. In case of bad coupling between primary inductor winding and secondary ZCD-winding an additional filtering by a capacitor at ZCD pin might be necessary in order to avoid mistriggering by long lasting oscillations during switching slopes of the PFC MOSFET.

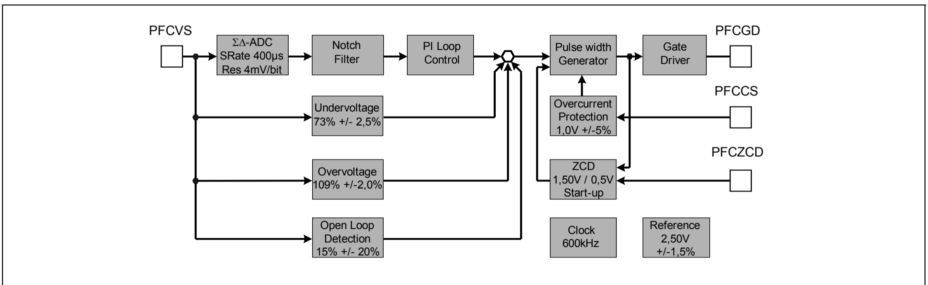


Figure 6 Structure of the mixed digital and analog control of PFC preconverter.

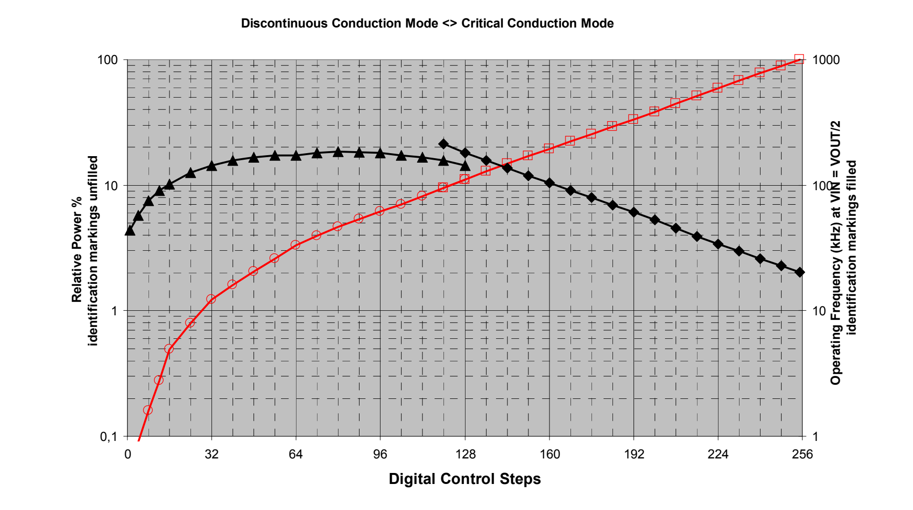


Figure 7 Relative output power and operating frequency of PFC control at VIN = VOUT /2 versus control step.

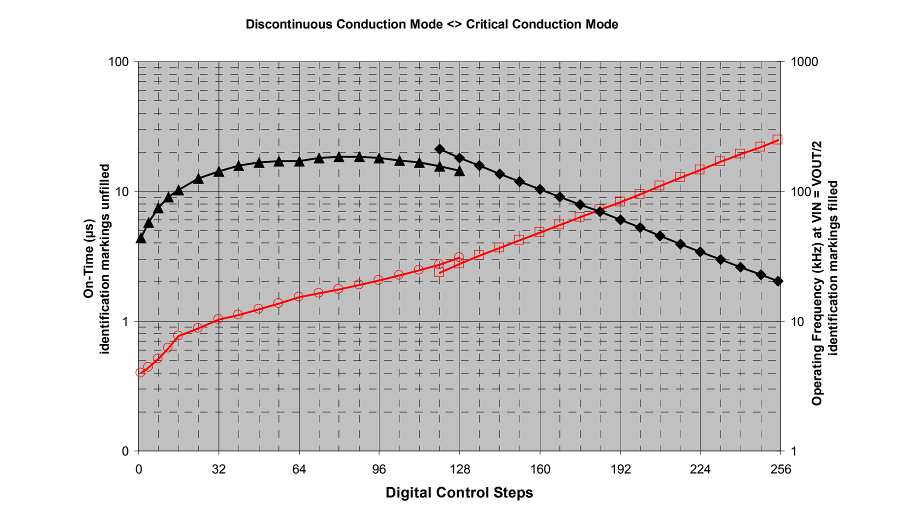


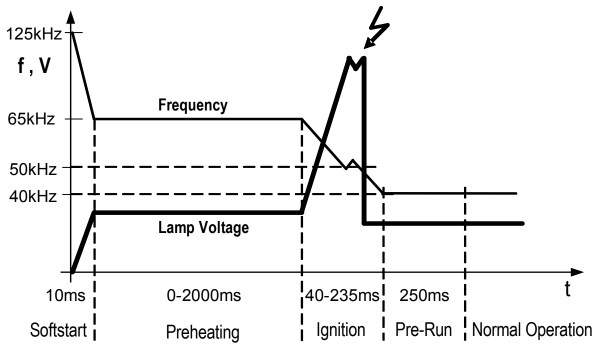
Figure 8 On-time and operating frequency of PFC control at VIN = VOUT /2 versus control step.

3.3 Typical operating levels during start-up

Within 10ms after start-up the inverter shifts operating frequency from 125kHz to the preheating frequency set by resistor at pin RFPH. Preheating time can be selected by programming resistor at RFPH pin in steps of 17ms from 0ms to 2000ms.

After preheating the operating frequency of the inverter is shifted downwards in 40ms typically to the run frequency. During this frequency shifting the voltage and current in the resonant circuit will rise when operating close to the resonant frequency with increasing voltage across the lamp. As soon as the lower current sense level (0,8V) is reached, the frequency shift downwards is stopped and increased by a couple of frequency steps in order to limit the current and the ignition voltage also. The procedure of shifting the operating frequency up and down in order to stay within the max ignition level is limited to a time frame of 235ms. If there is no ignition within this time the control is disabled and the status is latched as a fault mode.

Typical variation of operating frequency during start-up



Softstart proceeds in 15 steps à 650µs according Δf_{PH} = (120kHz - f_{PH})/ 15steps.
Ignition proceeds in 127 steps à 324µs according Δf_{IGN} = (f_{PH} - f_{RUN})/ 127steps.

Figure 9 Typical variation of operating frequency and lamp voltage during start-up.

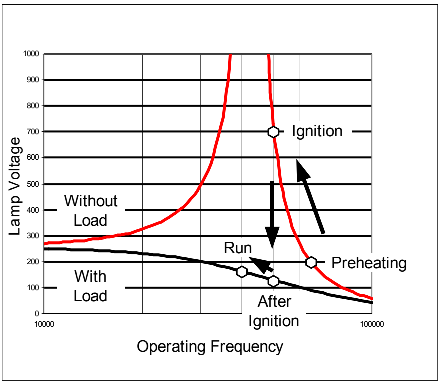


Figure 10 Typical lamp voltage versus operating frequency due to load change of the resonant circuit.

3.4 Detection of End-of-Life and Rectifier Effect

After ignition the lamp voltage breaks down to its run voltage level (typically 50Vpeak to 300Vpeak). Reaching the run frequency there follows a time period of 250ms called Pre-Run Mode, in which some of the monitoring features (EOL1, EOL2, Cap.Load1) are still disabled. In the subsequent Run Mode the End-of-life (EOL) monitoring is enabled. The event EOL1 is detected by measuring the positive and negative peak level of the lamp voltage by a current fed into the LVS pin (R41, R42, R43 in Fig. 11). If the sensed current exceeds 215µA for longer than 610µs the status end-of-life (EOL1) or the exceeding of the maximum output power is detected. In Fig. 12 the different levels of the sensed lamp voltage are illustrated.

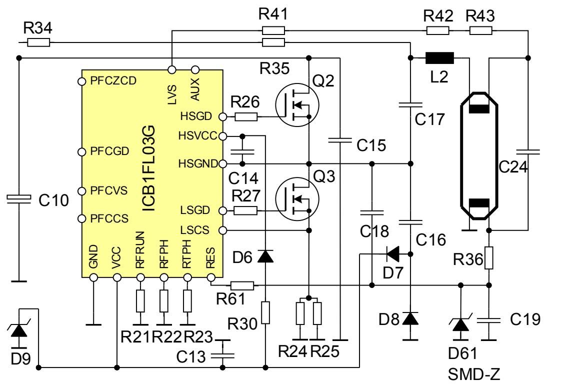


Figure 11 Circuit diagram of the lamp inverter section.

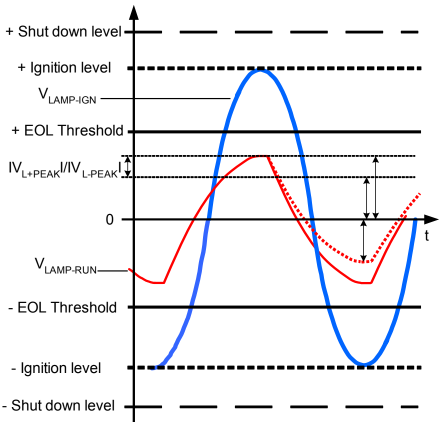


Figure 12 Sensed lamp voltage levels.

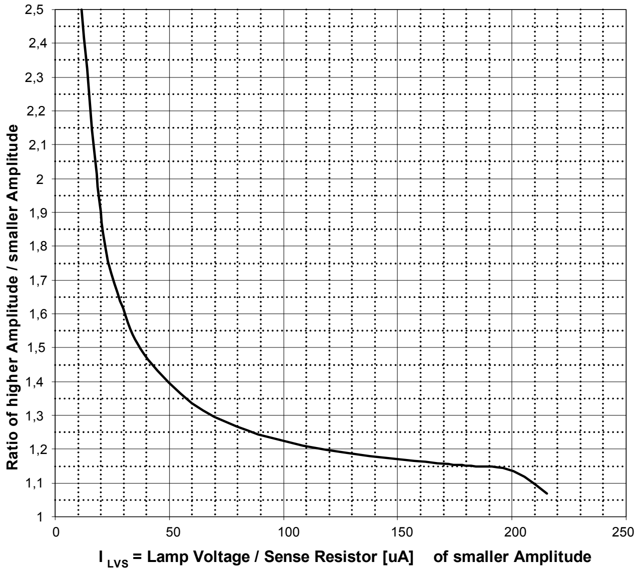


Figure 13 Maximum ratio of amplitudes versus sense current.

Furthermore the rectification effect (EOL2) is detected when the ratio of the higher amplitude divided by the smaller amplitude of the lamp voltage is bigger than illustrated in Fig. 13. for longer than 500ms. The ratio is evaluated each cycle of the lamp voltage. The limit of the ratio increases dependend on the peak current of the smaller amplitude of the lamp voltage from 1,15 at I_{LVS}= 200µA nonlinear to 1,4 at I_{LVS}= 50µA.

If the EOL2 conditions are detected, the control is disabled and the status is latched as a failure mode. Measuring the duration of incorrect operating conditions is done by a check every 4ms. If the fault condition is existing, a counter counts up, if the fault condition is not existing, the counter counts down. So we get an integration of the fault events that allows a very effective monitoring of strange operating conditions.

The detection of EOL1 and EOL2 requires an AC current input at the sense pin LVS for proper operation. A DC current at pin LVS will lead to a defined reaction only, if the level exeeds 175µA (typically) for longer than 610µs which results in a shut down and change over into the latched failure mode.

3.5 Detection of capacitive mode operating conditions

If there happens a situation like an open resonant circuit (e.g. a sudden break of the tube) the voltage across the resonant capacitor and current through the shunt of the low-side inverter MOSFET rise quickly. This event is detected by inverter current limitation (1,6V) and results in shut down of the control. This status is latched as a failure mode.

In another kind of failure the operation of the inverter may leave the zero voltage switching (ZVS) and move into capacitive mode operation or into operation below resonance. There are two different levels for capacitive mode detection implemented in the IC. A first criteria detects low deviations from ZVS (CapLoad1) and changes operation into fault mode, if this operation lasts longer than 500ms. For CapLoad1 the same counter is used as for the end-of-life evaluation.

A second threshold detects severe deviations such as rectangular shapes of voltage during operation below resonance (CapLoad2). Then the inverter is turned off as soon as these conditions last longer than 610µs and the IC changes over into fault mode. The evaluation of the failure condition is done by an up and down counter which samples the status every 40µs.

CapLoad1 is sensed in the moment when low-side Gate drive is turned on. If the voltage level at pin RES is above the V_{REScap} threshold (typ. 0,24V) related to the level V_{RESLLV}, conditions of CapLoad1 are assumed.

CapLoad2 is sensed in the moment when the high-side Gate drive is turned on. If the voltage level at pin RES is below the V_{REScap} threshold related to the level V_{RESLLV}, conditions of CapLoad2 are assumed. As the reference level V_{RESLLV} is a floating level, it is updated every on-time of the low-side MOSFET.

D61 limits voltage transients at pin RES that can occur during removal of the lamp in run mode.

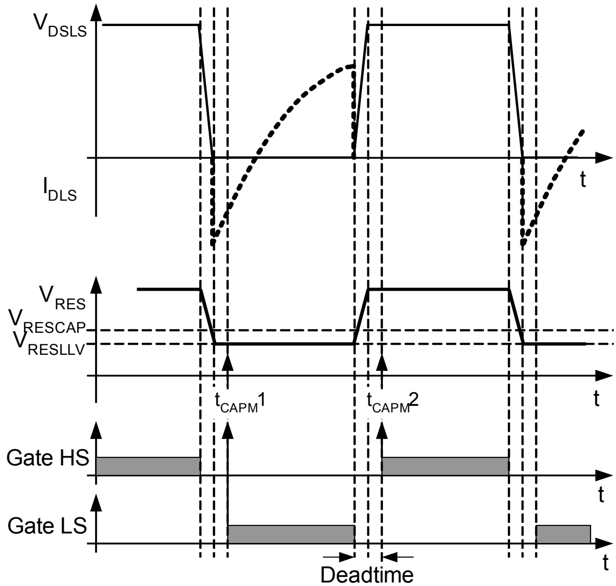


Figure 14 Levels and points in time for detection of CapLoad1 and CapLoad2.

3.6 Interruption of Operation and Restart after Lamp Removal

In the event of a failing operation the fault latch is set after the specified reaction time (e.g. 500ms at EOL2). Then the Gate drives are shut down immediately, the control functions are disabled and the current consumption is reduced to a level of 150µA (typically). Vcc is clamped by internal zener diode to max 17,5V at 2mA. So the internal zener diode is only designed to limit Vcc when fed from the start-up current, but not from the charge pump supply! There is a current limitation at the internal zener diode function (max 5mA at Vcc= 17,5V) in order to avoid conflicts with the clamping level of the external zener diode.

The capacitor at pin RES is discharged and charged during 32 cycles in order to generate a delay of several 10ms. The delay is implemented for avoiding malfunctions in detecting the lamp removal due to voltage transients that can occur after shut down. The reset of the fault latch happens after exceeding the 1,6V threshold at pin RES and enabling the IC after lamp removal and subsequent decreasing voltage level at pin RES below the 1,3V threshold.

The status failure mode is kept as long until a lamp removal is detected (interruption of current across filaments and detection of the return of the current) or the supply voltage drops below UVLO. After a break down of the supply voltage below the undervoltage lockout (UVLO) threshold the IC resets any failure latch and will try to restart as soon as Vcc exceeds the start-up threshold.

An undervoltage (75%) of the bus voltage will not be latched as a fault condition. If the undervoltage lasts longer than 80µs the Gate drives are switched off and the IC tries to restart after a Vcc hysteresis has been passed.

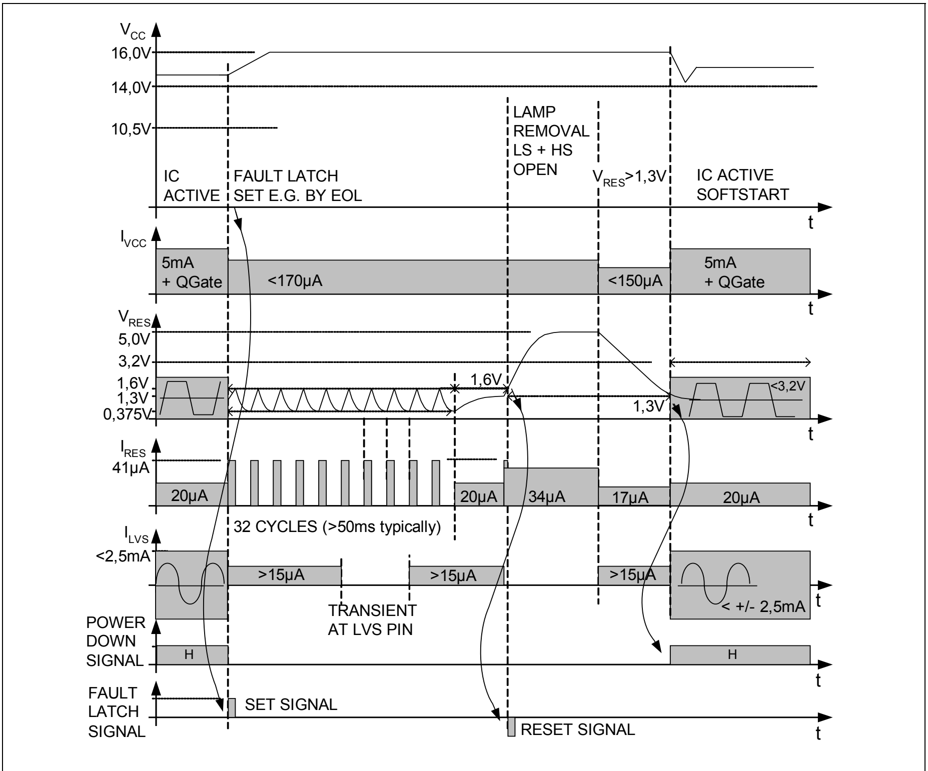


Figure 15 Interruption of operation by a fault condition and subsequent lamp removal.

4 State Diagram

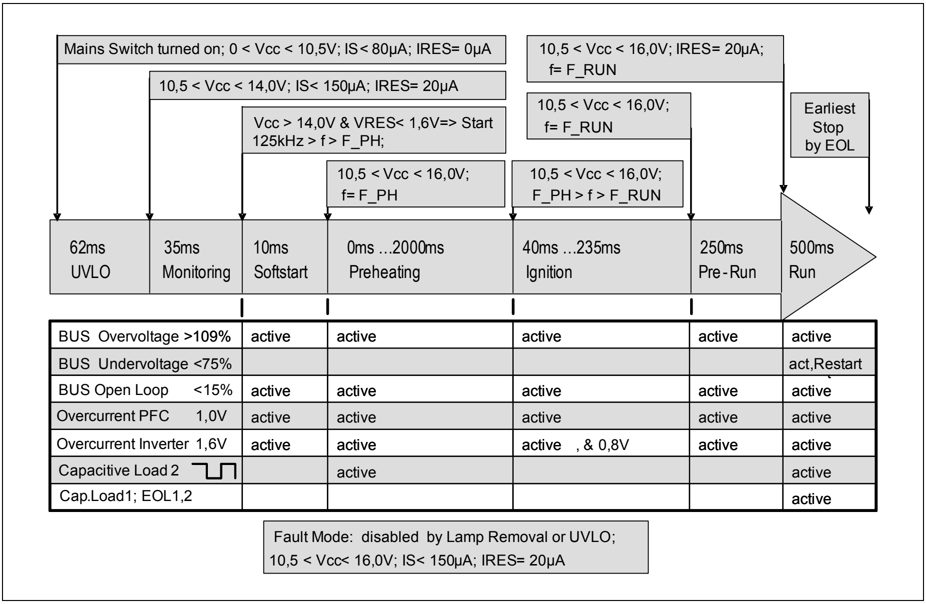


Figure 16 State Diagram

5 Protection Functions

Description of Fault	Fault-Type	Min. Duration of Effect	Detection active during: Softstart 10ms	Preheat Mode 0 - 2000ms	Ignition Mode 40 - 235ms	Pre-Run Mode 250ms	Run Mode	Consequence
+/- Peak Level of Lamp Voltage above threshold	EOL1	610µs					X	Power down, latched Fault Mode
Ratio of +/- amplitudes of lamp voltage > 1.15 or < 0.85	EOL2	500ms					X	Power down, latched Fault Mode
No zero voltage switching	Cap.Load 1	500ms					X	Power down, latched Fault Mode
Voltage at Pin RES > 3.0V	Open Filament	500ms					X	Power down, latched Fault Mode
Bus voltage > 109% of rated level in active operation	Overvoltage	500ms					X	Power down, latched Fault Mode
Bus voltage > 109% of rated level 10µs after power up	Overvoltage							Gate drivers off, restart after V_{CC} hysteresis
Bus voltage > 109% of rated level in active operation	PFC Overvoltage	5µs	X	X	X	X	X	Turn-off PFC MOSFET until Bus Voltage < 105%
Bus voltage < 75% of rated level	Undervoltage	80µs					X	Gate drivers off, restart after V_{CC} hysteresis
Bus voltage < 15% of rated level	Open Loop Detection	1µs	X	X	X	X	X	Power down
Capacitive Load, Operation below resonance	Cap.Load 2	610µs		X			X	Power down, latched Fault Mode
Run frequency can not be achieved	No Ignition	235ms			X			Power down, latched Fault Mode
Voltage at Pin RES > 1.6V before power up	LS open Filament	1ms						Prevents power up
Current into Pin LVS < 12µA	HS open Filament	1ms						Prevents power up
Voltage at Pin PFCCS > 1.0V	PFC Overcurrent	260ns	X	X	X	X	X	Turn-off PFC MOSFET immediately
Voltage at Pin LSCS > 0.8V	Inverter Current Limit	250ns			X			Increases the Operating Frequency
Voltage at Pin LSCS > 1.6V	Inverter Overcurrent	400ns	X	X	X	X	X	Power Down, Latched Fault Mode
Supply voltage at Pin VCC < 14.0V before power up	Below startup threshold	1µs						Prevents power up
Supply voltage at Pin VCC < 10.5V after power up	Below UVLO threshold	1µs	X	X	X	X	X	Power Down, Reset of Latched Fault Mode

6 Electrical Characteristics

Note: All voltages without the high side signals are measured with respect to ground (pin 4). The high side voltages are measured with respect to pin17/20. The voltage levels are valid if other ratings are not violated.

6.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 3 (VCC) and pin 18 (HSVCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
LSCS Voltage	V_{LSCS}	-5	6	V	
LSCS Current	I_{LSCS}	-3	3	mA	
LSGD Voltage	V_{LSGD}	-0.3	V_{cc}+0.3	V	internally clamped to 11V
VCC Voltage	V_{VCC}	-0.3	18	V	see VCC Zener Clamp
VCC Zener Clamp Current	$I_{VCCzener}$	-5	5	mA	IC in Power Down Mode
PFCGD Voltage	V_{PFCGD}	-0.3	V_{cc}+0.3	V	internally clamped to 11V
PFCCS Voltage	V_{PFCCS}	-5	6	V	
PFCCS Current	I_{PFCCS}	-3	3	mA	
PFCZCD Voltage	V_{PFCZCD}	-3	6	V	
PFCZCD Current	I_{PFCZCD}	-5	5	mA	
PFCVS Voltage	V_{PFCVS}	-0.3	5.3	V	
RFRUN Voltage	V_{RFRUN}	-0.3	5.3	V	
RFPH Voltage	V_{RFPH}	-0.3	5.3	V	
RTPH Voltage	V_{RTPH}	-0.3	5.3	V	
RES Voltage	V_{RES}	-0.3	5.3	V	
LVS Current1	I_{LVS_1}	-1	1	mA	IC in Power Down Mode
LVS Current2	I_{LVS_2}	-3	3	mA	IC in Active Mode
HSGND Voltage	V_{HSGND}	-900	900	V	referring to GND
HSGND, Voltage Transient	dV_{HSGND}/dt	-40	40	V/ns	
HSVCC Voltage	V_{HSVCC}	-0.3	18	V	referring to HSGND
HSGD Voltage	V_{HSGD}	-0.3	V_{HSVCC}+ 0.3	V	internally clamped to 11V referring to HSGND
PFCGD Peak Source Current	$I_{PFCGDsomax}$	—	150	mA	< 100ns
PFCGD Peak Sink Current	$I_{PFCGDsimax}$	—	700	mA	< 100ns
LSGD Peak Source Current	$I_{LSGDsomax}$	—	75	mA	< 100ns
LSGD Peak Sink Current	$I_{LSGDsimax}$	—	400	mA	< 100ns
HSGD Peak Source Current	$I_{HSGDsomax}$	—	75	mA	< 100ns
HSGD Peak Sink Current	$I_{HSGDsimax}$	—	400	mA	< 100ns
Junction Temperature	T_j	-25	150	°C	

Storage Temperature	T_S	-55	150	°C	
Max possible Power Dissipation	P_{tot}	—	2	W	PG-DSO-18-2, T_{amb} = 25°C
Thermal Resistance (Both Chips) Junction-Ambient	R_{thJA}	—	60	K/W	PG-DSO-18-2
Thermal Resistance (HS Chips) Junction-Ambient	R_{thJAHS}	—	120	K/W	PG-DSO-18-2
Thermal Resistance (LS Chips) Junction-Ambient	R_{thJALS}	—	120	K/W	PG-DSO-18-2
Soldering Temperature			260	°C	wave sold. acc.JESD22A111
ESD Capability	V_{ESD}	—	2	kV	Human body model[1)]

1) According to EIA/JESD22-A114-B (discharging an 100pF capacitor through an 1.5kΩ series resistor).

6.2 Operating Range

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
HSVCC Supply Voltage	V_{HSVCC}	$V_{HSVCCoff}$	17.0	V	referring to HSGND
HSGND Supply Voltage	V_{HSGND}	-900	900	V	referring to GND
VCC Supply Voltage	V_{VCC}	V_{VCCoff}	17.5	V	
LSCS Voltage Range	V_{LSCS}	-4	5	V	
PFCVS Voltage Range	V_{PFCVS}	0	4	V	
PFCCS Voltage Range	V_{PFCCS}	-4	5	V	
PFCZCD Current Range	I_{PFCZCD}	-4	4	mA	
LVS Voltage Range	V_{LVS}	-0.3	[1)]	V	IC in Power Down Mode
LVS Current Range	I_{LVS}	[2)]	300	µA	IC in Power Down Mode
LVS Current Range	I_{LVS}	-2.5	2.5	mA	IC in Active Mode
Junction Temperature	T_j	-25	125	°C	
Adjustable Preheating Frequency Range set by RFPH	F_{RFPH}	F_{RFRUN}	150	kHz	
Adjustable Run Frequency Range set by RFRUN	F_{RFRUN}	20	100	kHz	
Adjustable Preheating Time Range set by RTPH	t_{RTPH}	0	1980	ms	
Set Resistor for Run Frequency	R_{FRUN}	5	25	kΩ	
Set Resistor for Preheating Frequency (R_{FRUN} parallel R_{FPH})	R_{FRUN} II R_{FPH}	3.3		kΩ	
Set Resistor for Preheating Time	R_{TPH}	0	20	kΩ	

1) Limited by maximum of current range at LVS

2) Limited by minimum of voltage range at LVS

6.3 Characteristics

6.3.1 Power Supply Section

Note: The electrical characteristics involve the spread of values given within the specified supply voltage and junction temperature range T_J from – 25 °C to 125 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of V_{CC} = 15 V and V_{HSVCC} = 15V is assumed and the IC operates in active mode. Furthermore all voltages are referring to GND if not otherwise mentioned.

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
High Side Leakage Current	$I_{HSGNDleak}$		0.01	2	µA	V_{HSGND} = 800V V_{GND} = 0V
VCC Quiescent Current	I_{VCCqu1}		80	120	µA	$V_{VCC} = V_{VCCoff}$ - 0.5V
VCC Quiescent Current	I_{VCCqu2}		110	150	µA	$V_{VCC} = V_{VCCon}$ - 0.5V
VCC Supply Current with Inactive Gates	$I_{VCCsup1}$		5	7	mA	V_{PFCVS} > 2.725V
VCC Supply Current in Latched Fault Mode	$I_{VCClatch}$	—	110	170	µA	V_{RES} = 5V
LS VCC Turn-On Threshold LS VCC Turn-Off Threshold LSVCC Turn-On/Off Hysteresis	V_{VCCon} V_{VCCoff} V_{VCChys}	13.6 10.0 3.2	14.1 10.5 3.6	14.6 11.0 4.0	V V V	
VCC Zener Clamp Voltage	$V_{VCCclmp}$	15.7	16.3	16.9	V	I_{VCC} = 2mA V_{RES} = 5V
VCC Zener Clamp Current	$I_{VCCzener}$	2.5	—	5	mA	V_{VCC} = 17.5V V_{RES} = 5V
HSVCC Quiescent Current	$I_{HSVCCqu}$ [1)]	—	170	250	µA	$V_{HSVCC} = V_{HSVCCon}$ -0.5V
HSVCC Supply Current with Inactive Gate	$I_{HSVCCsup1}$ [1)]	—	0.65	1.2	mA	
HSVCC Turn-On Threshold HSVCC Turn-Off Threshold HSVCC Turn-On/Off Hysteresis	$V_{HSVCCon}$ [1)] $V_{HSVCCoff}$ [1)] $V_{HSVCChys}$ [1)]	9.6 7.9 1.4	10.1 8.4 1.7	10.7 9.1 2.0	V V V	

[1)] With reference to High Side Ground HSGND

6.3.2 PFC Section

6.3.2.1 PFC Current Sense (PFCCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Turn-Off Threshold	$V_{PFCCSoff}$	0.95	1.0	1.05	V	
Duration of Overcurrent for turn-off	$t_{PFCCSoff}$	200	250	320	ns	
Spike Blanking	$t_{blanking}$	140	200	260	ns	
PFCCS Bias Current	$I_{PFCCSbias}$	-0.5		0.5	µA	V_{PFCCS} = 1.5V

6.3.2.2 PFC Zero Current Detector (PFCZCD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Zero Crossing Upper Threshold	$V_{PFCZCDup}$	1.4	1.5	1.6	V	
Zero Crossing Lower Threshold	$V_{PFCZCDlow}$	0.4	0.5	0.6	V	
Zero Crossing Hysteresis	$V_{PFCZCDhys}$		1.0		V	
Clamping of Positive Voltages	$V_{PFCZCDpclp}$	5.0	6.3	7.2	V	I_{PFCZCD} = 4mA
Clamping of Negative Voltages	$V_{PFCZCDnclp}$	-3.5	-2.9	-2.0	V	I_{PFCZCD} = 4mA
PFCZCD Bias Current	$I_{PFCZCDbias}$	-0.5		0.5	µA	V_{PFCZCD} = 1.7V
PFCZCD Ringing Suppression Time	$t_{ringsup}$	350	500	650	ns	

6.3.2.3 PFC Bus Voltage Sense (PFCVS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	$V_{PFCVSref}$	2.47	2.5	2.53	V	
Overvoltage Upper Detection Limit	$V_{PFCVSup}$	2.675	2.725	2.78	V	
Overvoltage Lower Detection Limit	$V_{PFCVSlow}$	2.57	2.625	2.67	V	
Overvoltage Hysteresis	$V_{PFCVShys}$	70	100	130	mV	
Undervoltage Detection Limit	$V_{PFCVSuv}$	1.79	1.83	1.87	V	
Undervoltage Shut Down	$V_{PFCVSsd}$	0.30	0.375	0.45	V	
Bias Current (ESD-Stress<1KV)	$I_{PFCVSbias}$	-1		1	µA	V_{PFCVS} = 2.5V
Bias Current (ESD-Stress>1KV)	$I_{PFCVSbias}$	-2.5		2.5	µA	V_{PFCVS} = 2.5V

6.3.2.4 PFC PWM Generation

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Initial On-Time	$t_{PFCon\text{-}initial}$	2.0	3.0	3.8	µs	V_{PFCZCD} = 0V
Max. On-Time	$t_{PFCon\text{-}max}$	19	23.5	28	µs	0.45V < V_{PFCVS} < 2.45V
Repetition Time when missing Zero Crossing	t_{PFCrep}	38	50	62	µs	V_{PFCZCD} = 0V
Off-time when missing ZCD Signal	t_{PFCoff}	35	42	49	µs	V_{PFCZCD} = 0V

6.3.2.5 PFC Gate Drive (PFCGD)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
PFCGD Low Voltage	$V_{PFCGDlow}$	0.4	0.7	0.9	V	I_{PFCGD} = 5mA
		0.4	0.75	1.1	V	I_{PFCGD} = 20mA
		-0.1	0.3	0.6	V	I_{PFCGD} = -20mA
PFCGD High Voltage	$V_{PFCGDhigh}$	10.2	11	11.8	V	I_{PFCGD} = -20mA
		9.0	—	—	V	I_{PFCGD} = -1mA V_{VCC} = V_{VCCoff} + 0.3V
		8.5	—	—	V	I_{PFCGD} = -5mA V_{VCC} = V_{VCCoff} + 0.3V
PFCGD Voltage Active Shut Down	$V_{PFCGDsd}$	0.4	0.75	1.1	V	I_{PFCGD} = 20mA V_{VCC} = 5V
PFCGD Peak Source Current	$I_{PFCGDsource}$	—	100	—	mA	R_{load} = 4Ω + C_{Load} = 3.3nF[1)]
PFCGD Peak Sink Current	$I_{PFCGDsink}$	—	-500	—	mA	R_{load} = 4Ω + C_{Load} = 3.3nF[1)]
PFCGD Rise Time 2V < V_{LSGD} < 8V	$t_{PFCGDrise}$	110	220	400	ns	R_{load} = 4Ω + C_{Load} = 3.3nF
PFCGD Fall Time 8V > V_{LSGD} > 2V	$t_{PFCGDfall}$	20	45	70	ns	R_{load} = 4Ω + C_{Load} = 3.3nF

[1)] The parameter is not subject to production test - verified by design/characterization

6.3.3 Inverter Section

6.3.3.1 Inverter Control (RFRUN, RFPH, RTPH)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Start-Up Frequency	$F_{startup}$	112	125	138	kHz	
Duration of Soft Start, shift F from Start-Up to Preheating Frequency	$t_{softstart}$	9.0	11.0	13.5	ms	
Preheating Frequency	F_{RFPH1}	97.0	100	103.0	kHz	R_{RFPH} = 10kΩ R_{RFRUN} = 10kΩ
Run Frequency	F_{RFRUN1}	49.0	50.0	51.0	kHz	R_{RFRUN} = 10kΩ
Preheating Time	t_{RTPH1}	720	900	1080	ms	R_{RTPH} = 8.06kΩ
Preheating Time	t_{RTPH2}	50	90	130	ms	R_{RTPH} = 806Ω[1)]
Current Source Preheating Time	I_{RTPH}	132	140	148	µA	
Min. Duration of Ignition, shift F from Preheating to Run Frequency	$t_{IGNITION}$	34	40	48	ms	[1)]
Max. Duration of Ignition, shift F from Preheating to Run Frequency	$t_{NOIGNITION}$	210	235	290	ms	[1)]
Duration of Pre-Run, time period after operating frequency has reached Run Frequency first time after ignition	t_{PRERUN}	210	250	290	ms	[1)]
Minimum Duration of fault condition by EOL2, Cap.Load 1, Open filament and Overvoltage for entering latched Fault Mode	$t_{CAPLOAD1}$	420	500	580	ms	[1)]
Minimum Duration of fault condition by EOL1, Cap.Load 2 for entering latched Fault Mode	$t_{CAPLOAD2}$	520	610	770	µs	

[1)] The parameter is not subject to production test - verified by design/characterization

6.3.3.2 Inverter Low Side Current Sense (LSCS)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Current Limit Threshold during Ignition Mode	$V_{LSCSlimit}$	0.76	0.80	0.84	V	
Duration of Current above Threshold for enabling Frequency Increase	$t_{LSCSlimit}$	200	250	320	ns	
Overcurrent Shut Down Threshold	$V_{LSCSovc}$	1.55	1.60	1.65	V	
Duration of Overcurrent for entering Latched Fault Mode	$t_{LSCSovc}$	320	400	480	ns	
Bias Current LSCS	$I_{LSCSbias}$	-0.5		0.5	µA	V_{LSCS} = 1.5V
Inverter Dead Time between LS off and HS on	$t_{deadtime}$	1.50	1.75	2.0	µs	