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ICB2FL01G

Smart Ballast Control IC for Fluorescent Lamp Ballasts

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Never stop thinking

ICB2FL01G

Revision History		
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Actual Release: V1.2 Date: 05.05.2010		Previous Release: 18.02.2009
Page of actual Rel.	Page of prev. Rel.	Subjects changed since last release
3	3	Figure 1 Update
9	9	LVS1 Text Update
11	11	Figure 3 Update
21	21	Capter 2.4.2.1 Text Update and Figure 15 Update
24	24	PFC ON Time versus i_{ZCD} Signal
29	29	Update of Figure 26 and Text
38	38	Update 3.3 State Diagram
40	40	Update Protection Function Matrix HS Fil. Detection @ LVS1
53	53	BOM Update deleted Partnumbers of MOSFETs
54	54	Figure 42 Schematic of a serial Lamp Ballast Design
54	55	Figure 42 rename in Figure 43 and shift one page

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2nd Generation FL-Controller for Fluorescent Lamp Ballasts

Product Highlights

Lowest Count of external Components
900V-Half-Bridge driver with coreless Transformer Technology
Supports Customer In-Circuit Test Mode for reduced Tester Time
Supports Multi-Lamp Designs
Integrated digital Timers up to 40 seconds
Numerous Monitoring and Protection Features for highest Reliability
All Parameter are valid over a wide Temperature Range of T_J = - 25°C until + 125°C

Features PFC

Discontinuous Mode PFC for Load Range 0 to 100%
Integrated digital Compensation of PFC Control Loop
Improved Compensation for low THD of AC Input Current also in DCM Operation
Adjustable PFC Current Limitation

Features Lamp Ballast Inverter

Adjustable Detection of Overload and Rectifier Effect (EOL)
Detection of Capacitive Load operation
Improved Ignition Control allows Operation close to the magnetic Saturation of the lamp Inductors
Restart with skipped Preheating at short interruptions of Line Voltage (for Emergency Lighting)
Parameters adjustable by Resistors only
Pb-free Lead Plating; RoHS compliant

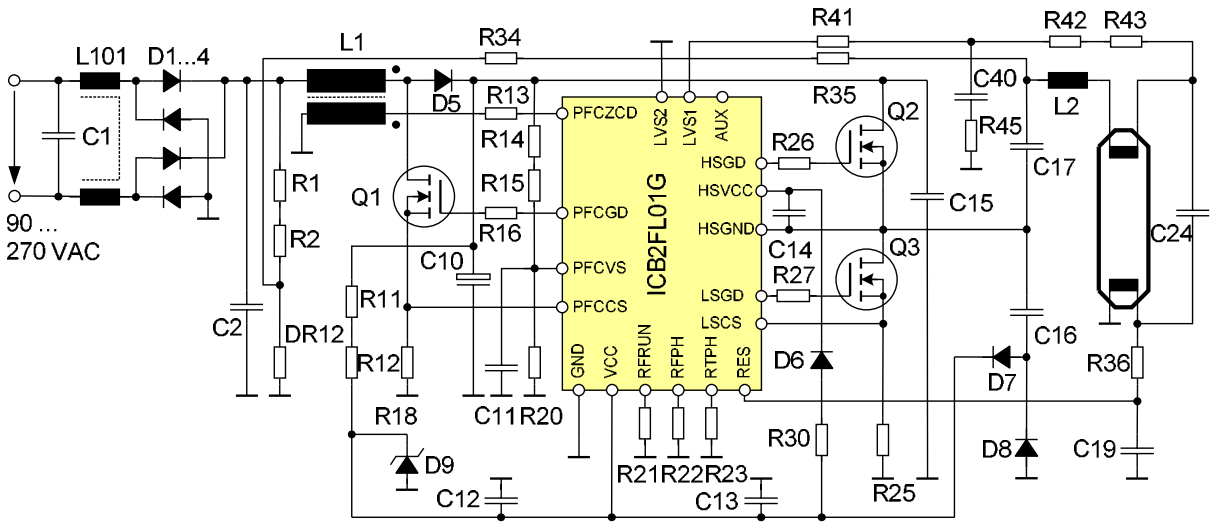

Figure 1: Typical Application Circuit of Ballast for a single Fluorescent Lamp

Description

The FL-Controller ICB2FL01G is designed to control fluorescent lamp ballast including a discontinuous mode Power Factor Correction (PFC), a lamp inverter control and a high voltage level shift half-bridge driver.
The control concept covers requirements for T5 lamp ballasts for single and multi-lamp designs. ICB2FL01G is based on the 1st Generation FL-Controller Technology, is easy to use and simply to design in. Therefore a basis for a cost effective solution for fluorescent lamp ballasts of high reliability. Figure 1 shows a typical application circuits of ballast for a single fluorescent T8 lamp with current mode preheat.

Table of Contents

1 Pin Configuration and Description

1.1 Pin Configuration

Pin	Symbol	Function
1	LSCS	Low side current sense (inverter)
2	LSGD	Low side Gate drive (inverter)
3	V_{CC}	Supply voltage
4	GND	Low side Ground
5	PFCGD	PFC Gate drive
6	PFCCS	PFC current sense
7	PFCZCD	PFC zero current detector
8	PFCVS	PFC voltage sense
9	RFRUN	Set R for run frequency
10	RFPH	Set R for preheat frequency
11	RTPH	Set R for preheating time
12	RES	Restart after lamp removal
13	LVS1	Lamp voltage sense 1
14	LVS2	Lamp voltage sense 2
15	AUX	Auxiliary output
16		Creepage distance
17	HSGND	High side ground
18	HSVCC	High side supply voltage
19	HSGD	High side Gate drive (inverter)
20		Not connected

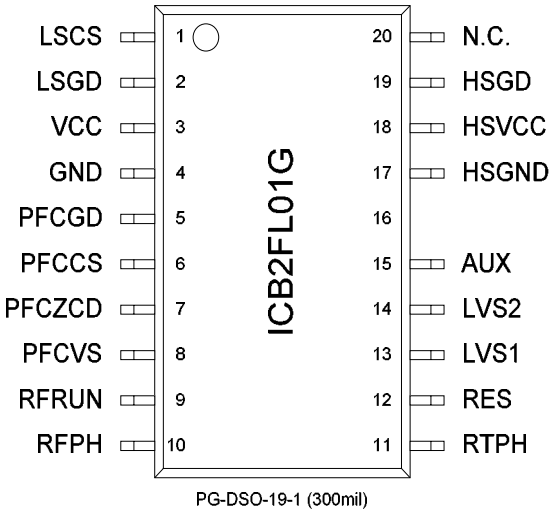

Figure 2: Package PG-DSO-19-1

1.2 Pin Description

LSCS (Low-side current sense, Pin 1)
This pin is directly connected to the shunt resistor which is located between the Source terminal of the low-side MOSFET of the inverter and ground.
Internal clamping structures and filtering measures allow for sensing the Source current of the low side inverter MOSFET without additional filter components.
There is a first threshold of 0.8V. If this threshold is exceeded for longer than 500ns during preheat or run mode, an inverter over current is detected and causes a latched shut down of the IC. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8V threshold. This stops the decreasing of the frequency and waits for ignition. The ignition control is now continuously monitored by the LSCS PIN. The Ignition control is designed to handle a choke operation in saturation while ignition in order to reduce the choke size.
If the sensed current signal exceeds a second threshold of 1.6V for longer than 500ns during start-up, soft start, ignition mode and pre-run, the IC changes over into a latched shut down.
There are further thresholds active at this pin during run mode that detects a capacitive mode operation. A first threshold at 100mV needs to sense a positive current during the second 50% on-time of the low-side MOSFET for proper operation (Capload 1). A second threshold of -100mV senses the current before the high-side MOSFET is turned on. A voltage level below of this threshold indicates a faulty operation (Capload 2). Finally a third threshold at 2.0 V senses even short overcurrent during turn-on of the high-side MOSFET such as they are typical for reverse recovery currents of a diode (Capload 2). If one of these three comparator thresholds indicate wrong operating conditions for longer than 620µs (Capload 2) or 2500ms (Capload 1) in run mode, the IC turns off the Gates and changes into fault mode due to detected capacitive mode operation (non-zero voltage switching).
The threshold of -100mV is also used to adjust the dead time between turn-off and turn-on of the half-bridge drivers in a range of 1.25µs to 2.5µs during all operating modes.

LSGD (Low-side Gate drive, Pin 2)
The Gate of the low-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO (under voltage lockout) and a limitation of the max H-level at 11.0 V during normal operation. In order to turn-on the MOSFET softly (with a reduced di_{DRAIN}/dt); the Gate voltage rises within 220ns typically from L-level to H-level. The fall time of the Gate voltage is less than 50ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the Gate drive loop. It is recommended to use a resistor of typically 10Ω between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor. The dead time between LSGD signal and HSGD signal is self adapting between 1.25µs and 2.5µs.

Vcc (Supply voltage, Pin 3)
This pin provides the power supply of the ground related section of the IC. There is a turn-on threshold at 14.1V and an UVLO threshold at 10.6V. Upper supply voltage level is 17.5V. There is an internal zener diode clamping V_{CC} at 16.3V (at I_{VCC}=2mA typically). The maximum zener current is internally limited to 5mA. For higher current levels an external zener diode is required. Current consumption during UVLO and during fault mode is less than 170µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for Gate drive and logic signal currents. In order to use a skipped preheating after short interruptions of mains supply it is necessary to feed the start-up current (160µA) from the bus voltage. Note: for external V_{CC} supply see notes in flowchart chapter 3.3.

GND (Ground, Pin 4)
This pin is connected to ground and represents the ground level of the IC for supply voltage, Gate drive and sense signals.

PFCGD (PFC Gate drive, Pin 5)
The Gate of the MOSFET in the PFC preconverter designed in boost topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. In order to turn-on the MOSFET softly (with a reduced di_{DRAIN}/dt), the Gate drive voltage rises within 220ns from L-level to H-level. The fall time of the Gate voltage is less than 50ns in order to turn off quickly.
A resistor of typically 10Ω between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor is recommended.
The PFC section of the IC controls a boost converter as a PFC preconverter in discontinuous conduction mode (DCM). Typically the control starts with Gate drive pulses with a fixed on-time of typically 4.0µs at V_{ACIN} = 230V increasing up to 22.7µs and with an off-time of 47µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from a fixed frequent operation to an operation with variable frequency. The PFC works in a critical conduction mode operation (CritCM) when rated and / or medium load conditions are present. That means triangular shaped currents in the boost converter choke without gaps and variable operating frequency. During low load (detected by an internal compensator) we get an operation with discontinuous conduction mode (DCM) that means triangular shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current.

PFCCS (PFC current sense, Pin 6)
The voltage drop across a shunt resistor located between Source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0 V for longer than 200ns the PFC Gate drive is turned off as long as the zero current detector (ZCD) enables a new cycle. If there is no ZCD signal available within 52µs after turn-off of the PFC Gate drive, a new cycle is initiated from an internal start-up timer.

PFCZCD (PFC zero current detector, Pin 7)
This pin senses the point of time when the current through boost inductor becomes zero during off-time of the PFC MOSFET in order to initiate a new cycle.
The moment of interest appears when the voltage of the separate ZCD winding changes from positive to negative level which represents a voltage of zero at the inductor windings and therefore the end of current flow from lower input voltage level to higher output voltage level. There is a threshold with hysteresis, for increasing level 1.5V, for decreasing level 0.5V, which detects the change of inductor voltage.

A resistor, connected between ZCD winding and PIN 7, limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (6.3V and -2.9V typically @ 5mA) of the IC.
If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52µs after turn-off of the PFC Gate drive. The source current out of this pin during the on-time of the PFC-MOSFET indicates the voltage level of the AC supply voltage. During low input voltage levels the on-time of the PFC-MOSFET is enlarged in order to minimize gaps in the line current during zero crossing of the line voltage and improve the THD (Total Harmonic Distortion) of the line current. An optimization of the THD is possible by trimming of the resistor between this pin and the ZCD-winding.

PFCVS (PFC voltage sense, Pin 8)
The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for rated bus voltage is 2.5V. There are further thresholds at 0.3125V (12.5% of rated bus voltage) for the detection of open control loop and at 1.875V (75% of rated bus voltage) for the detection of an under voltage and at 2.725V (109% of rated bus voltage) for the detection of an overvoltage. The overvoltage threshold operates with a hysteresis of 100mV (4% of rated bus voltage). For the detection of a successful start-up the bus voltage is sensed at 95% (2.375V). It is recommended to use a small capacitor between this pin and GND as a spike suppression filter.
In run mode, a PFC overvoltage stops the PFC Gate drive within 5µs. As soon as the bus voltage is less than 105% of rated level, the Gate drives are enabled again. If the overvoltage lasts for longer than 625ms, an inverter overvoltage is detected and turns off the inverter the gate drives also. This causes a power down and a power up when V_{BUS}<109%.
A bus under- (V_{BUS}>75%) or inverter overvoltage during run mode is handled as fault U. In this situation the IC changes into power down mode and generates a delay of 100ms by an internal timer. Then start-up conditions are checked and if valid, a further start-up is initiated. If start-up conditions are not valid, a further delay of 100ms is generated.
This procedure is repeated maximum seven times. If a start-up is successful within these seven cycles, the situation is interpreted as a short interruption of mains supply and the preheating is skipped. Any further start-up attempt is initiated including the preheating.

RFRUN (Set R for run frequency, Pin 9)
A resistor from this pin to ground sets the operating frequency of the inverter during run mode. Typical run frequency range is 20 kHz to 120 kHz. The set resistor R_RFRUN can be calculated based on the run frequency f_{RUN} according to the equation:

$$R_{FRUN} = \frac{5 \cdot 10^8 \Omega Hz}{f_{RUN}}$$

RFPH (Set R for preheat frequency, Pin 10)
A resistor from this pin to ground sets together with the resistor at pin 9 the operating frequency of the inverter during preheat mode. Typical preheat frequency range is run frequency (as a minimum) to 150 kHz. The set resistor R_RFPH can be calculated based on the preheat frequency f_{PH} and the resistor R_{RFRUN} according to the equation:

$$R_{RFPH} = \frac{R_{RFRUN}}{\frac{f_{PH} \cdot R_{RFRUN}}{5 \cdot 10^8 \Omega Hz} - 1}$$

RTPH (Set R for preheating time, Pin 11)
A resistor from this pin to ground sets the preheating time of the inverter during preheat mode. A set resistor range from zero to 25kΩ corresponds to a range of preheating time from zero to 2500ms subdivided in 127 steps.

$$R_{RTPH} = \frac{t_{\mathrm{Pr}eHeating}}{100 \frac{ms}{k\Omega}}$$

RES (Restart, Pin 12)
A source current out of this pin via resistor and filament to ground monitors the existence of the low-side filament of the fluorescent lamp for restart after lamp removal. A capacitor from this pin directly to ground eliminates a superimposed AC voltage that is generated as a voltage drop across the low-side filament. With a second sense resistor the filament of a paralleled lamp can be included into the lamp removal sense. Note: during start up, the chip supply voltage Vcc has to be below 14.1V before V_{RES} reaches the filament detection level.

During typical start-up with connected filaments of the lamp a current source I_{RES3} (-21.3 µA) is active as long as V_{CC} > 10.6V and V_{RES} < V_{RES1} (1.6V). An open low-side filament is detected, when V_{RES} > V_{RES1}. Such a condition will prevent the start-up of the IC. In addition the comparator threshold is set to V_{RES2} (1.3V) and the current source changes to I_{RES4} (-17.7 µA). Now the system is waiting for a voltage level lower than V_{RES2} at the RES pin that indicates a connected low-side filament, which will enable the start-up of the IC.
An open high-side filament is detected when there is no sink current $I_{LVSSINK}$ (>18 µA) into both of the LVS pins before the V_{CC} Start-up threshold is reached. Under these conditions the current source at the RES pin is I_{RES1} (-42.6µA) as long as V_{CC} > 10.6V and V_{RES} < V_{RES1} (1.6V) and the current source is I_{RES2} (-35.4 µA) when the threshold has changed to V_{RES2} (1.3V). In this way the detection of the high-side filament is mirrored to the levels on the RES pin.
There is a further threshold of 3.2V active at the RES pin during run mode. If the voltage level rises above this threshold for longer than 620µs, the IC changes over into latched fault mode.
In any case of fault detection with different reaction times the IC turns-off the Gate drives and changes into power down mode with a current consumption of 170µA max. An internal timer generates a delay time of 200ms, before start-up conditions are checked again. As soon as start-up conditions are valid, a second start-up attempt is initiated. If this second attempt fails, the IC remains in latched fault mode until a reset is generated by UVLO or lamp removal. The RES PIN can be deactivated via set the PIN to GND (durable).

LVS1 (Lamp voltage sense 1, Pin 13)
Before start-up this pin senses a current fed from the rectified line voltage via resistors through the high-side filaments of the lamp for the detection of an inserted lamp.
The sensed current fed into the LVS pin has to exceed 12 µA typically at a voltage level of 6.0 V at the LVS pin. The reaction on the high side filament detection is mirrored to the RES pin (see pin 12). In addition the detection of available mains supply after an interruption is sensed by this pin. Together with pin LVS2 and pin RES the IC can monitor the lamp removal of totally four lamps. If the functionality of this pin is not required, e.g. for single lamp designs, it can be disabled by connecting this pin to ground.

During run mode the lamp voltage is monitored with this pin by sensing a current proportional to the lamp voltage via resistors. An overload is indicated by an excessive lamp voltage. If the peak to peak lamp voltage effects a peak to peak current above a threshold of 21.3μA_{PP} for longer than 620µs, a fault EOL1 (end-of-life) is assumed. If the DC current at the LVS pin exceeds a threshold of ±42µA for longer than 2500ms, a fault EOL2 (rectifier effect) is assumed. The levels of AC sense current and DC sense current can be set separately by external RC network. Note, in case of a deactivation of the LVS1/2 PIN, a reactivation starts, when the current out the LVS1/2 PIN exceeds $V_{LVSEnable1}$ in RUN Mode.

LVS2 (Lamp voltage sense 2, Pin 14)
LVS2 has the same functionality as pin LVS1 for monitoring in parallel an additional lamp circuitry.

AUX (Auxiliary output, Pin 15)
This pin provides a control current for a NPN bipolar transistor during DCM operating mode of the PFC section. There is a source current of -450µA plus the current which is fed into pin PFCZCD from the detector winding available only during the enlarged off-time. That differ the discontinuous conduction mode (DCM) from the critical conduction mode (CritCM). With this transistor a resistor for damping oscillations can be switched to the ZCD winding in order to minimize the line current harmonics during DCM operating mode. If this function is not used, this pin has to be not connected.

Pin 16 Not Existing
PIN 16 does not exist, in order to provide a wider creepage distance to the high-side gate driver. Please pay attention to relevant standards.

HSGND (High-side ground, Pin 17)
This pin is connected to the Source terminal of the high-side MOSFET which is also the node of high-side and low-side MOSFET. This pin represents the floating ground level of the high-side driver and the high-side supply.

HSVCC (High-side supply voltage, Pin 18)
This pin provides the power supply of the high-side ground related section of the IC. An external capacitor between pin 17 and pin 18 acts like a floating battery which has to be recharged cycle by cycle via high voltage diode from low-side supply voltage during on-time of the low-side MOSFET. There is an UVLO threshold with hysteresis that enables high-side section at 10.1V and disables it at 8.4V.

HSGD (High-side Gate drive, Pin 19)
The Gate of the high-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO and a limitation of the max H-level at 11.0 V during normal operation. The switching characteristics are the same as described for LSGD (pin 2). It is recommended to use a resistor of about 10 Ω between drive pin and Gate in order to avoid oscillations and in order to shift the power dissipation of discharging the Gate capacitance into this resistor. The dead time between LSGD signal and HSGD signal is self adapting between 1.25µs and 2.5µs (typically).

Not connected (Pin 20)
This pin is internally not connected.

2 Functional Description

2.1 Typical Application Circutry

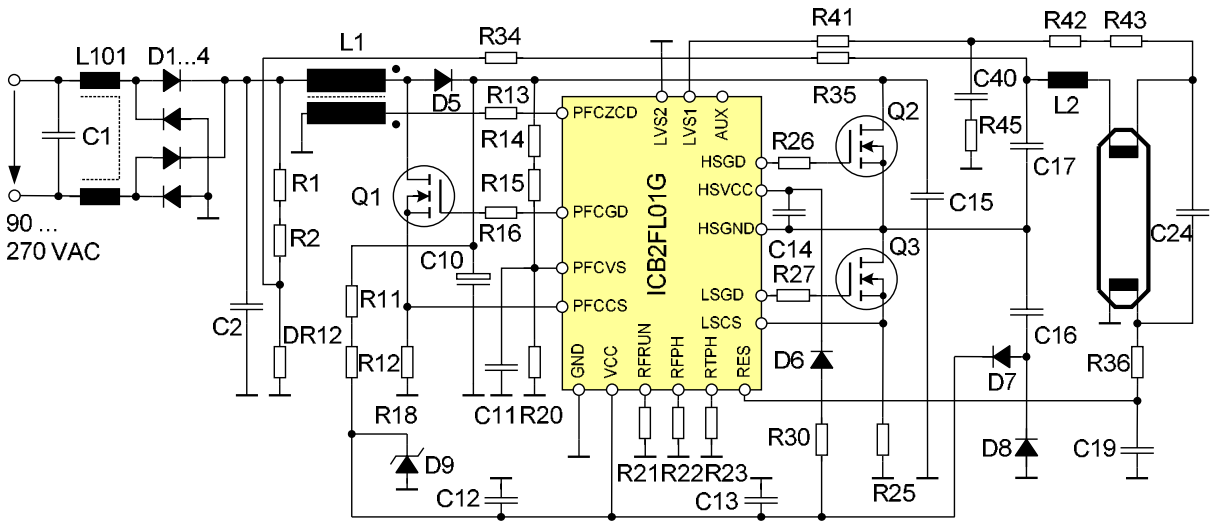

Figure 3: Application Circuit of Ballast for a single Fluorescent Lamp (FL)

The schematic in Figure 3 shows a typical application for a T5 single fluorescence lamp. It is designed for universal input voltage from 90 V_{AC} until 270 V_{AC}. The following chapters are explaining the components and referring to this schematic.

2.2 Normal Start Up

This chapter describes the basic operation flow (8 phases) from the UVLO (Under Voltage Lock Out) into Run Mode without any error detection. For detailed infromation see the following chapters 2.2.1 and 2.2.2. Figure 4 shows the 8 different phases during a typical start form UVLO (phase 1 Figure 4) to Run Mode (phase 8 Figure 4) into normal Operation (no failure detected).
In case the AC line input is switched ON, the V_{CC} voltage rises to the UVLO threshold V_{CC} = 10.6 V (no IC activities during UVLO). If V_{CC} exceeds the first threshold of V_{CC} = 10.6 V, the IC starts the first level of detection activity, the high and low side filament detection during the Start Up Hysteresis (phase 2 Figure 4).

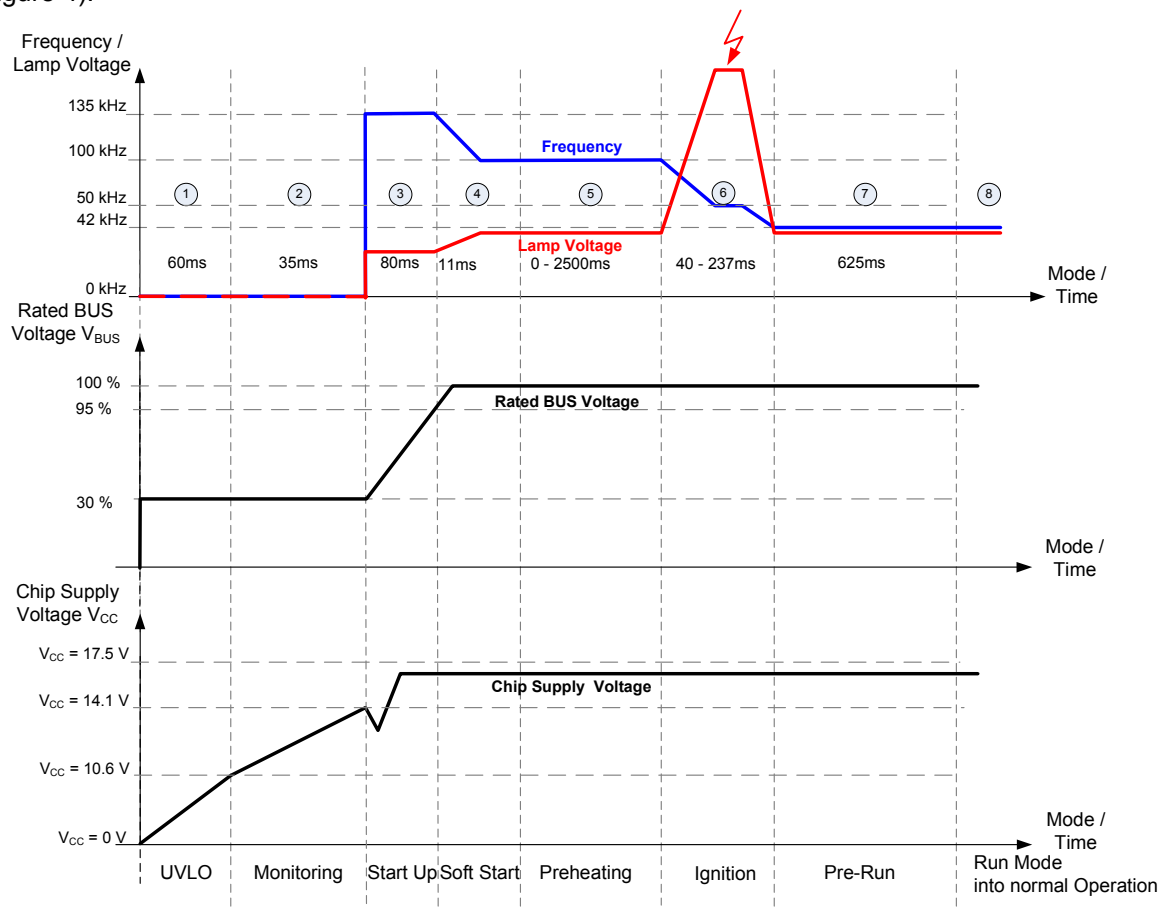

Figure 4: Typical Start Up Procedure in Run Mode (in normal Operation)

Followed by the end of the Start Up Hysteresis (phase 2 Figure 4) V_{CC} > 14.1 V and before phase 3 is active, a second level of detection activity senses for 80 µs (propagation delay of the IC) whether the rated bus voltage is below 12.5 % or above 105 %. If the previous bus voltage conditions are fulfilled and the filaments are detected, the IC starts the operation with an internally fixed startup frequency of typically 135 kHz (all gates are active). In case the bus voltage reaches a level of 95% of the rated bus voltage within latest 80ms (phase 3 Figure 4), the IC enters the Soft Start. During the Soft Start (phase 4 Figure 4), the Start Up frequency shifts from 135 kHz down to the set preheating frequency (chapter 2.2.2). In the Soft Start phase, the lamp voltage rises and the chip supply voltage reaches its working level from 10.6 V < V_{CC} < 17.5 V. After finish the Soft Start, the IC enters the Preheating mode (phase 5 Figure 4) for preheating the filaments (adjustable time) in order to extend the life cycle of the FL filaments. By finishing the preheating, the controller starts the Ignition (phase 6 Figure 4). During the Ignition phase, the frequency decreases from the set preheating frequency down to the set operation frequency (adjustable see chapter 2.2.2). If the Ignition is successful, the IC enters the Pre – Run mode (phase 7 Figure 4).

This mode is in order to prevent a malfunction of the IC due to an instable system e.g. the lamp parameters are not in a steady state condition. After finish the 625 ms Pre Run phase, the IC switches over to the Run mode (phase 8 Figure 4) with a complete monitoring.

2.2.1 Operating Levels from UVLO to Soft Start

This chapter describes the operating flow from phase 1 (UVLO) until phase 4 (Soft Start) in detail. The control of the ballast is able to start the operation within less than 100 ms (IC in active Mode). This is achieved by a small Start Up capacitor (about 1µF C12 and C13 – fed by start up resistors R11 and R12 in Figure 3) and the low current consumption during the UVLO (I_{VCC} = 130 µA – phase 1 Figure 5) and Start Up Hysteresis (I_{VCC} = 160 µA – defines the start up resistors – phase 2 Figure 5) phases. The chip supply stage of the IC is protected against over voltage via an internal Zener clamping network which clamps the voltage at 16.3 V and allows a current of 2.5 mA. For clamping currents above 2.5 mA, an external Zener diode (D9 Figure 3) is required.[1]

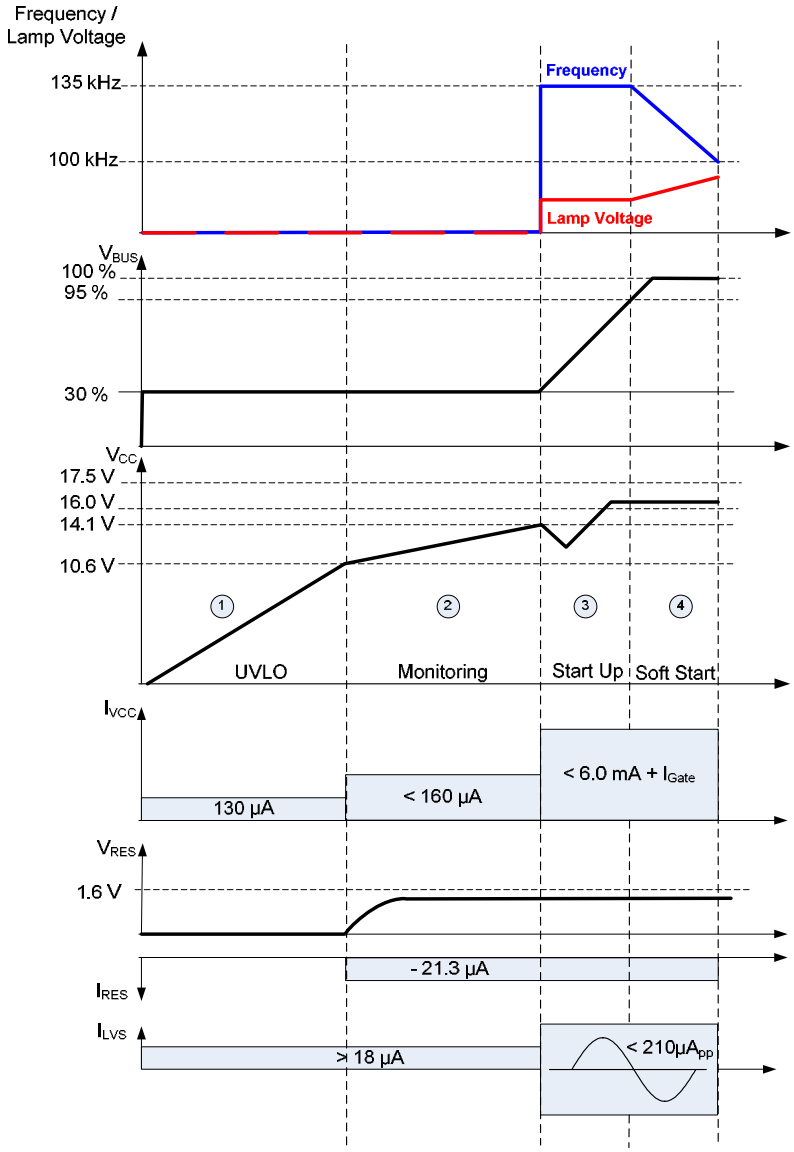

Figure 5: Progress of Level during a typical Start – UP

[1] I_{Gate} depends on MOSFET

In case of V_{CC} exceeds the 10.6 V level and stays below 14.1 V (Start up Hysteresis – phase 2 Figure 5), the IC checks whether the lamps are assembled by detecting a current across the filaments. The low side filaments are checked from a source current of typical I_{RES3} = - 21.3 µA out of PIN 12 RES
(Figure 5 I_{RES}). This current produces a voltage drop of V_{RES} < 1.6 V (filament is ok) at the low side filament sense resistor (R 36 in Figure 3), connected to GND (via low side filament). An open low side filament is detected (see chapter 2.3.2), when the voltage at the RES PIN exceeds the V_{RES} > 1.6V threshold (Figure 5 V_{RES}).
The high side filaments are checked by a current of I_{LVS} > 12 µA typically via resistors R41, R42 and R43 (Figure 3) into the LVS1 PIN 13 (for a single lamp operation) and LVS2 PIN 14 for a multi lamp operation. Note: in case of a single lamp operation, the unused LVS PIN has to be disabled via connection to GND. An open high side filament is detected (see 2.3.3) when there is no sink current into the LVS PIN. This causes a higher source current out of the RES PIN (typical 42.6 µA / 35.4 µA) in order to exceed V_{RES} > 1.6 V. In case of defect filaments, the IC keeps monitoring until there is an adequate current from the RES or the LVS PIN present (e.g. in case of removal a defect lamp).
When V_{CC} exceeds the 14.1 V threshold - by the end of the start up hysteresis in phase 2 Figure 5 - the IC waits for 80µs and senses the bus voltage. When the rated bus voltage is in the corridor of 12.5% < $V_{BUSrated}$ < 105% the IC powers up the system and enters phase 3 (Figure 5 $V_{BUSrated}$ > 95 % sensing) when not, the IC initiates an UVLO when the chip supply voltage is below V_{CC} < 10.6 V. As soon as the condition for a power up is fulfilled, the IC starts the inverter gate operation with an internal fixed Start Up frequency of 135 kHz. The PFC gate drive starts with a delay of app. 300µs. Now, the bus voltage will be checked for a rated level above 95 % for a duration of 80 ms (phase 3 Figure 5). When leaving phase 3, the IC enters the Soft Start phase and shifts the frequency from the internal fixed Start Up frequency of 135 kHz down to the set Preheating frequency e.g. f_{RFPH} = 100 kHz.

2.2.2 Operating Levels from Soft Start to Run Mode

This chapter describes the operating flow from phase 5 (Preheating mode) until phase 8 (Run mode) in detail. In order to extend the life time of the filaments, the controller enters - after the Soft Start Phase - the Preheating mode (phase 5 Figure 6). The preheating frequency is set by resistors R22 PIN RFPH to GND in combination with R21 (Figure 3) typ. 100 kHz e.g. R22 = 8.2 kΩ in parallel to R21 = 11.0 kΩ see Figure 3 at theR_{FRUN} - PIN). The preheating time can be selected by the programming resistor (R23 in Figure 3) at PIN RTPH from 0 ms up to 2500 ms (phase 5 Figure 6).

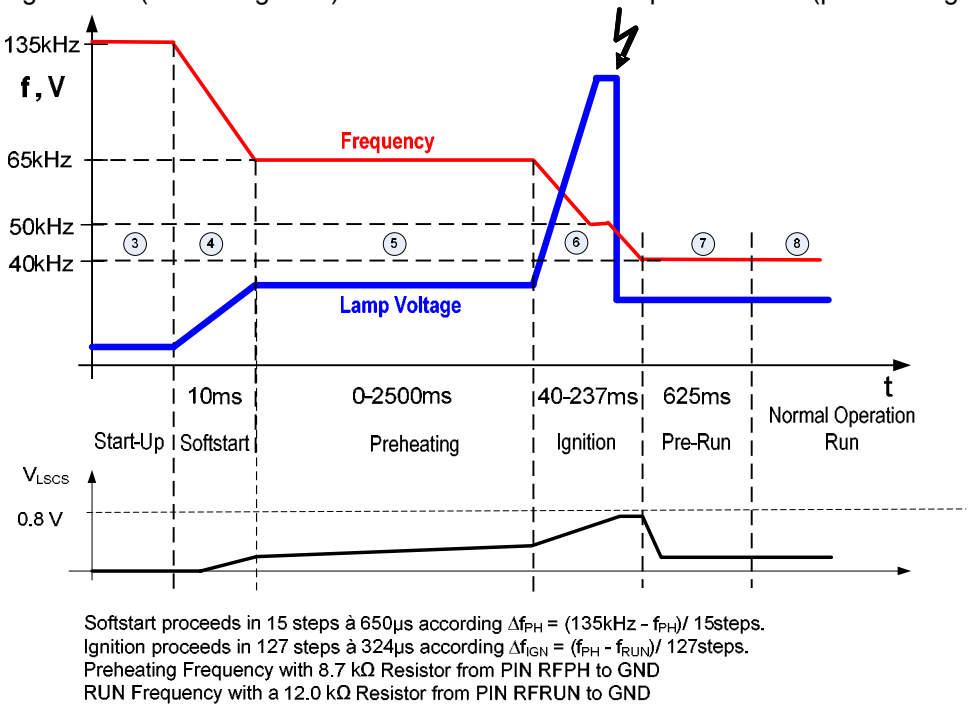

Figure 6: Typical Variation of Operating Frequency during Start Up

During Ignition (phase 6 Figure 6), the operating frequency of the inverter is shifted downward in t_{typ} = 40 ms (t_{max} = 237 ms) to the run frequency set by a resistor (R21 in Figure 3) at PIN RFRUN to GND (typical 45 kHz with 11.0 kΩ resistor). During this frequency shifting, the voltage and current in the resonant circuit will rise when the operation is close to the resonant frequency with increasing voltage across the lamp. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8V threshold. This stops the decreasing of the frequency and waits for ignition. The ignition control is now continuously monitored by the LSCS PIN. The maximum duration of the Ignition procedure is limited to 237 ms. Is there no Ignition within this time frame, the ignition control is disabled and the IC changes over into the latched fault mode. Furthermore, in order to reduce the lamp choke, the ignition control is designed to operate with a lamp choke in magnetic saturation during ignition. For an operation in magnetic saturation during ignition; the voltage at the shunt at the LSCS pin 1 has to be V_{LSCS} = 0.75V when ingition voltage is reached. If the ignition is successful, the IC enters the Pre – Run mode (phase 7 Figure 6). The Pre Run mode is a safety mode in order to prevent a malfunction of the IC due to an instable system e.g. the lamp parameters are not in a steady state condition. After 625 ms Pre Run mode, the IC changes into the Run Mode (phase 8 Figure 6). The Run mode monitors the complete system regarding bus over- and under voltage, open loop, over current of PFC and / or Inverter, lamp over voltage (EOL1) and rectifier effect (EOL2) see chapter 2.5) and capacitive load 1 and 2 (see chapter 2.6).

Functional Description

Figure 7 shows the lamp voltage versus the frequency during the different phases from Preheating to the Run Mode. The lamp voltage rises by the end of the Preheating phase with a decreasing frequency (e.g. 100 kHz to 50 kHz) up to 700 V during Ignition. After Ignition, the lamp voltage drops down to its working level with continuo decreasing the frequency (Figure 7) down to its working level e.g. 45 kHz (set by a resistor at the R_{FRUN} pin to ground). After stops the decreasing of the frequency, the IC enters the Pre Run mode.

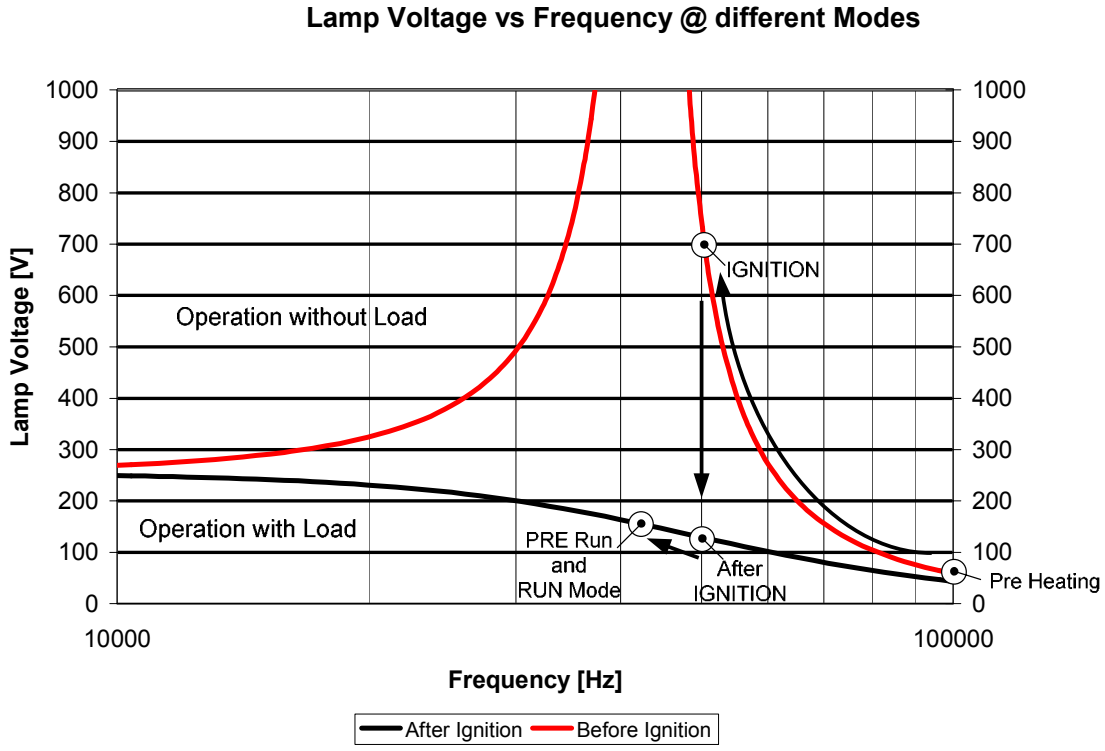

Figure 7: Lamp Voltage versus Frequency during the different Start up Phases

2.3 Filament Detection during Start Up and Run Mode

The low and high side filament detection is sensed via the RES and the LVS pins. The low side filament detection during start up and run mode is detected via the RES pin only. An open high side filament during start up will be sensed via the LVS and the RES pins.

2.3.1 Start Up with broken Low Side Filament

A source current of I_{RES3} = - 21.3 µA out of the RES pin (12) monitors during a start up (also in Run mode) the existence of a low side filament. In case of an open low side filament during the start up hysteresis (10.6V < V_{CC} < 14.1V) a capacitor (C19 in Figure 3) will be charged up via I_{RES3} = - 21.3 µA. When the voltage at the RES pin (12) exceeds V_{RES1} = 1.6 V, the controller prevents a power up and clamps the RES voltage internally at V_{RES} = 5.0 V. The gate drives of the PFC and inverter stage do not start working.

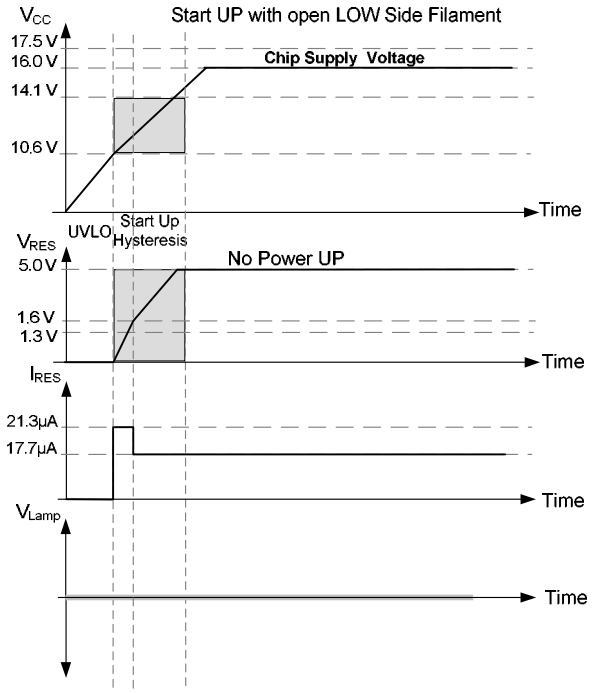

Figure 8: Startup with open Low Side Filament

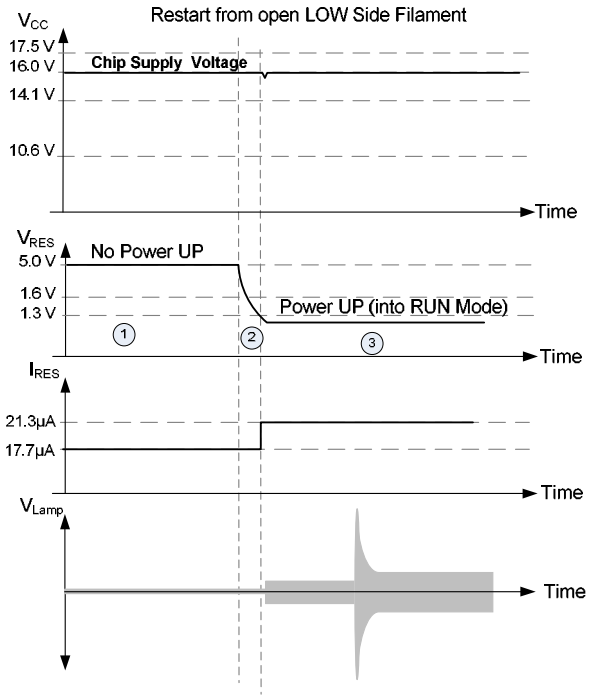

Figure 9: Restart from open Low Side Filament

The IC comparators are set now to a threshold of V_{RES1} = 1.3V and to I_{RES4} = - 17.7µA, the controller waits until the voltage at the RES pin drops below V_{RES1} = 1.3V.When a filament is present (Figure 9 section 2), the voltage drops below 1.3V and the value of the source current out of the RES pin is set from I_{RES4} = - 17.7 µA up to I_{RES3} = - 21.3 µA. Now the controller powers up the system including Soft Start and Preheating into the Run mode.

2.3.2 Low Side Filament Detection during Run Mode

In case of an open low side filament during Run mode, the current out of the RES pin I_{RES3} = - 21.3 µA charges up the capacitor C19 in Figure 3. If the voltage at the RES pin exceeds the V_{RES3} = 3.2V threshold, the controller detects an open low side filament and stops the gate drives after a delay of t = 620µs of an internal timer.

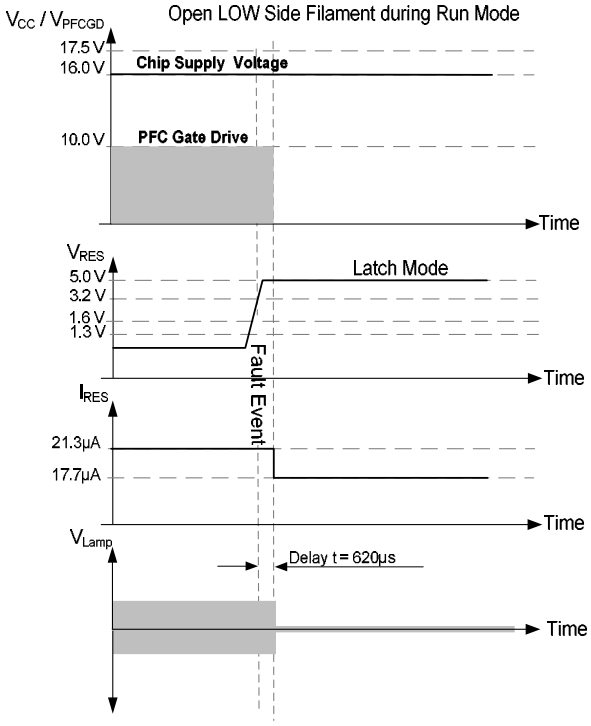

Figure 10: Open Low Side Filament Run Mode

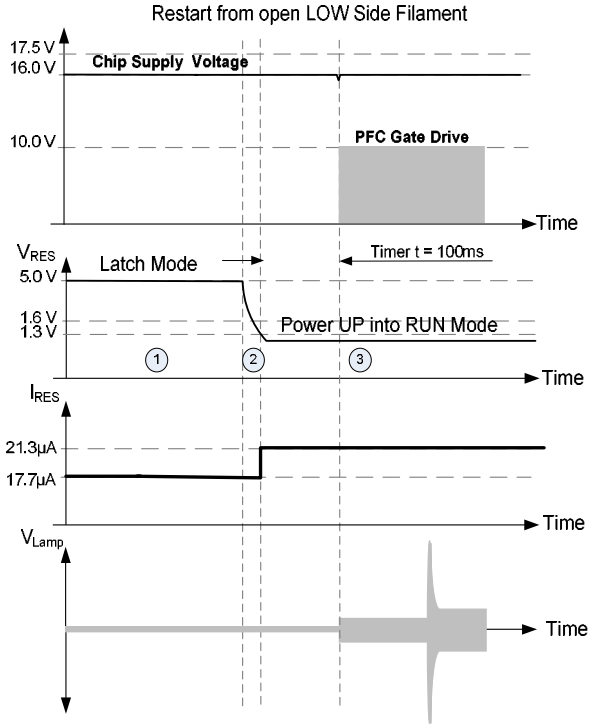

Figure 11: Restart from open LS Filament

A restart is initiated when a filament is detected e.g. in case of a lamp removal. In case of a filament is present (Figure 11 section 2), the voltage drops below 1.3V and the value of the source current out of the RES pin is set from I_{RES4} = - 17.7 µA up to I_{RES3} = - 21.3 µA. The controller powers up the system including Soft Start and Preheating into the Run mode (Figure 11 section 3).

2.3.3 Start Up with broken High Side Filament

An open high side filament during the start up hysteresis (10.6V < V_{CC} < 14.1V) is detected, when the current into the LVS pin 13 or 14 is below I_{LVS} = 12 µA (typically). In that case, the current out of the RES pin 12 rises up to I_{RES1} = - 42.6 µA. That causes a voltage at the RES pin crosses V_{RES1} = 1.6V. The source current is now set to I_{RES2} = - 35.4 µA and another threshold of V_{RES2} = 1.3V is active. The controller prevents a power up (see Figure 12), the gate drives of the PFC and inverter stage do not start working.

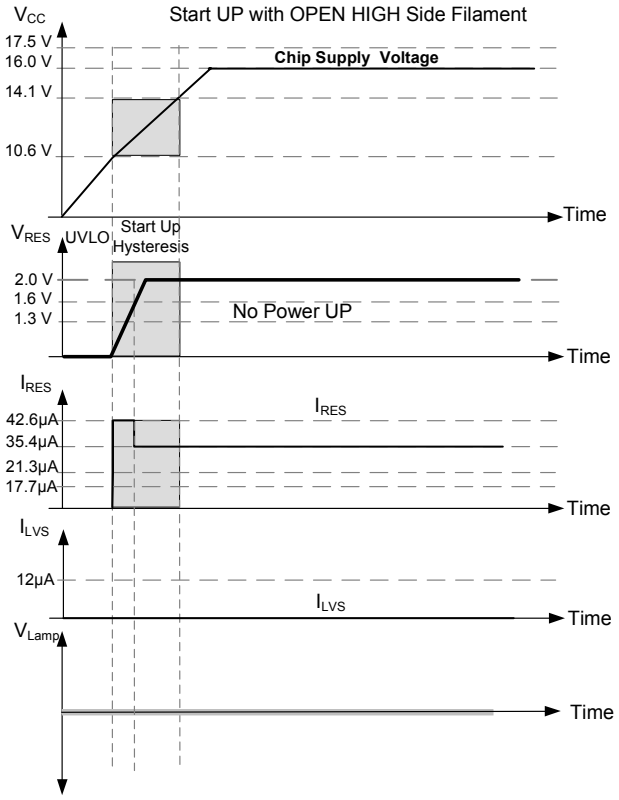

Figure 12: Start Up with open high Side Filament

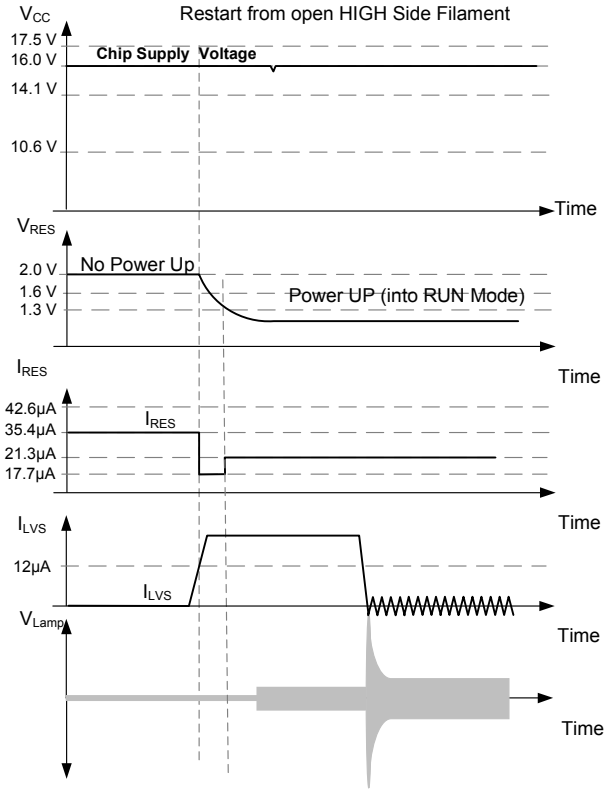

Figure 13: Restart from open high Side Filament

When the high side filament is present, e.g. insert a lamp, the current of the active LVS pins exceeds I_{LVS} > 12 µA (typically), the res current drops from I_{RES2} = - 35.4 µA down to I_{RES4} = - 17.7 µA (Figure 13). Now the controller senses the low side filament. When a low side filament is also present, and the controller drops (after a short delay due to a capacitor at the res pin) below V_{RES2} = 1.3V, the res current is set to I_{RES3} = - 21.3 µA, the controller powers up the system.

2.4 PFC Pre Converter

2.4.1 Discontinuous Conduction and Critical Conduction Mode Operation

The digital controlled PFC pre converter starts with an internally fixed ON time of typical t_{ON} = 4.0µs and variable frequency. The ON – time is enlarged every 280 µs (typical) up to a maximum ON – time of 22.7 µs. The control switches quite immediately from the discontinuous conduction mode (DCM) over into critical conduction mode (CritCM) as soon as a sufficient ZCD signal is available. The frequency range in CritCM is 22 kHz until 500 kHz, depending on the power (Figure 14) with a variation of the ON time from 22.7 µs > t_{ON} > 0.5µs.

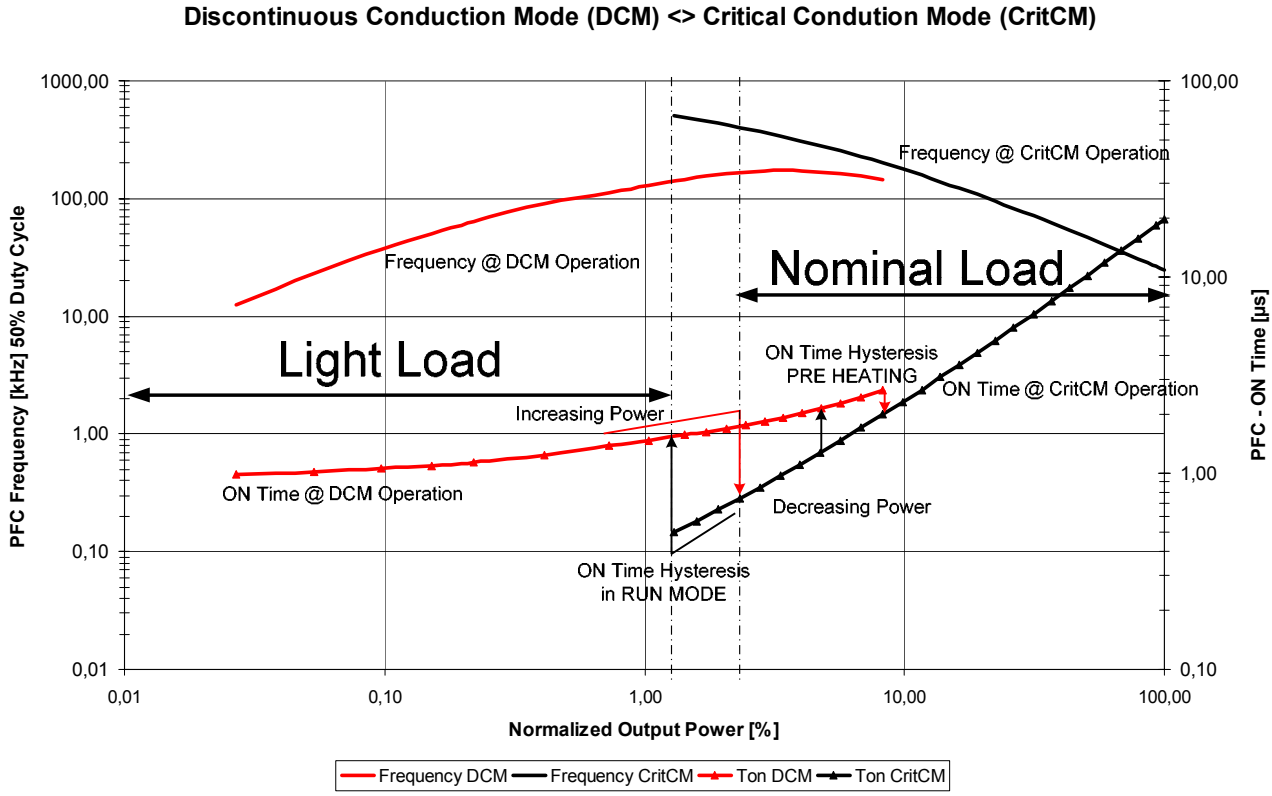

Figure 14: Operating Frequency and ON Time versus Power in DCM and CritCM Operation

For lower loads ($P_{OUTNorm}$ < 8 % from the normalized load[2]) the control operates in discontinuous conduction mode (DCM) with an ON – time from 4.0µs and increasing OFF – time. The frequency during DCM is variable in a range from 144 kHz down to typically 22 kHz @ 0.1 % Load (Figure 14). With this control method, the PFC converter enables a stable operation from 100 % load down to 0.1 %. Figure 14 shows the ON time range in DCM and CritCM (Critical Conduction Mode) operation. In the overlapping area of CritCM and DCM is a hysteresis of the ON time which causes a negligible frequency change.

[2] Normalized Power @ Low Line Input Voltage and maximum Load

2.4.2 PFC Bus Voltage Sensing

Over voltage, open loop, bus 95 % and under voltage states (Figure 15) of the PFC bus voltage are sensed at the PFCVS pin via the network R14, R15, R20 and C11 Figure 3 (C11 acts as a spike suppression filter).

2.4.2.1 Bus Over Voltage and PFC Open Loop

The bus voltage loop control is completely integrated (Figure 16) and provided by an 8 Bit sigma – delta A/D – converter with a typical sampling rate of 280 µs and a resolution of 4 mV/Bit. After leaving phase 2 (monitoring), the IC starts the power up (VCC > 14.1V). After power up, the IC senses for 80µs – 130µs the bus voltage below 12.5% (open loop) or above 105% (bus over voltage). In case of a bus over voltage ($V_{BUSrated}$ > 109 %) or open loop ($V_{BUSrated}$ < 12.5 %) in phases 3 until 8 the IC shuts off the gate drives of the PFC within 5µs respective in 1µs. In this case, the PFC restarts automatically when the bus voltage is within the corridor (12.5% < $V_{BUSrated}$ < 105 %) again. Is the bus voltage after the 80µs – 130µs valid, the bus voltage sensing is set to 12.5% < $V_{BUSrated}$ < 109 %. In case leaving these thresholds for longer than 1µ (open loop) or 5µs (overvoltage) the PFC gate drive stops working until the voltage drops below 105% or exceeds the 12.5% level. If the bus over voltage (> 109%) lasts for longer than 625ms in run mode, the inverter gates also shut off and a power down with complete restart is attempt (Figure 15).

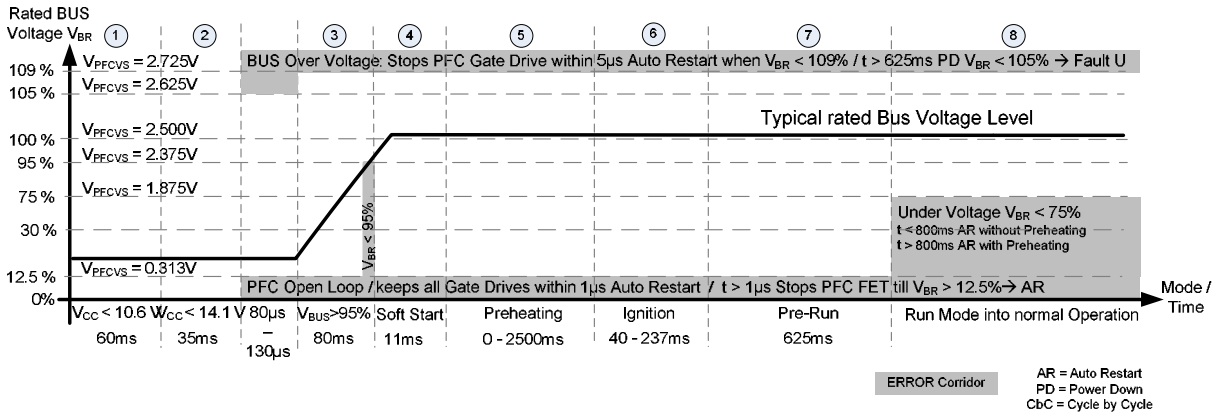

Figure 15: PFC Bus Voltage Operating Level and Error Detection

2.4.2.2 Bus Voltage 95% and 75% Sensing

When the rated bus voltage is in the corridor of 12.5% < $V_{BUSrated}$ < 109 %, the IC will check whether the bus voltage exceeds the 95 % threshold (Figure 15 phase 3) within 80 ms before entering the soft start phase 4. Another threshold is activated when the IC enters the run mode (phase 8). When the rated bus voltage drops below 75% for longer than 84 µs, a power down with a complete restart is attempted when a counter exceeds 800 ms. In case of a short term bus under voltage (the bus voltage reaches its working level in run mode before exceeding typically 800 ms (min. 500ms) the IC skips phases 1 until 5 and starts with ignition (condition for emergency lighting see 2.7.1). The internal reference level of the bus voltage sense V_{PFCVS} is 2.5 V (100 % of the rated bus voltage) with a high accuracy. A surge protection is activated in case of a rated bus voltage of V_{BUS} > 109% and a low side current sense voltage of V_{LSCS} > 0.8V for longer as 500ns in PRE RUN and RUN Mode.

2.4.3 PFC Structure of Mixed Signal

A digital NOTCH filter eliminates the input voltage ripple - independent from the mains frequency. A subsequent error amplifier with PI characteristic cares for a stable operation of the PFC pre converter (Figure 16).

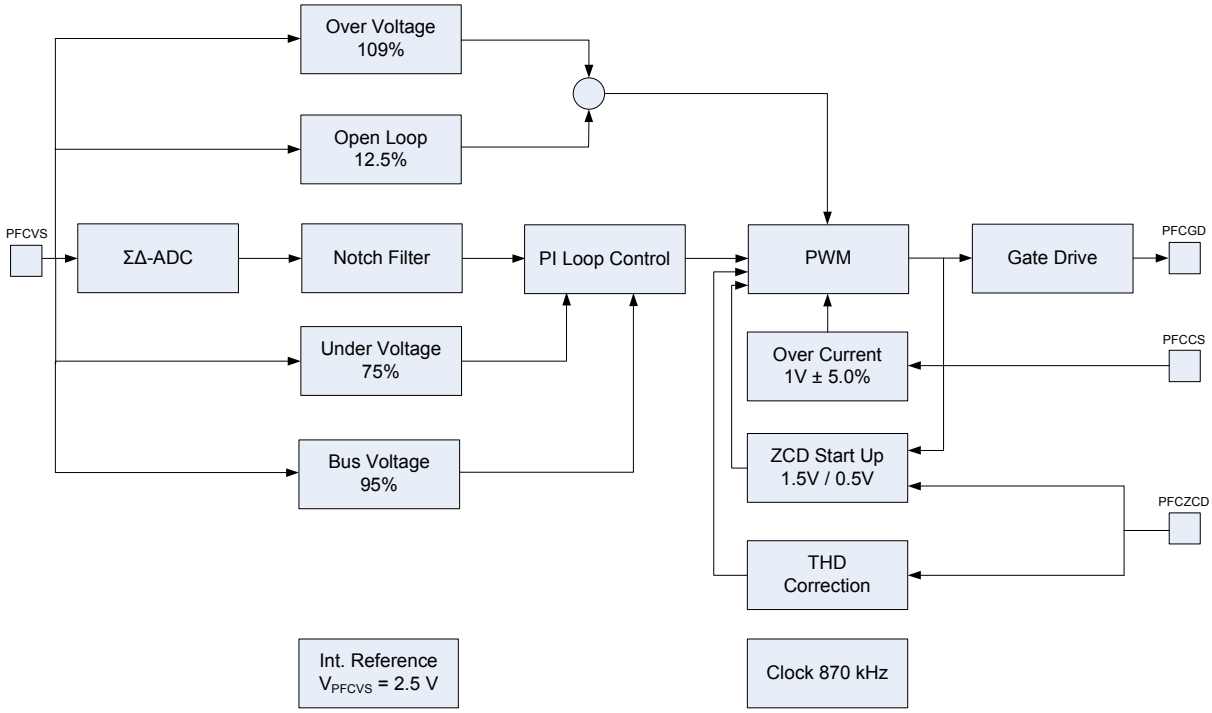

Figure 16: Structure of the mixed digital and analog control of the PFC pre converter

The zero current detection (ZCD) is sensed by the PFCZCD pin via R13 (Figure 3). The information of finished current flow during demagnetization is required in CritCM and in DCM as well. The input is equipped with a special filtering including a blanking of typically 500 ns and a large hysteresis of typically 0.5 V and 1.5 V V_{PFCZCD} (Figure 16).

2.4.4 THD Correction via ZCD Signal

An additional feature is the THD correction (Figure 16). In order to optimize the improved THD (especially in the zones A shown in Figure 17 ZCD @ AC Input Voltage), there is a possibility to extend pulse width of the gate signal (blue part of the PFC gate signal in Figure 17) via variable PFC ZCD resistor (see Resistor R13 in Figure 3) in addition to the gate signal controlled by the V_{PFCVS} signal (gray part of the PFC gate signal in Figure 17).

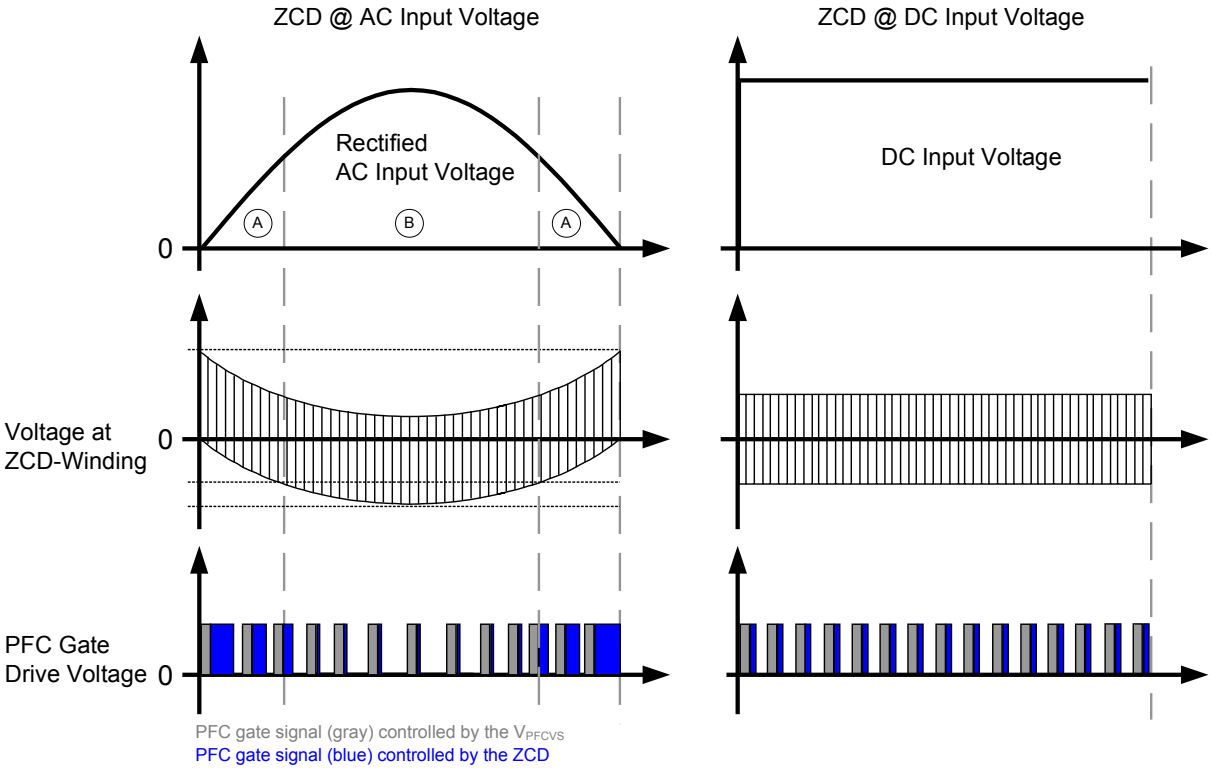

Figure 17: THD Optimization using adjustable Pulse Width Extension

In case of DC input voltage (see DC Input Voltage in Figure 17), the pulse width gate signal is fixed as a combination of the gate signal controlled by the V_{PFCVS} pin (gray) and the additional pulse width signal controlled by the ZCD pin (blue) shown in Figure 17 ZCD @ DC Input Voltage.
The PFC current limitation at pin PFCCS interrupts the ON – time of the PFC MOSFET if the voltage drop at the shunt resistors R18 (Figure 3) exceeds the V_{PFCCS} = 1.0 V (Figure 16). This interrupt will restart after the next sufficient signal from ZCD is available (Auto Restart). The first value of the resistor can be calculated by the ratio of the PFC mains choke and ZCD winding the bus voltage and a current of typically 1.5 mA (see equation below). An adjustment of the ZCD resistor causes an optimized THD.

$$R_{ZCD} = \frac{\frac{N_{ZCD}}{N_{PFC}} * V_{BUS}}{1.5mA}$$

Equation 1: R_{ZCD} a good pratical Value

The relationship between the extended PFC pulse width and the zero crossing detection current is shown in Figure 19.

2.4.5 Optional THD Correction dedicated for DCM Operation

For applications with a wide input voltage range and / or for applications using a wide variation of the power e.g. dimming, the application might work in the DCM (Discontinuous Conduction Mode). In order to minimize the high order harmonics during DCM, the detection of the DCM should be as close as possible at the point of inflection of the PFC drain source voltage shown in Figure 18. This can be realized with an optional damping network (R4, D10 and Q4 from the AUX pin to the ZCD resistor R13.

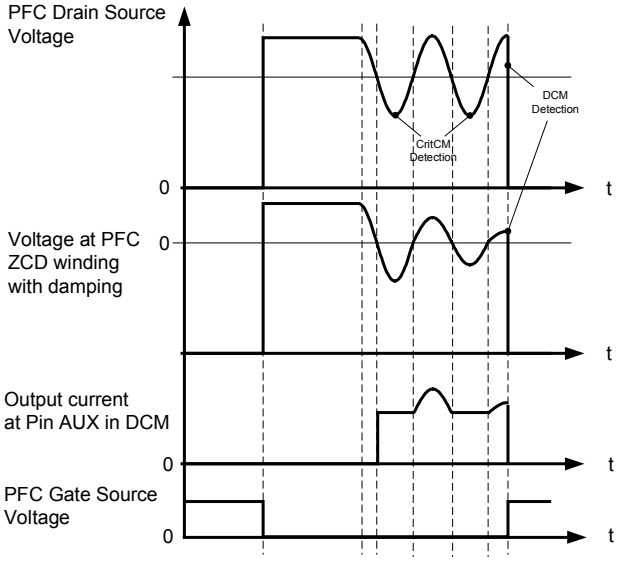

Figure 18: Signal Shapes with optional damping of oscillations during DCM operation of PFC

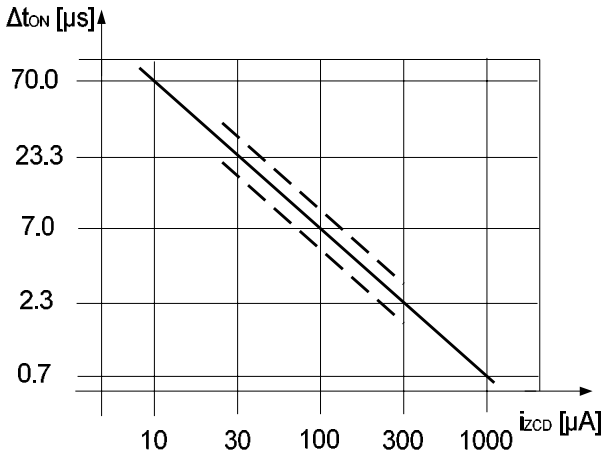

Figure 19: PFC ON Time Extension versus Zero Crossing Current Signal

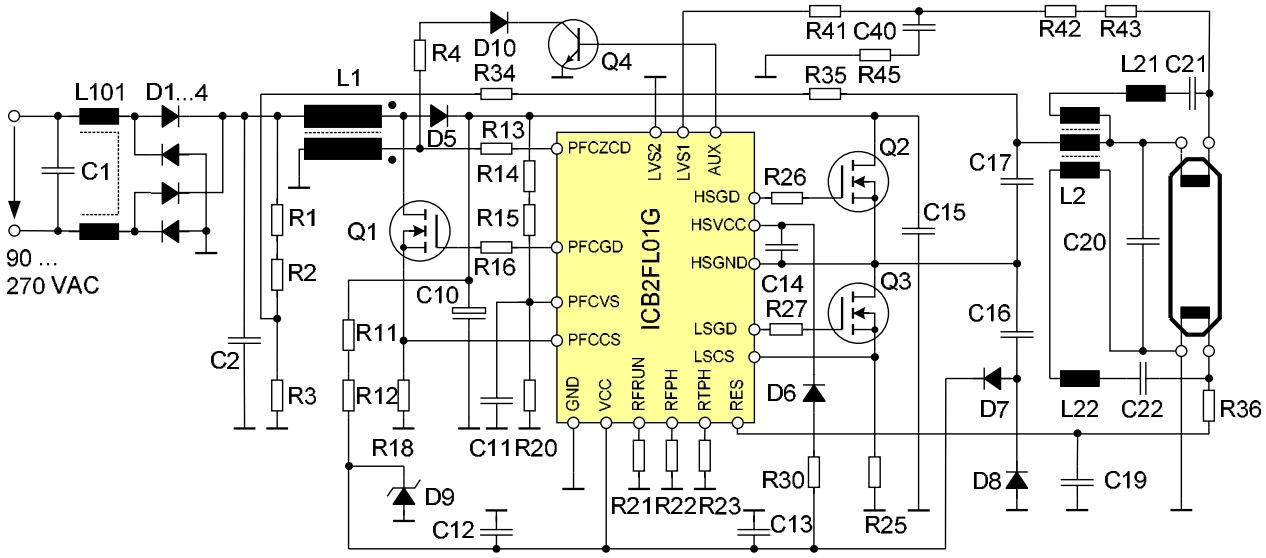

Figure 20: Optional Circuit for attenuating oscillations during DCM operation of PFC.

2.5 Detection of End-of-Life and Rectifier Effect

Two effects are present by End of Life (EOL): lamp over voltage (EOL1) and a rectifier effect (EOL2). After Ignition (see 1 in Figure 21), the lamp voltage breaks down to its run voltage level with decreasing frequency. By reaching the run frequency, the IC enters the Pre Run Mode for 625 ms. During this period, the EOL detection is still disabled. In the subsequent RUN Mode (2 in Figure 21) the detection of EOL1 (lamp over voltage see 3 Figure 21) and EOL2 (rectifier effect see 4 Figure 21) is complete enabled.

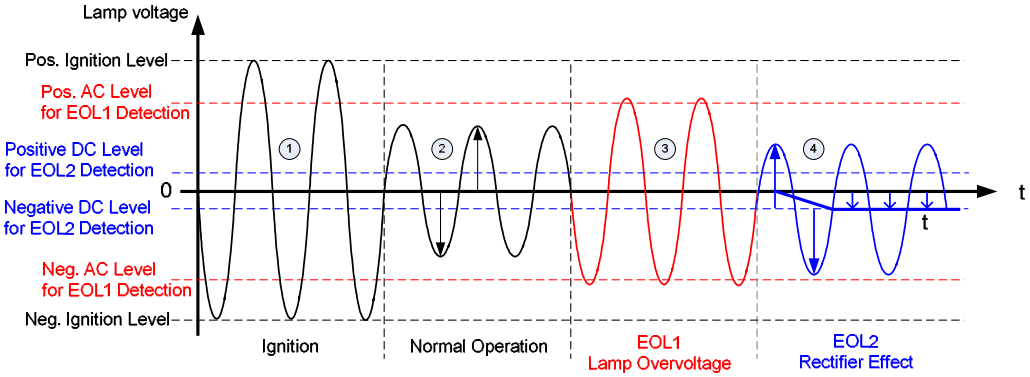

Figure 21: End of Life and Rectifier Effect

2.5.1 Detection of End of Life 1 (EOL1) – Lamp Overvoltage

The event of EOL1 is detected by measuring the positive and negative peak level of the lamp voltage via an AC current fed into the LVS pin (Figure 22). This AC current is fed into the LVS pins (LVS1 for single lamp and LVS2 for multi lamp applications) via Network R41, R42, R43 and the low pass filter C40 and R45 see Figure 3. If the sensed AC current exceeds 210 μA_{PP} for longer than 620 µs, the status of end-of-life (EOL1) is detected (lamp overvoltage / overload see Figure 22 LVSAC Current). The EOL1 fault results in a latched power down mode (after trying a single restart) the controller is continuously monitoring the status until EOL1 status changes e.g. a new lamp is inserted.

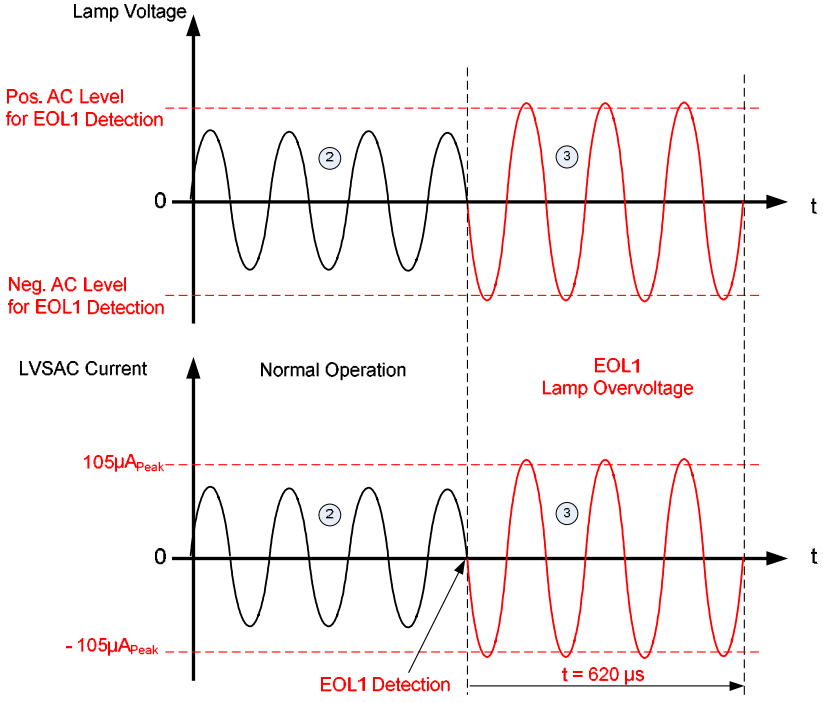

Figure 22: End of Life (EOL1) Detection, Lamp Voltage versus AC LVS Current