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ICB2FL03G

2nd Generation FL Controller for Fluorescent Lamp Ballasts

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Final V1.1, 2013-08-14	
page 54-55	inserted **Chapter 5.3.4 Parameter limits for extended temperature range down to -40°C**
Final V1.0 2013-02-14	
page 45	changed max value for $I_{HSVCCqu1}$ from 270µA to 280µA changed min value for $V_{HSVCCOn}$ from 9.9V to 9.8V
page 48	changed min value for $V_{PFCGDRise}$ from 105ns to 100ns typo correction: $V_{PFCGDRise}$ & $V_{PFCGDFall}$ --> $t_{PFCGDRise}$ & $t_{PFCGDFall}$
page 50	changed min value for $t_{LSGDRise}$from 105ns to 100ns
page 52	changed min value for $T_{HSGDRise}$ from 140ns to 120ns typo correction: $T_{HSGDRise}$ & $T_{HSGDFall}$ --> $t_{HSGDRise}$ & $t_{HSGDFall}$

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2nd Generation FL-Controller for Fluorescent Lamp Ballasts

Product Highlights

- Lowest count of external components
- 650 V half-bridge driver with coreless transformer technology
- Supports Customer In-Circuit Test Mode for reduced tester time
- Supports multi-lamp designs (series connection)
- Integrated digital timers up to 40 seconds
- Numerous monitoring and protection features for highest reliability
- Very high accuracy of frequencies and timers over the whole temperature range
- Very low standby losses

PFC Features

- Discontinuous mode PFC for load range 0 to 100%
- Integrated digital compensation of PFC control loop
- Improved compensation for low THD of AC input current, also in DCM operation
- Adjustable PFC current limitation

Lamp Ballast Inverter Features

- Adjustable detection of overload and rectifier effect (EOL)
- Detection of capacitive load operation
- Improved ignition control allows operation close to the magnetic saturation of the lamp inductors
- Restart with skipped preheating on short interruptions of line voltage (for emergency lighting)
- Parameters adjustable by resistors only
- Pb-free lead plating; RoHS-compliant

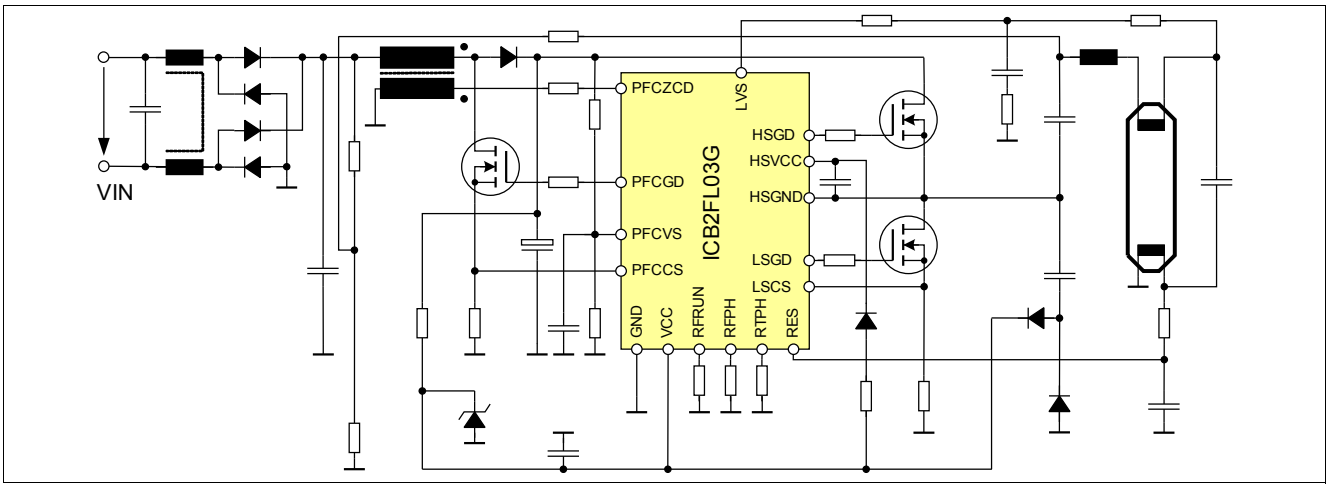

Figure 1 Typical Application Circuit of Ballast for a Single Fluorescent Lamp

Description

The FL controller ICB2FL03G is designed to control fluorescent lamp ballast, including a discontinuous mode Power Factor Correction (PFC), lamp inverter control and a high-voltage level shift half-bridge driver.

The control concept covers requirements for T5 lamp ballasts for single and multi-lamp designs (series connection supported). ICB2FL03G is based on the 2nd-generation FL controller technology, is easy to use and simple to design in. This makes the ICB2FL03G a basis for cost-effective solutions for fluorescent lamp ballasts with high reliability. **Figure 1** shows a typical application circuit of ballast for a single fluorescent T8 lamp with current mode preheating.

1 Pin Configuration and Functionality

1.1 Pin Configuration

Table 1 Pin Configuration for PG-DSO-16

Pin	Symbol	Function
1	LSGD	Low side gate drive (inverter)
2	LSCS	Low side current sense (inverter)
3	VCC	Supply voltage
4	GND	Low side ground
5	PFCGD	PFC gate drive
6	PFCCS	PFC current sense
7	PFCZCD	PFC zero current detector
8	PFCVS	PFC voltage sense
9	RFRUN	Set R for run frequency
10	RFPH	Set R for preheat frequency
11	RTPH	Set R for preheating time
12	LVS	Lamp voltage sense
13	RES	Restart after lamp removal
14	HSGND	High side ground
15	HSVCC	High side supply voltage
16	HSGD	High side gate drive (inverter)

1.2 PG-DSO-16 Package

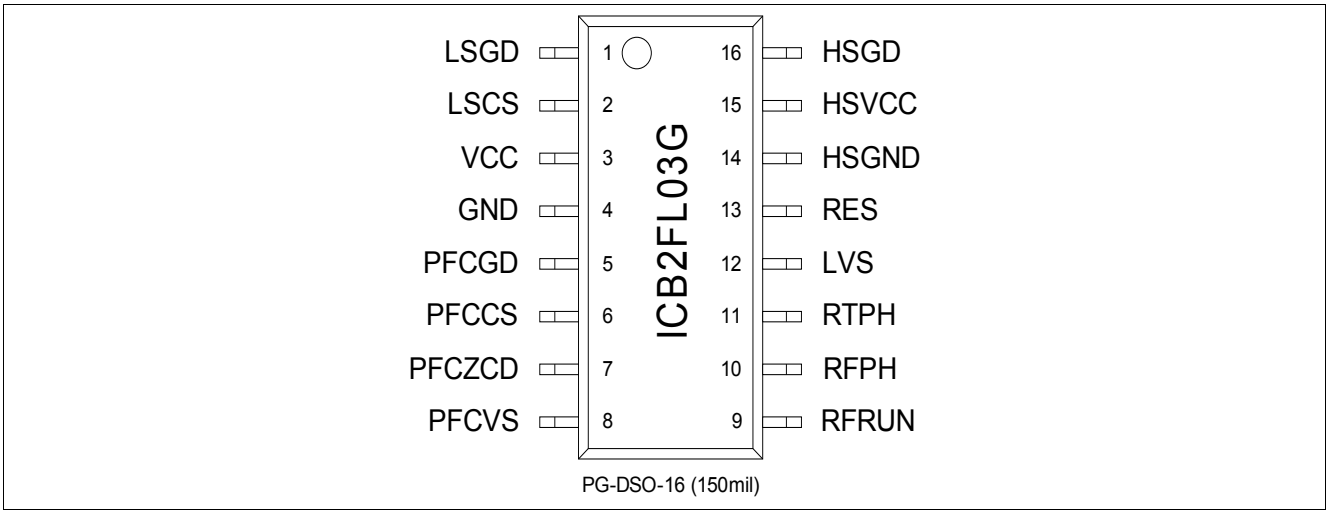

Figure 2 PG-DSO-16 Package (top view)

1.3 Pin Functionality

LSGD (low-side gate drive, pin 1)

The gate of the low-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO (under voltage lockout) and limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt); the gate voltage typically rises within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the gate drive loop. It is recommended to use a resistor of typically 10 Ω between drive pin and gate in order to avoid oscillations and in order to shift the power dissipation of discharging the gate capacitance into this resistor. The dead time between the LSGD signal and HSGD signal is self-adapting between 1.05 µs and 2.1 µs.

LSCS (low-side current sense, pin 2)

This pin is directly connected to the shunt resistor which is located between the source terminal of the low-side MOSFET of the inverter and ground.

Internal clamping structures and filtering measures allow for sensing the source current of the low-side inverter MOSFET without additional filter components.

The first threshold is 0.8 V. If this threshold is exceeded for longer than 500 ns during preheat or run mode, an inverter overcurrent is detected and causes a latched shutdown of the IC. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8 V threshold. This stops the frequency decrease and waits for ignition. The ignition control is now continuously monitored by the LSCS PIN. The ignition control is designed to handle choke operation in saturation during ignition in order to reduce the choke size.

If the sensed current signal exceeds a second threshold of 1.6 V for longer than 500 ns during start-up, soft start, ignition mode and pre-run, the IC changes over into latched shutdown.

There are further thresholds active at this pin during run mode that detect capacitive mode operation. An initial threshold at 50 mV needs to sense a positive current during the second 50 % on-time of the low-side MOSFET for proper operation (cap. load 1). A second threshold of -50mV senses the current before the high-side MOSFET is turned on. A voltage level below this threshold indicates faulty operation (cap. load 2). Finally a third threshold at 2.0 V senses even short overcurrent during turn-on of the high-side MOSFET, typical for reverse recovery currents of a diode (cap. load 2). If any of these three comparator thresholds indicates incorrect operating conditions for longer than 620 µs (cap. load 2) or 2500 ms (cap. load 1) in run mode, the IC turns off the gates and changes into fault mode due to detected capacitive mode operation (non-zero voltage switching).

The threshold of -50 mV is also used to adjust the dead time between turn-off and turn-on of the half-bridge drivers in a range of 1.05 µs to 2.1 µs during all operating modes.

Vcc (supply voltage, pin 3)

This pin provides the power supply of the ground related section of the IC. There is a turn-on threshold at 14.0 V and an UVLO threshold at 10.6 V. The upper supply voltage level is 17.5 V. There is an internal zener diode clamping V_{CC} at 16.3 V (at I_{VCC} = 2 mA typically). The maximum zener current is internally limited to 5 mA. An external zener diode is required for higher current levels. Current consumption during UVLO and during fault mode is less than 170 µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for gate drive and logic signal currents. In order to skip preheating after short interruptions to the mains supply it is necessary to feed the start-up current (160 µA) from the bus voltage. Note: for external V_{CC} supply, see notes in the flowchart (**Section 3.3**).

GND (ground, pin 4)

This pin is connected to ground and represents the ground level of the IC for supply voltage, gate drive and sense signals.

PFCGD (PFC gate drive, pin 5)

This pin controls the gate of the MOSFET in the PFC preconverter designed in boost topology. There is an active L-level during UVLO and limitation of the max H-level at 11.0 V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate drive voltage rises within 245 ns from L-level to H-level. The fall time of the gate voltage is less than 50 ns in order to turn off quickly.

A resistor of typically 10 Ω between the drive pin and gate is recommended in order to avoid oscillations and in order to shift the power dissipation of discharging the gate capacitance into this resistor.

The PFC section of the IC controls a boost converter as a PFC preconverter in discontinuous conduction mode (DCM). Control usually starts with gate drive pulses with a fixed on-time of typically 4.0 µs at V_{ACIN} = 230 V, increasing up to 24 µs and with an off-time of 47 µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from fixed frequency operation to operation with variable frequency. The PFC works in critical conduction mode operation (CritCM) when rated and / or medium load conditions are present. This means triangular-shaped currents in the boost converter choke without gaps and variable operating frequency. During low loads (detected by an internal compensator) operation is in discontinuous conduction mode (DCM) – i.e., triangular-shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current.

PFCCS (PFC current sense, pin 6)

The voltage drop across a shunt resistor located between the source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0 V for longer than 200 ns, the PFC gate drive is turned off as long as the zero current detector (ZCD) enables a new cycle. If no ZCD signal is available within 52 µs after turn-off of the PFC gate drive, a new cycle is initiated from an internal start-up timer.

PFCZCD (PFC zero current detector, pin 7)

This pin senses the point of time when the current through boost inductor becomes zero during off-time of the PFC MOSFET in order to initiate a new cycle.

The moment of interest appears when the voltage of the separate ZCD winding changes from the positive to negative level, which represents a voltage of zero at the inductor windings and therefore the end of current flow from the lower input voltage level to the higher output voltage level. There is a threshold with hysteresis – for increasing level 1.5 V, for decreasing level 0.5 V – which detects the change in inductor voltage.

A resistor, connected between ZCD winding and pin 7, limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (6.3 V and -2.9 V typically @ 5 mA) of the IC.

If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52 µs after turn-off of the PFC gate drive. The source current flowing out of this pin during the on-time of the PFC-MOSFET indicates the voltage level of the AC supply voltage. During low input voltage levels the on-time of the PFC-MOSFET is increased in order to minimize gaps in the line current during zero crossing of the line voltage and improve the THD (Total Harmonic Distortion) of the line current. Optimization of the THD is possible by trimming of the resistor between this pin and the ZCD winding.

PFCVS (PFC voltage sense, pin 8)

The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for rated bus voltage is 2.5 V. There are further thresholds at 0.3125 V (12.5 % of the rated bus voltage) for the detection of open control loop, at 1.875 V (75 % of the rated bus voltage) for the detection of undervoltage, and at 2.725 V (109 % of the rated bus voltage) for the detection of overvoltage. The

overvoltage threshold operates with a hysteresis of 100 mV (4 % of the rated bus voltage). For the detection of successful start-up, the bus voltage is sensed at 95 % (2.375 V). It is recommended to use a small capacitor between this pin and GND as a spike suppression filter.

In run mode, a PFC overvoltage stops the PFC gate drive within 5 µs. As soon as the bus voltage is less than 105 % of the rated level, the gate drives are enabled again. If the overvoltage lasts for longer than 625 ms, inverter overvoltage is detected and the inverter turns off the gate drives also. This causes powerdown and powerup when V_{BUS} < 109 %.

A bus undervoltage (V_{BUS} > 75 %) or inverter overvoltage during run mode is handled as a fault U. In this situation the IC changes into powerdown mode and generates a delay of 100 ms by an internal timer. Then startup conditions are checked and if valid, a further startup is initiated. If startup conditions are not valid, a further delay of 100 ms is generated.

This procedure is repeated a maximum of seven times. If startup is successful within these seven cycles, the situation is interpreted as a short interruption of the mains supply and the preheating is skipped. Any further startup attempt is initiated to include the preheating.

RFRUN (set R for run frequency, pin 9)

A resistor from this pin to ground sets the operating frequency of the inverter during run mode. The typical run frequency range is 20 kHz to 120 kHz. The set resistor R_RFRUN can be calculated, based on the run frequency f_{RUN} according to the equation:

$$R_{FRUN} = \frac{5 \cdot 10^8 \Omega Hz}{f_{RUN}}$$

RFPH (set R for preheat frequency, pin 10)

A resistor from this pin to ground, together with the resistor at pin 9, sets the operating frequency of the inverter during preheating mode. The typical preheating frequency range is from the run frequency (as a minimum) to 150 kHz. The set resistor R_RFPH can be calculated, based on the preheating frequency f_{PH} and the resistor R_{RFRUN} according to the equation:

$$R_{RFPH} = \frac{R_{RFRUN}}{\frac{f_{PH} \cdot R_{RFRUN}}{5 \cdot 10^8 \Omega Hz} - 1}$$

RTPH (set R for preheating time, pin 11)

A resistor from this pin to ground sets the preheating time of the inverter during preheating mode. A set resistor range from zero to 25 kΩ corresponds to a range of preheating times from zero to 2500 ms subdivided into 127 steps, as expressed below:

$$R_{RTPH} = \frac{t_{PreHeating}}{100 \frac{ms}{k\Omega}}$$

LVS (lamp voltage sense, pin 12)

Before startup this pin senses a current fed from the rectified line voltage via resistors through the high-side filaments of the lamp for detection of an inserted lamp.

The sensed current fed into the LVS pin has to exceed 12 µA typically at a voltage level of 6.0 V at the LVS pin. The reaction on the high side filament detection is mirrored at the RES pin (see pin 13). In addition, the detection of available mains supply after an interruption is sensed by this pin. Together with the RES pin, the IC can monitor the lamp removal of one lamp path (series connection of lamps is possible). If the functionality of this pin is not required, it can be disabled by connecting this pin to ground.

During run mode the lamp voltage is monitored with this pin by sensing a current proportional to the lamp voltage via resistors. An overload is indicated by an excessive lamp voltage. If the peak-to-peak lamp voltage causes a peak-to-peak current above a threshold of 210 μA_{PP} for longer than 620 µs, a fault EOL1 (end-of-life) is assumed. If the DC current at the LVS pin exceeds a threshold of ±42 µA for longer than 2500 ms, a fault EOL2 (rectifier effect) is assumed. The levels of AC sense current and DC sense current can be set separately by an external RC network. Note that in the case of deactivation of the LVS PIN, reactivation starts when the voltage at the LVS pin exceeds $V_{LVSEnable1}$ in RUN Mode.

RES (restart, pin 13)

A source current flowing out of this pin via resistor and filament to ground monitors the existence of the low-side filament of the fluorescent lamp for restart after lamp removal. A capacitor from this pin directly to ground eliminates a superimposed AC voltage that is generated as a voltage drop across the low-side filament. With a second sense resistor, the filament of a parallel lamp can be included in the lamp removal sensing. Note that during startup the chip supply voltage V_{cc} has to be below 14.0 V before V_{RES} reaches the filament detection level.

During typical start-up with connected filaments of the lamp a current source I_{RES3} (-21.3 µA) is active as long as V_{CC} > 10.6 V and V_{RES} < V_{RES1} (1.6 V). An open low-side filament is detected when V_{RES} > V_{RES1}. Such a condition will prevent the start-up of the IC. In addition, the comparator threshold is set to V_{RES2} (1.3 V) and the current source changes to I_{RES4} (-17.7 µA). The system is then waiting for a voltage level lower than V_{RES2} at the RES pin to indicate a connected low-side filament, which will enable the start-up of the IC.

An open high-side filament is detected when there is no sink current $I_{LVSSINK}$ (< 12 µA typ.) into the LVS pin before the V_{CC} start-up threshold is reached. Under these conditions the current source at the RES pin is I_{RES1} (-42.6 µA) as long as V_{CC} > 10.6 V and V_{RES} < V_{RES1} (1.6 V) and the current source is I_{RES2} (-35.4 µA) when the threshold has changed to V_{RES2} (1.3 V). In this way, the detection of the high-side filament is mirrored at the levels on the RES pin.

There is a further threshold of 3.2 V active at the RES pin during run mode. If the voltage level rises above this threshold for longer than 620 µs, the IC changes over into latched fault mode.

In any case of fault detection with different reaction times the IC turns off the gate drives and changes into powerdown mode with a current consumption of 170 µA max. An internal timer generates a delay time of 200 ms before start-up conditions are checked again. As soon as start-up conditions are valid, a second start-up attempt is initiated. If this second attempt fails, the IC remains in latched fault mode until a reset is generated by UVLO or lamp removal. The RES PIN can be deactivated by setting the PIN to GND (durable).

HSGND (high-side ground, pin 14)

This pin is connected to the source terminal of the high-side MOSFET, which is also the node of the high-side and low-side MOSFET. This pin represents the floating ground level of the high-side driver and the high-side supply.

HSVCC (high-side supply voltage, pin 15)

This pin provides the power supply of the high-side ground-related section of the IC. An external capacitor between pins 14 and 15 acts like a floating battery, which has to be recharged cycle by cycle via the high-voltage diode from low-side supply voltage during on-time of the low-side MOSFET. There is a UVLO threshold with hysteresis that enables the high-side section at 10.4 V and disables it at 8.6 V.

HSGD (high-side gate drive, pin 16)

The gate of the high-side MOSFET in a half-bridge inverter topology is controlled by this pin. There is an active L-level during UVLO and limitation of the max H-level at 11.0 V during normal operation. The switching characteristics are the same as described for LSGD (pin 1). It is recommended to use a resistor of about 10 Ω between the drive pin and gate in order to avoid oscillations and in order to shift the power dissipation of discharging the gate capacitance into this resistor. The dead time between LSGD signal and HSGD signals is self-adapting between 1.05 µs and 2.1 µs (typically).

2 Functional Description

This section describes applications and functionality of the chip.

2.1 Typical Application Circuitry

The schematic shown in **Figure 3** shows a typical application for a T5 single fluorescent lamp. It is designed for universal input voltage from 90 V_{AC} up to 270 V_{AC}. The following sections explain the components in reference to this schematic.

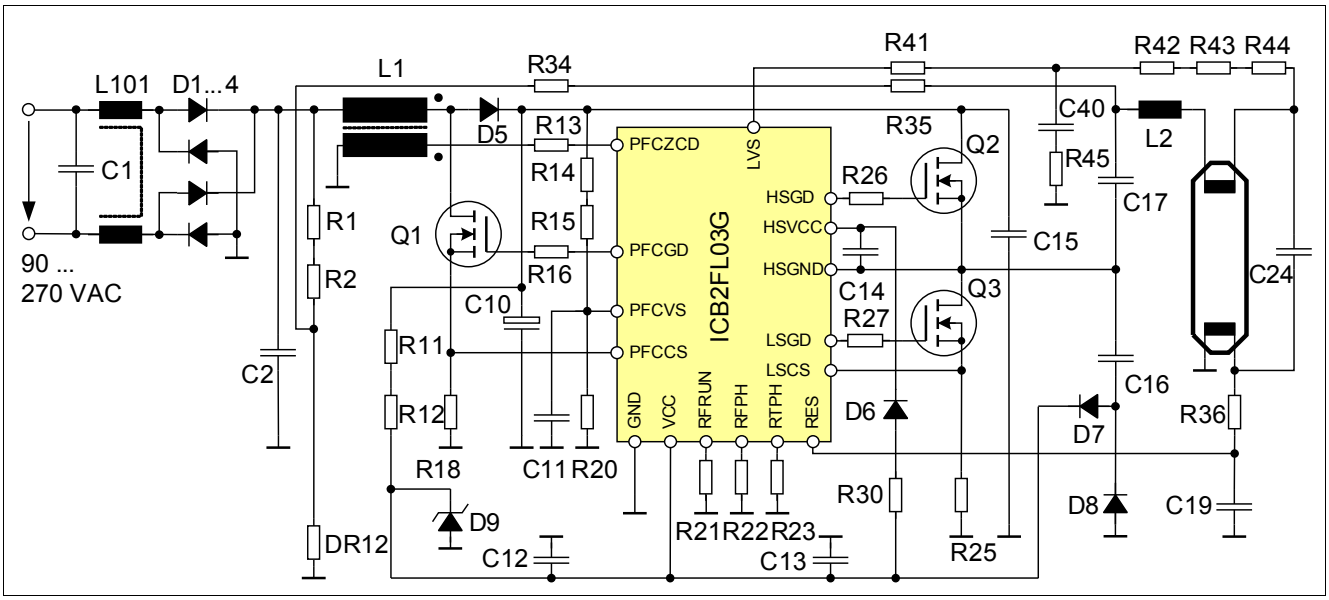

Figure 3 Application Circuit of Ballast for a Single Fluorescent Lamp (FL)

2.2 Normal Startup

This section describes the basic operation flow (8 phases) from the UVLO (Under Voltage Lock Out) into run mode without any error detection. For detailed information see **Section 2.2.1** and **Section 2.2.2**. **Figure 4** shows the 8 different phases during a typical start from UVLO (phase 1, **Figure 4**) to run mode (phase 8, **Figure 4**) and then into normal operation (no failure detected).

If the AC line input is switched ON, the V_{CC} voltage rises to the UVLO threshold V_{CC} = 10.6 V (no IC activity during UVLO). If V_{CC} exceeds the first threshold of V_{CC} = 10.6 V, the IC starts the first level of detection activity, the high and low side filament detection during the start-up hysteresis (phase 2, **Figure 4**).

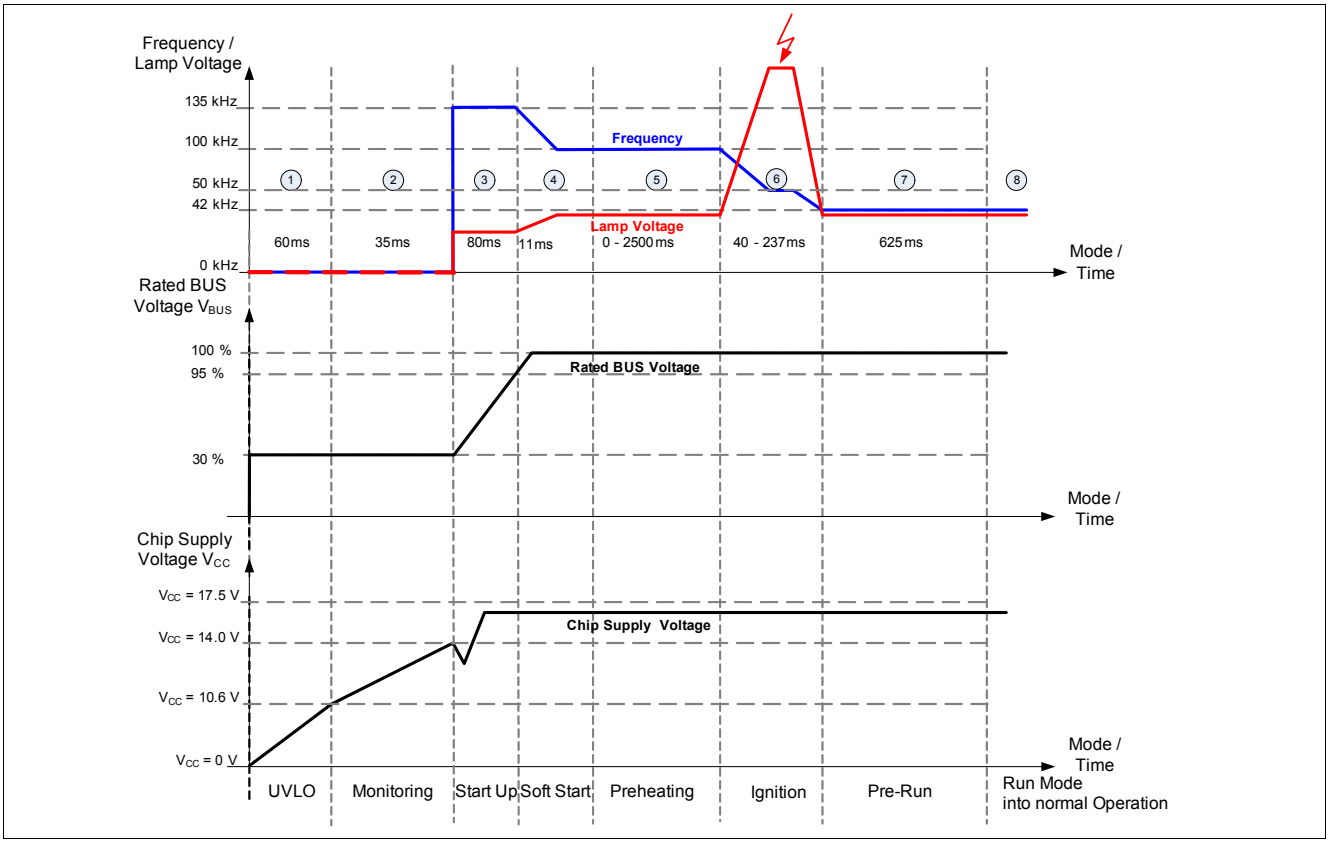

Figure 4 Typical Startup Procedure in Run Mode (in Normal Operation)

Followed at the end of the start-up hysteresis (phase 2, **Figure 4**) V_{CC} > 14.0 V and before phase 3 is active, a second level of detection activity senses for 130 µs (propagation delay of the IC) whether the bus voltage is between 12.5 % and 105 %. If the previous bus voltage conditions are fulfilled and the filaments are detected, the IC starts the operation with an internally fixed startup frequency of typically 135 kHz (all gates are active). If the bus voltage reaches a level of 95 % of the rated bus voltage within 80 ms at the latest (phase 3, **Figure 4**), the IC enters the soft start phase. During soft start (phase 4 , **Figure 4**), the start-up frequency shifts from 135 kHz down to the set preheating frequency (**Section 2.2.2**). In the soft start phase, the lamp voltage rises and the chip supply voltage reaches its working level from 10.6 V < V_{CC} < 17.5 V. After the soft start has finished, the IC enters the preheating mode (phase 5, **Figure 4**) for preheating the filaments (adjustable time) in order to extend the life cycle of the FL filaments. On finishing preheating, the controller starts ignition (phase 6, **Figure 4**). During the ignition phase, the frequency decreases from the set preheating frequency down to the set operation frequency (adjustable, see **Section 2.2.2**). If ignition is successful, the IC enters the pre-run mode (phase 7, **Figure 4**).

This mode is provided in order to prevent a malfunction of the IC due to an unstable system – e.g., the lamp parameters are not in a steady state condition. After finishing the 625 ms pre-run phase, the IC switches over to the run mode (phase 8, **Figure 4**) with complete monitoring.

2.2.1 Operating Levels from UVLO to Soft Start

This section describes the operating flow from phase 1 (UVLO) to phase 4 (soft start) in detail. The control of the ballast is able to start the operation within less than 100 ms (IC in active mode). This is achieved by a small start-up capacitor (about 1 µF C12 and C13 – fed by start-up resistors R11 and R12 in **Figure 3**) and the low current consumption during the UVLO (I_{VCC} = 130 µA – phase 1, **Figure 5**) and start-up hysteresis (I_{VCC} = 160 µA – defines the start-up resistors – phase 2, **Figure 5**) phases. The chip supply stage of the IC is protected against overvoltage via an internal Zener clamping network, which clamps the voltage at 16.3 V and allows a current of 2.5 mA. For clamping currents above 2.5 mA, an external Zener diode (D9, **Figure 3**) is required.[1)]

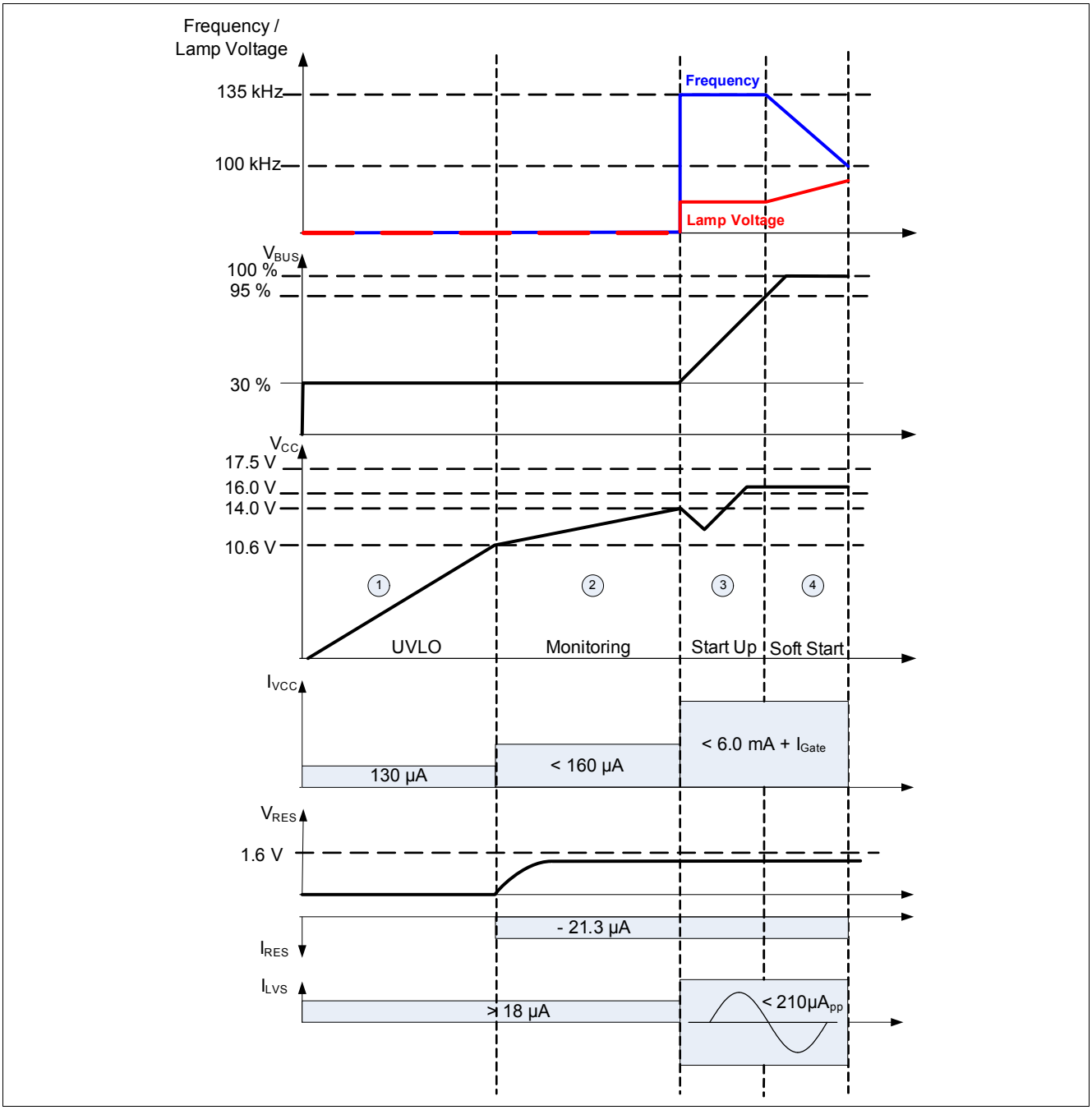

Figure 5 Typical Startup Procedure in Run Mode (in Normal Operation)

1) I_{Gate} depends on MOSFET

If V_{CC} exceeds the 10.6 V level and stays below 14.0 V (start-up hysteresis – phase 2, **Figure 5**), the IC checks whether the lamps are assembled by detecting a current across the filaments.

The low side filaments are checked from a source current of typical I_{RES3} = - 21.3 µA flowing out of pin 13 RES (**Figure 5** I_{RES}). This current produces a voltage drop of V_{RES} < 1.6 V (filament is ok) at the low side filament sense resistor (R 36 in **Figure 3**), connected to GND (via low side filament). An open low side filament is detected (see **Section 2.3.2**), when the voltage at the RES pin exceeds the V_{RES} > 1.6 V threshold (**Figure 5** V_{RES}).

The high side filaments are checked by a current of I_{LVS} > 12 µA typically via resistors R41, R42, R43 and R44 (**Figure 3**) into the LVS pin 12 (for a single lamp operation). An unused LVS pin has to be disabled via connection to GND. An open high side filament is detected (see **Section 2.3.3**) when there is no sink current into the LVS pin. This causes a higher source current out of the RES pin (typically 42.6 µA / 35.4 µA) in order to exceed V_{RES} > 1.6 V. In the case of defective filaments, the IC keeps monitoring until an adequate current from the RES or the LVS pin is present (e.g. in case of removal of a defective lamp).

When V_{CC} exceeds the 14.0 V threshold – by the end of the start-up hysteresis in phase 2 , **Figure 5** – the IC waits for 130 µs and senses the bus voltage. If the rated bus voltage is in the corridor of 12.5 % < $V_{BUSrated}$ < 105 %, the IC powers up the system and enters phase 3 (**Figure 5** $V_{BUSrated}$ > 95 % sensing); if not, the IC initiates a UVLO until the chip supply voltage falls below V_{CC} < 10.6 V. As soon as the condition for a power-up is fulfilled, the IC starts the inverter gate operation with an internal fixed start-up frequency of 135 kHz. The PFC gate drive starts with a delay of approx. 300 µs. Next, the bus voltage will be checked for a rated level above 95 % for a duration of 80 ms (phase 3, **Figure 5**). When leaving phase 3, the IC enters the soft start phase and shifts the frequency from the internal fixed start-up frequency of 135 kHz down to the set preheating frequency – e.g. f_{RFPH} = 100 kHz.

2.2.2 Operating Levels from Soft Start to Run Mode

This section describes the operating flow from phase 5 (preheating mode) to phase 8 (run mode) in detail. In order to extend the lifetime of the filaments, the controller enters – after the soft start phase – the preheating mode (phase 5, **Figure 6**). The preheating frequency is set by resistors R22 pin R_{FPH} to GND in combination with R21 (**Figure 3**) typ. 100 kHz e.g. R22 = 8.2 kΩ in parallel to R21 = 11.0 kΩ (see **Figure 3**, RFRUN pin). The preheating time can be selected by the programming resistor (R23 in **Figure 3**) at pin RTPH from 0 ms up to 2500 ms (phase 5, **Figure 6**).

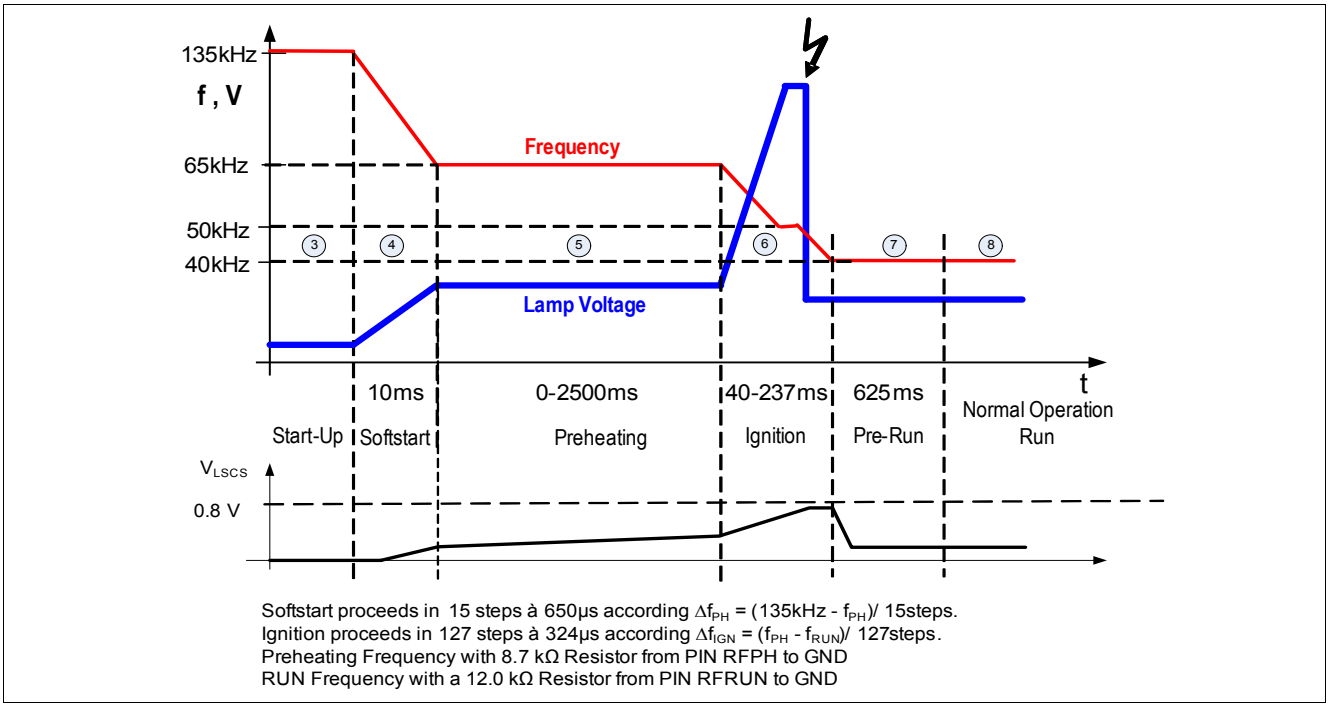

Figure 6 Typical Variation of Operating Frequency during Startup

During ignition (phase 6, **Figure 6**), the operating frequency of the inverter is shifted downward in t_{typ} = 40 ms (t_{max} = 237 ms) to the run frequency set by a resistor (R21 in **Figure 3**) at pin RFRUN to GND (typically 45 kHz with an 11.0 kΩ resistor). During this frequency shifting, the voltage and current in the resonant circuit will rise when the operation is close to the resonant frequency with increasing voltage across the lamp. The ignition control is activated if the sensed slope at the LSCS pin reaches typically 205 mV/µs ± 25 mV/µs and exceeds the 0.8 V threshold. This stops the decrease of the frequency and waits for ignition. The ignition control is now continuously monitored by the LSCS pin. The maximum duration of the ignition procedure is limited to 237 ms. If there is no ignition within this time frame, the ignition control is disabled and the IC changes over into the latched fault mode.

Furthermore, in order to reduce the size of the lamp choke, the ignition control is designed to operate with a lamp choke in magnetic saturation during ignition. For operation in magnetic saturation during ignition; the voltage at the shunt at the LSCS pin 2 has to be V_{LSCS} = 0.75 V when the ignition voltage is reached. If ignition is successful, the IC enters the pre-run mode (phase 7, **Figure 6**). The pre-run mode is a safety mode in order to prevent a malfunction of the IC due to an unstable system – e.g., the lamp parameters are not in a steady state condition. After 625 ms pre-run mode, the IC changes to the run mode (phase 8, **Figure 6**). The run mode monitors the complete system regarding bus over- and undervoltage, open loop, overcurrent of PFC and / or inverter, lamp overvoltage (EOL1) and rectifier effect (EOL2) (see **Section 2.5**) and capacitive loads 1 and 2 (see **Section 2.6**).

Figure 8 shows the lamp voltage versus the frequency during the different phases from preheating to the run mode. The lamp voltage rises by the end of the preheating phase with decreasing frequency (e.g., 100 kHz to 50 kHz) up to, for example, 700 V during ignition. After ignition, the lamp voltage drops down to its working level with continuous decreasing of the frequency (**Figure 8**) down to its working level e.g. 45 kHz (set by a resistor at the RFRUN pin to ground). After decreasing of the frequency stops, the IC enters the pre-run mode.

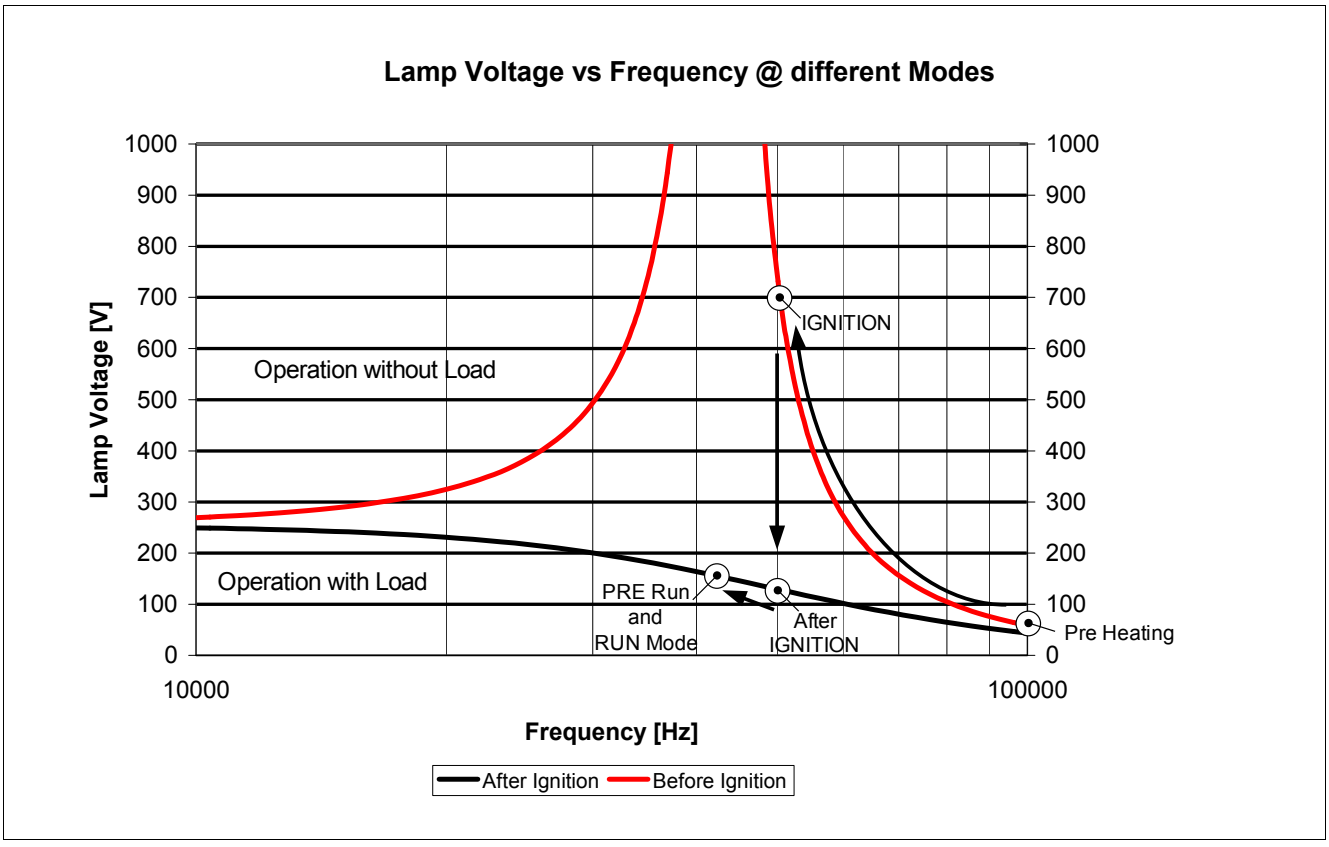

Figure 7 Lamp Voltage versus Frequency during the different Startup Phases

2.3 Filament Detection during Start-Up and Run Mode

The low and high side filament detection is sensed via the RES and the LVS pins. The low side filament detection during start-up and run mode is detected via the RES pin only. An open high side filament during start-up will be sensed via the LVS and the RES pins.

2.3.1 Start-Up with broken Low Side Filament

A source current of I_{RES3} = -21.3 µA from the RES pin (13) monitors the existence of a low side filament during a start-up (also in run mode). In the case of an open low side filament during the start-up hysteresis (10.6 V < V_{CC} < 14.0 V) a capacitor (C19 in **Figure 3**) will be charged up via I_{RES3} = -21.3 µA. When the voltage at the RES pin (13) exceeds V_{RES1} = 1.6 V, the controller prevents a power up and clamps the RES voltage internally at V_{RES} = 5.0 V. The gate drives of the PFC and inverter stage do not start working.

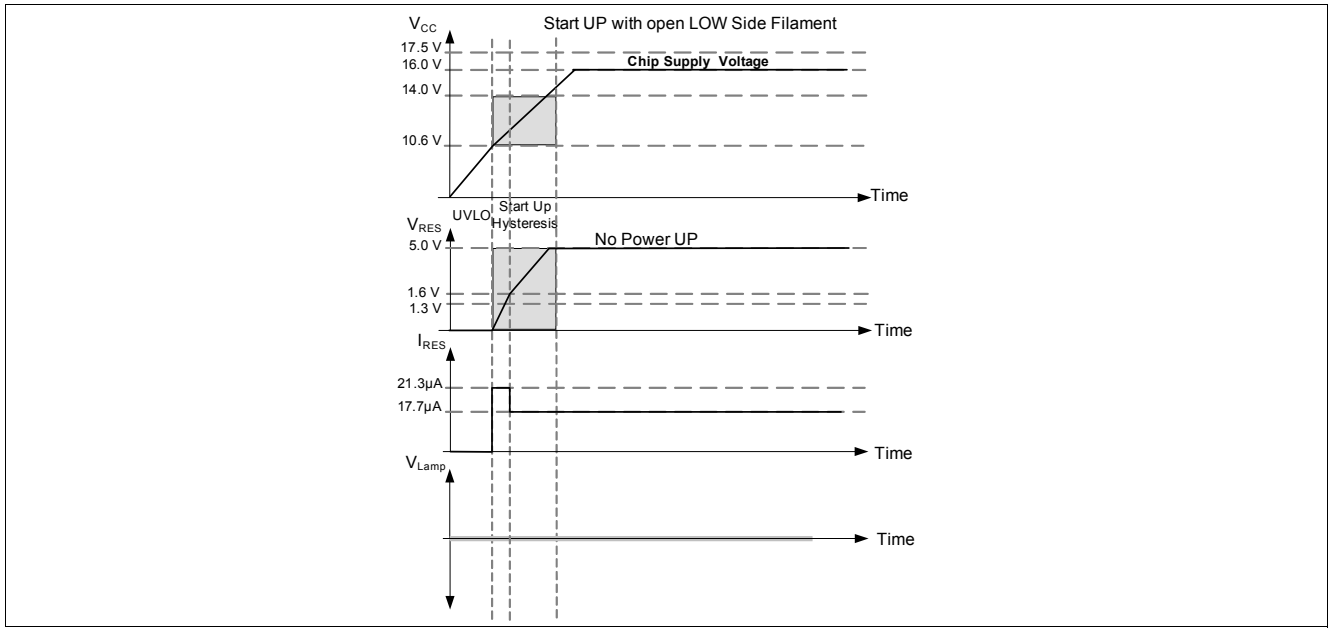

Figure 8 Start-Up with Open Low Side Filament

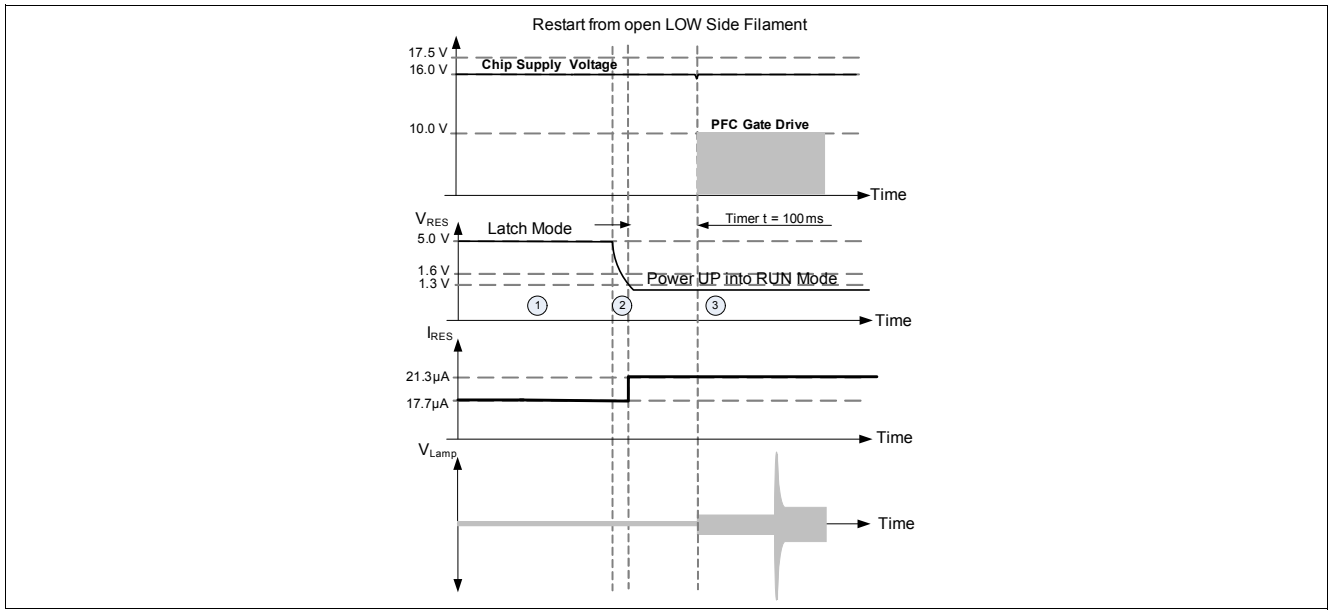

Figure 9 Restart from Open Low Side Filament

The IC comparators are then set to a threshold of V_{RES1} = 1.3 V and to I_{RES4} = - 17.7µA, the controller waits until the voltage at the RES pin drops below V_{RES1} = 1.3 V.

When a filament is present (**Figure 9**, section 2), the voltage drops below 1.3 V and the value of the source current out of the RES pin is set from I_{RES4} = -17.7 µA up to I_{RES3} = -21.3 µA. The controller then powers up the system, including soft start and preheating, into the run mode.

2.3.2 Low Side Filament Detection during Run Mode

In the case of an open low side filament during run mode, the current flowing out of the RES pin I_{RES3} = -21.3 µA charges up the capacitor C19 in **Figure 3**. If the voltage at the RES pin exceeds the V_{RES3} = 3.2 V threshold, the controller detects an open low side filament and stops the gate drives after a delay of t = 620 µs of an internal timer.

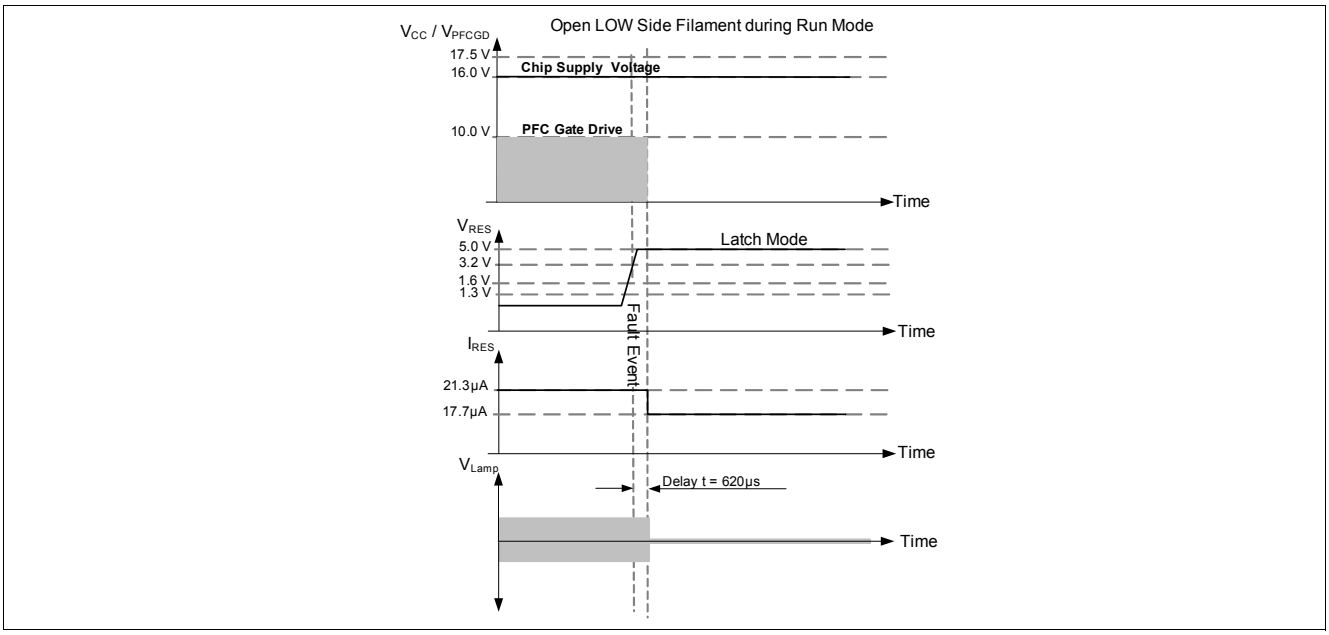

Figure 10 Open Low Side Filament Run Mode

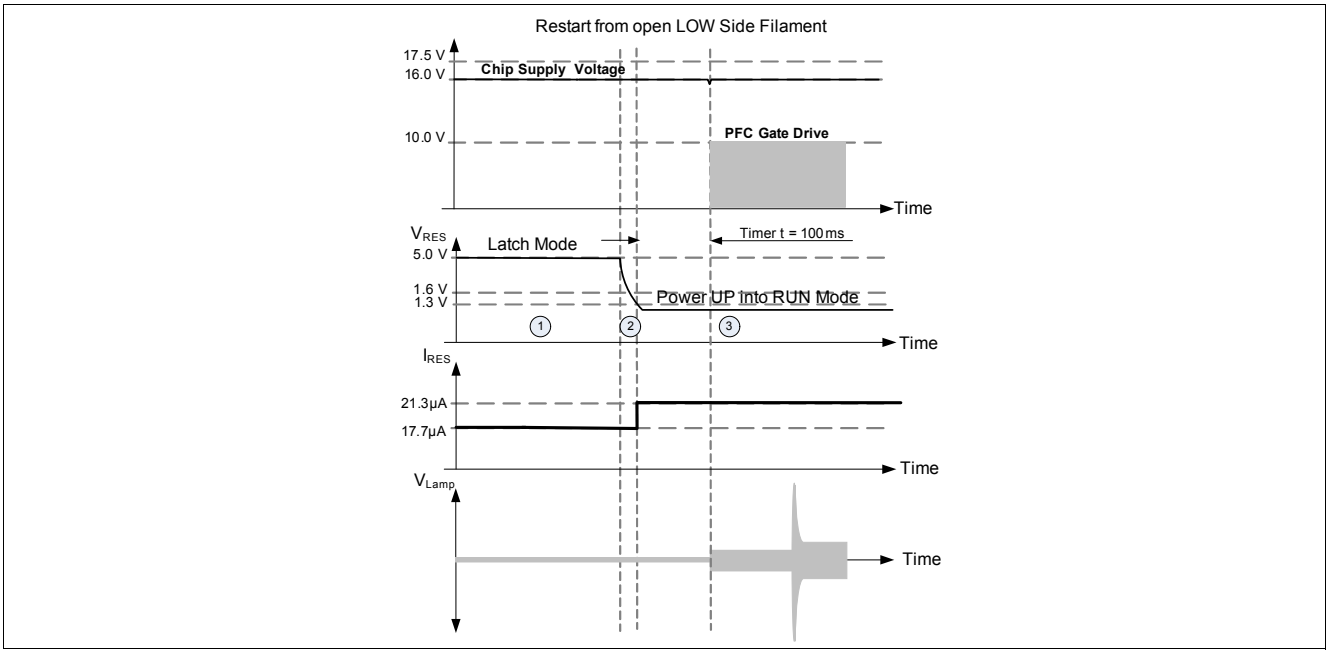

Figure 11 Restart from Open LS Filament

A restart is initiated when a filament is detected e.g. in the case of a lamp removal. If a filament is present (**Figure 11**, section 2), the voltage drops below 1.3 V and the value of the source current flowing out of the RES pin is set from I_{RES4} = -17.7 µA up to I_{RES3} = -21.3 µA. The controller powers up the system, including soft start and preheating, into the run mode (**Figure 11**, section 3).

2.3.3 Start-Up with Broken High Side Filament

An open high side filament during the start-up hysteresis (10.6 V < V_{CC} < 14.0 V) is detected when the current into the LVS pin 12 is below I_{LVS} = 12 µA (typically). In that case, the current flowing out of the RES pin 13 rises up to I_{RES1} = -42.6 µA. This causes the voltage at the RES pin to cross V_{RES1} = 1.6 V. The source current is now set to I_{RES2} = -35.4 µA and another threshold of V_{RES2} = 1.3 V is active. The controller prevents a power-up (see **Figure 12**), and the gate drives of the PFC and inverter stage do not start working.

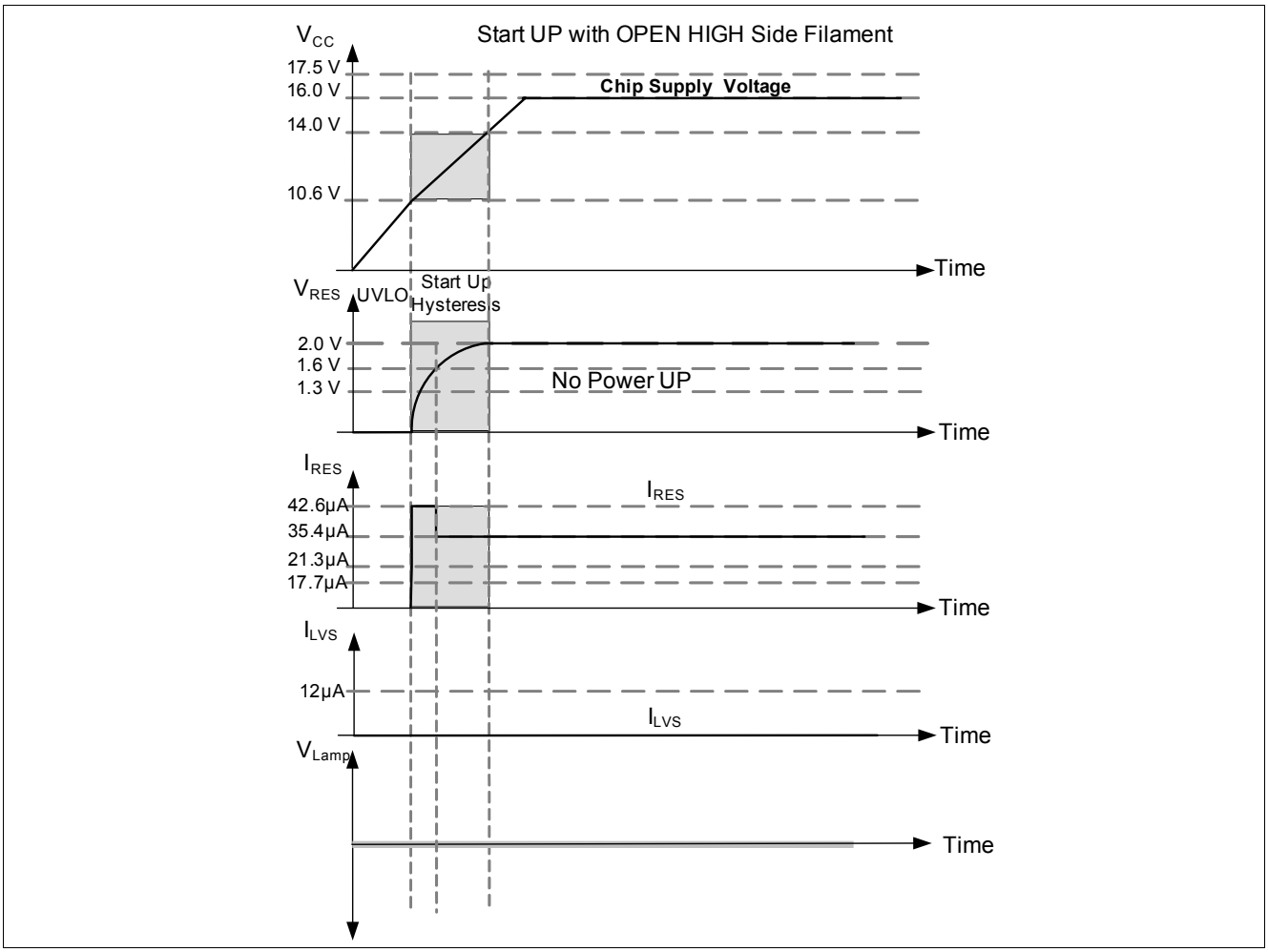

Figure 12 Start-Up with Open High Side Filament

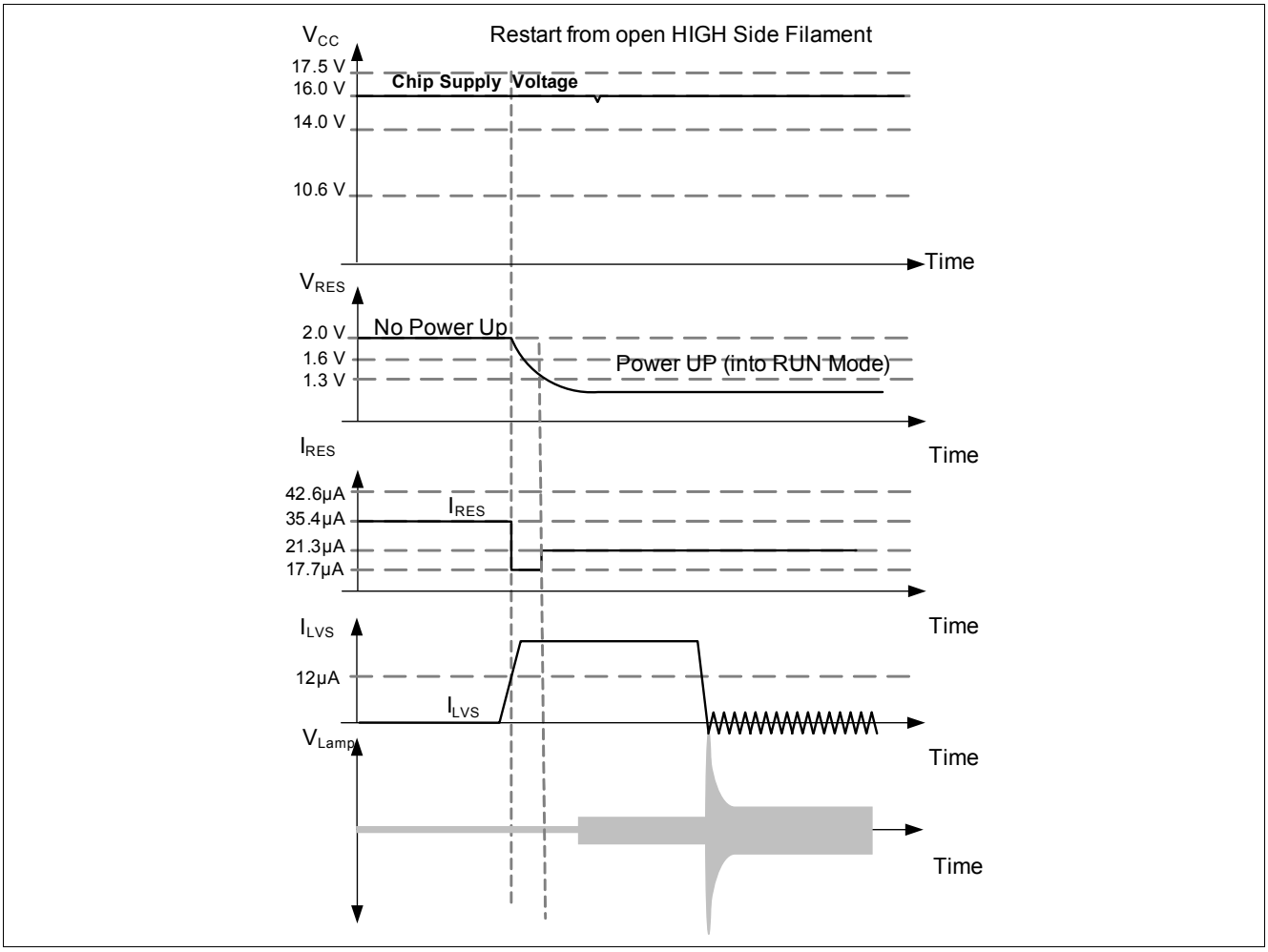

Figure 13 Restart from Open High Side Filament

When the high side filament is present, e.g. insertion of a lamp, the current of the active LVS pin exceeds I_{LVS} > 12 µA (typically), the RES current drops from I_{RES2} = -35.4 µA down to I_{RES4} = -17.7 µA (**Figure 13**). The controller then senses the low side filament. If a low side filament is also present, and the controller drops (after a short delay due to a capacitor at the RES pin) below V_{RES2} = 1.3 V, the RES current is set to I_{RES3} = -21.3 µA, and the controller powers up the system.

2.4 PFC Preconverter

2.4.1 Discontinuous Conduction and Critical Conduction Mode Operation

The digitally controlled PFC preconverter starts with an internally fixed ON time of typically t_{ON} = 4.0 µs and a variable frequency. The ON time is increased every 280 µs (typical) up to a maximum ON time of 24 µs. The control switches practically immediately from the discontinuous conduction mode (DCM) to critical conduction mode (CritCM) as soon as a sufficient ZCD signal becomes available. The frequency range in CritCM is 22 kHz to 500 kHz depending on the power (**Figure 14**), with a variation of the ON time from 24 µs > t_{ON} > 0.5µs.

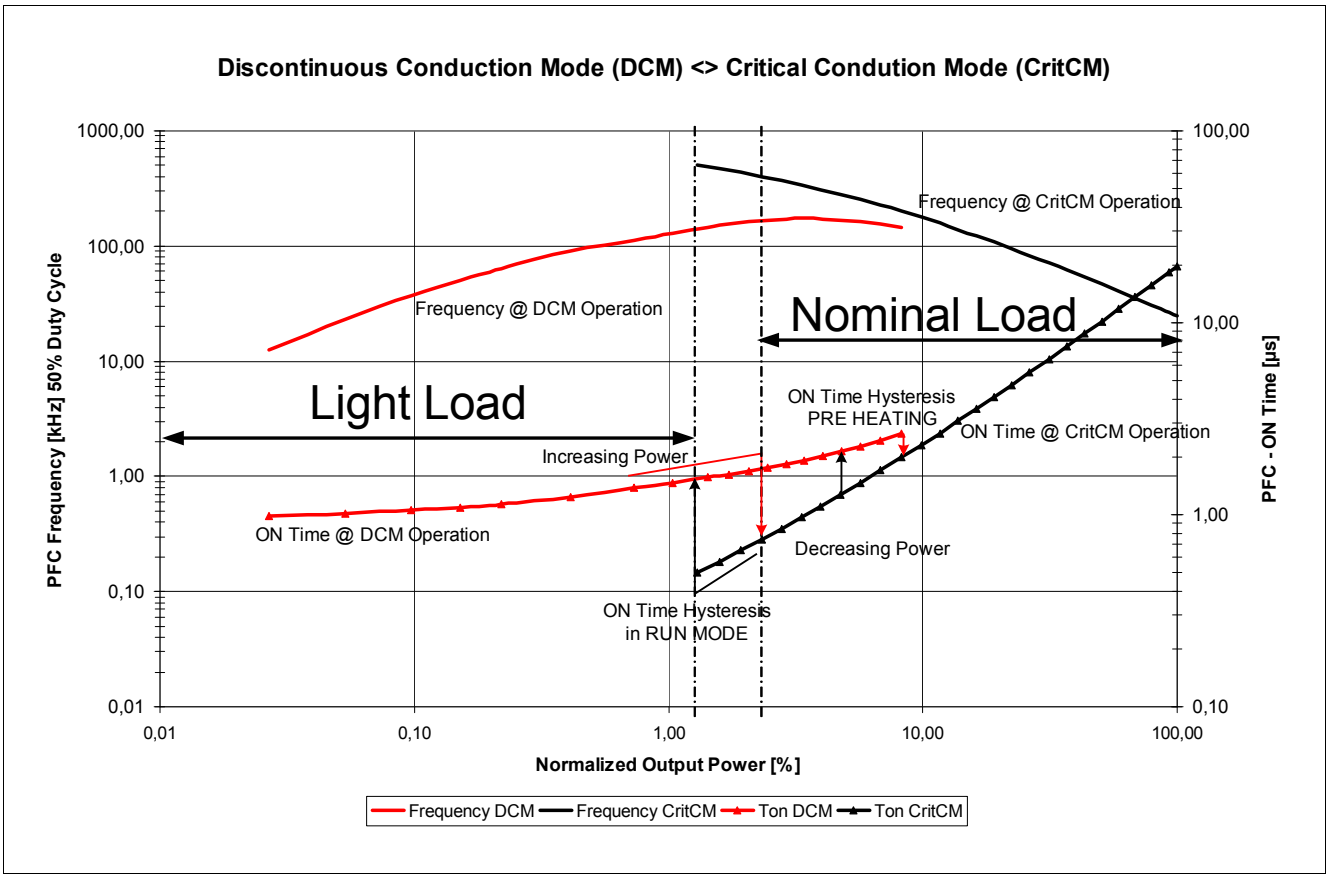

Figure 14 Operating Frequency and ON Time versus Power in DCM and CritCM Operation

For lower loads ($P_{OUTNorm}$ < 8 % from the normalized load[1)]) the control operates in discontinuous conduction mode (DCM) with an ON time from 4.0 µs and increasing OFF time. The frequency during DCM is variable in a range from 144 kHz down to typically 22 kHz @ 0.1 % load (**Figure 14**). With this control method, the PFC converter enables stable operation from 100 % load down to 0.1 %. **Figure 14** shows the ON time range in DCM and CritCM (Critical Conduction Mode) operation. In the overlapping area of CritCM and DCM there is a hysteresis of the ON time which causes a negligible frequency change.

2.4.2 PFC Bus Voltage Sensing

Overvoltage, open loop, bus 95 % and undervoltage states (**Figure 15**) of the PFC bus voltage are sensed at the PFCVS pin via the network R14, R15, R20 and C11 – **Figure 3** (C11 acts as a spike suppression filter).

1) Normalized power @ low line input voltage and maximum load

2.4.2.1 Bus Overvoltage and PFC Open Loop

The bus voltage loop control is completely integrated (**Figure 16**) and provided by an 8-bit sigma/delta A/D converter with a typical sampling rate of 280 µs and resolution of 4 mV/bit. After leaving phase 2 (monitoring), the IC starts power-up (V_{CC} > 14.0 V). After power-up, the IC senses the bus voltage below 12.5 % (open loop) or above 105 % (bus overvoltage) for 130 µs. In the case of bus overvoltage ($V_{BUSrated}$ > 109 %) or open loop ($V_{BUSrated}$ < 12.5 %) in phases 3 to 8, the IC shuts off the gate drives of the PFC within 5 µs or 1 µs respectively. In this case, the PFC restarts automatically when the bus voltage is within the corridor (12.5 % < $V_{BUSrated}$ < 105 %) again. Is the bus voltage valid after 130 µs, the bus voltage sensing is set to 12.5 % < $V_{BUSrated}$ < 109 %. If these thresholds are exceeded for longer than 1 µs (open loop) or 5 µs (overvoltage), the PFC gate drive stops working until the voltage drops below 105 % or exceeds the 12.5 % level. If the bus overvoltage (> 109 %) lasts for longer than 625 ms in run mode, the inverter gates also shut off and a power-down with complete restart is attempted (**Figure 15**).

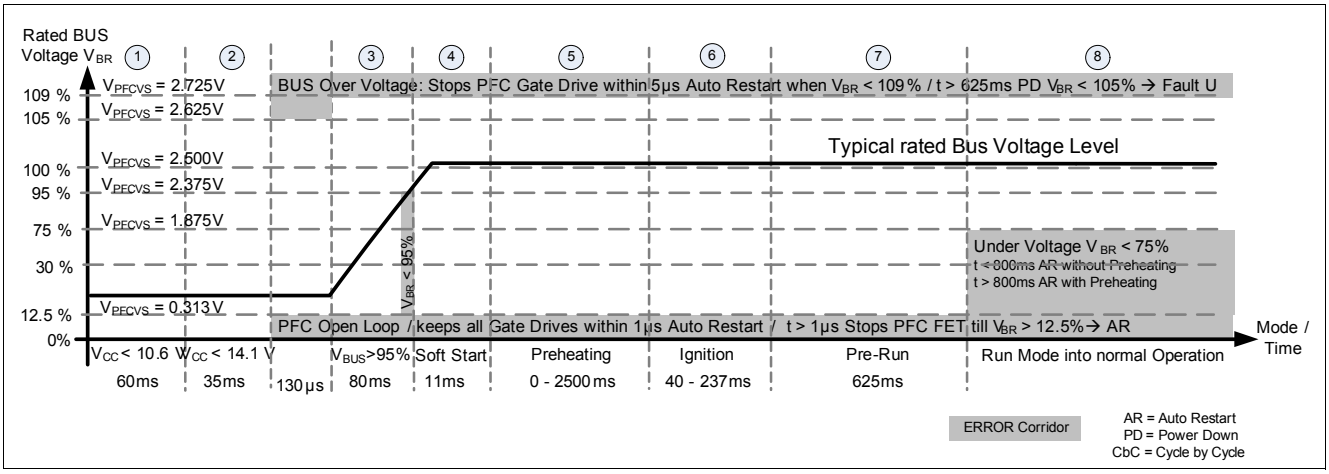

Figure 15 PFC Bus Voltage Operating Level and Error Detection

2.4.2.2 Bus Voltage 95 % and 75 % Sensing

When the rated bus voltage is in the corridor of 12.5 % < $V_{BUSrated}$ < 109 %, the IC will check whether the bus voltage exceeds the 95 % threshold (**Figure 15**, phase 3) within 80 ms before entering the soft start phase 4. Another threshold is activated when the IC enters the run mode (phase 8). If the rated bus voltage drops below 75 % for longer than 84 µs, a power-down with a complete restart is attempted when a counter exceeds 800 ms. In the case of short-term bus undervoltage (the bus voltage reaches its working level in run mode before exceeding typically 800 ms (min. 500 ms)) the IC skips phases 1 to 5 and starts with ignition (see **Section 2.7.1** for conditions for emergency lighting). The internal reference level of the bus voltage sense V_{PFCVS} is 2.5 V (100 % of the rated bus voltage) with a high accuracy. A surge protection is activated in the case of a rated bus voltage of V_{BUS} > 109 % and a low side current sense voltage of V_{LSCS} > 1.6 V in pre-run mode, or V_{LSCS} > 0.8 V in run mode for longer than 500 ns.

2.4.3 PFC Structure of Mixed Signals

A digital NOTCH filter eliminates the input voltage ripple independently of the mains frequency. A subsequent error amplifier with PI characteristic ensures stable operation of the PFC preconverter (**Figure 16**).

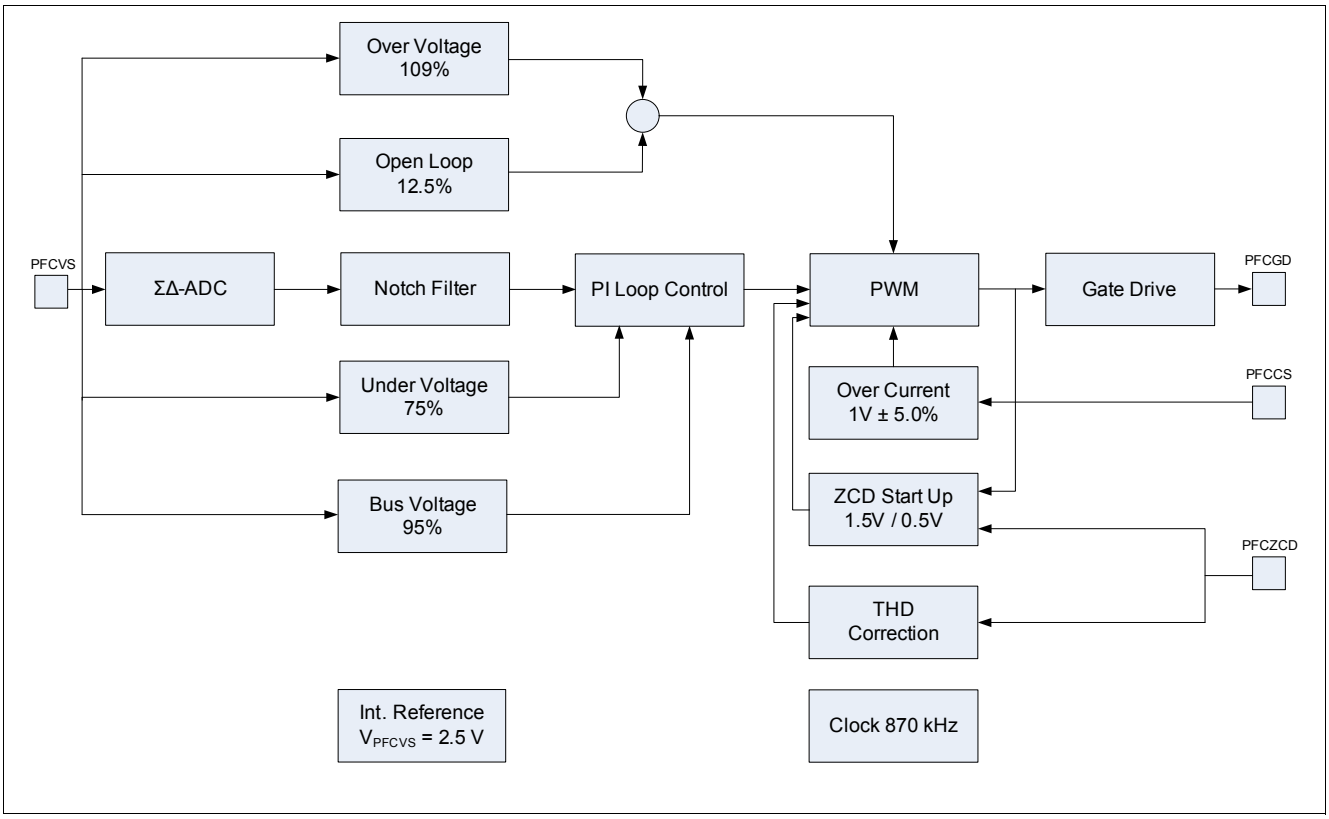

Figure 16 Structure of the Mixed Digital and Analog Control of the PFC Preconverter

The zero current detection (ZCD) is sensed by the PFCZCD pin via R13 (**Figure 3**). Notification of finished current flow during demagnetization is required in CritCM and in DCM also. The input is equipped with a special filtering system, including blanking of typically 500 ns and a large hysteresis of typically 0.5 V and 1.5 V V_{PFCZCD} (**Figure 16**).

2.4.4 THD Correction via ZCD Signal

An additional feature is the THD correction (**Figure 16**). In order to optimize the improved THD (especially in the zones A shown in **Figure 17** ZCD @ AC Input Voltage), there is a possibility to extend the pulse width of the gate signal (blue part of the PFC gate signal in **Figure 17**) with the variable PFC ZCD resistor (see resistor R13 in **Figure 3**) in addition to the gate signal controlled by the V_{PFCVS} signal (gray part of the PFC gate signal in **Figure 17**).