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# CoolSET™-F3

## ICE3A1065LJ

Off-Line SMPS Current Mode  
Controller with integrated 650V  
Startup Cell/Depletion CoolMOS™  
( Latched and frequency jitter  
Mode )

Power Management & Supply



Never stop thinking.

**CoolSET™-F3  
ICE3A1065LJ**

**Revision History: 2011-06-30**

**Datasheet**

Previous Version: 2.2

Page	Subjects (major changes since last revision)
22	revised outline dimension for PG-DIP-8 package

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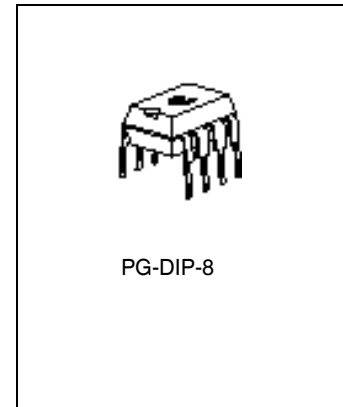
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### Off-Line SMPS Current Mode Controller with integrated 650V Startup Cell/Depletion CoolMOS™ ( Latched and frequency jitter Mode )



#### Product Highlights

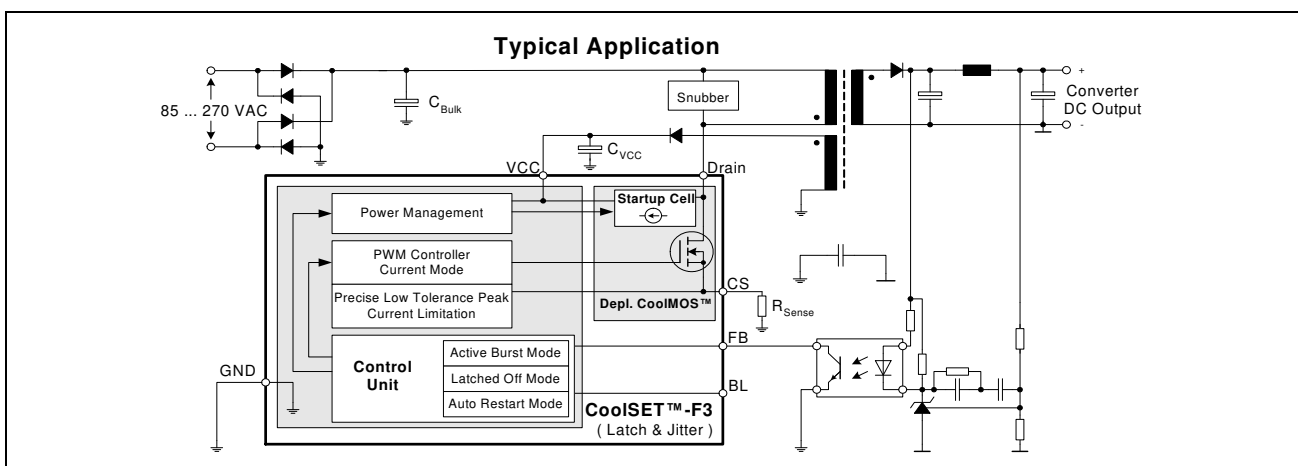
- Active Burst Mode to reach the lowest Standby Power Requirements < 100mW
- Built-in latched Off Mode and external latch enable function to increase robustness of the system
- Built-in and extendable blanking Window for high load jumps to increase system reliability
- Built-in soft start
- Frequency jitter for low EMI
- Pb-free lead plating; RoHS compliant

#### Features

- 650V avalanche rugged CoolMOS™ with built-in Startup Cell
- Active Burst Mode for lowest Standby Power
- Fast load jump response in Active Burst Mode
- 100kHz internally fixed switching frequency
- Built-in latched Off Mode for Overtemperature, Overvoltage & Short Winding Detection
- Auto Restart Mode for Overload, Open Loop & VCC Undervoltage
- Built-in Soft Start
- Built-in and extendable blanking Window for short duration high current
- External latch enable function
- Max Duty Cycle 75%
- Overall tolerance of Current Limiting < ±5%
- Internal PWM Leading Edge Blanking
- BiCMOS technology provide wide VCC range
- Frequency jitter and soft driving for low EMI

#### Description

The CoolSET™-F3 meets the requirements for Off-Line Battery Adapters and low cost SMPS for the lower power range. Adopting the BiCMOS technology, the IC can provide a wider VCC range up to 26V. Furthermore the Active Burst Mode is integrated to achieve the lowest Standby Power Requirements <100mW at no load and  $V_{in} = 270VAC$ . As the controller is always active during the Active Burst Mode, it is an immediate response on load jumps. And it leads to <1% ripple of the output voltage. In case of Overtemperature, Overvoltage or Short Winding, it enters into Latched Off Mode, which can be reset by recycling the AC main line. When there are open loop and overload conditions, it would enter Auto Restart Mode. In addition, an external latch enable function is provided for extra flexibility in protection. With the built-in soft start, the component count can be further reduced. The internal precise peak current limitation can effectively optimize the dimension of the transformer and the output diode. The built-in and extendable blanking window can prevent the mis-triggering of Auto Restart Mode. The frequency jitter mode can effectively reduce the EMI noise and further reduce the components in input filter.



Type	Package	Marking	V <sub>DS</sub>	F <sub>osc</sub>	R <sub>DSon</sub> <sup>1)</sup>	230VAC ±15% <sup>2)</sup>	85-265 VAC <sup>2)</sup>
ICE3A1065LJ	PG-DIP-8	ICE3A1065LJ	650V	100kHz	2.95	32W	16W

<sup>1)</sup> t<sub>yp</sub> @ T=25°C

<sup>2)</sup> Calculated maximum input power rating at T<sub>a</sub>=75°C, T<sub>f</sub>=125°C and without copper area as heat sink.



<b>Table of Contents</b>		<b>Page</b>
<b>1</b>	<b>Pin Configuration and Functionality</b> .....	5
1.1	Pin Configuration with PG-DIP-8 .....	5
1.2	Pin Functionality .....	5
<b>2</b>	<b>Representative Blockdiagram</b> .....	6
<b>3</b>	<b>Functional Description</b> .....	7
3.1	Introduction .....	7
3.2	Power Management .....	7
3.3	Startup Phase .....	8
3.4	PWM Section .....	9
3.4.1	Oscillator .....	9
3.4.2	PWM-Latch FF1 .....	9
3.4.3	Gate Driver .....	9
3.5	Current Limiting .....	10
3.5.1	Leading Edge Blanking .....	10
3.5.2	Propagation Delay Compensation .....	10
3.6	Control Unit .....	11
3.6.1	Basic and Extendable Blanking Mode .....	11
3.6.2	Active Burst Mode .....	12
3.6.2.1	Entering Active Burst Mode .....	12
3.6.2.2	Working in Active Burst Mode .....	12
3.6.2.3	Leaving Active Burst Mode .....	12
3.6.3	Protection Modes .....	13
3.6.3.1	Latched Off Mode .....	13
3.6.3.2	Auto Restart Mode .....	14
<b>4</b>	<b>Electrical Characteristics</b> .....	16
4.1	Absolute Maximum Ratings .....	16
4.2	Operating Range .....	16
4.3	Characteristics .....	17
4.3.1	Supply Section .....	17
4.3.2	Internal Voltage Reference .....	17
4.3.3	PWM Section .....	18
4.3.4	Soft Start time .....	18
4.3.5	Control Unit .....	18
4.3.6	Current Limiting .....	19
4.3.7	CoolMOS™ Section .....	20
<b>5</b>	<b>Temperature derating curve</b> .....	21
<b>6</b>	<b>Outline Dimension</b> .....	22
<b>7</b>	<b>Marking</b> .....	23
<b>8</b>	<b>Schematic for recommended PCB layout</b> .....	24

## Pin Configuration and Functionality

# 1 Pin Configuration and Functionality

## 1.1 Pin Configuration with PG-DIP-8

Pin	Symbol	Function
1	BL	Blanking and Latch
2	FB	Feedback
3	CS	Current Sense/ 650V <sup>1)</sup> Depl. CoolMOS™ Source
4	Drain	650V <sup>1)</sup> Depl. CoolMOS™ Drain
5	Drain	650V <sup>1)</sup> Depl. CoolMOS™ Drain
6	n.c.	Not Connected
7	VCC	Controller Supply Voltage
8	GND	Controller Ground

<sup>1)</sup> at  $T_j = 110^\circ\text{C}$

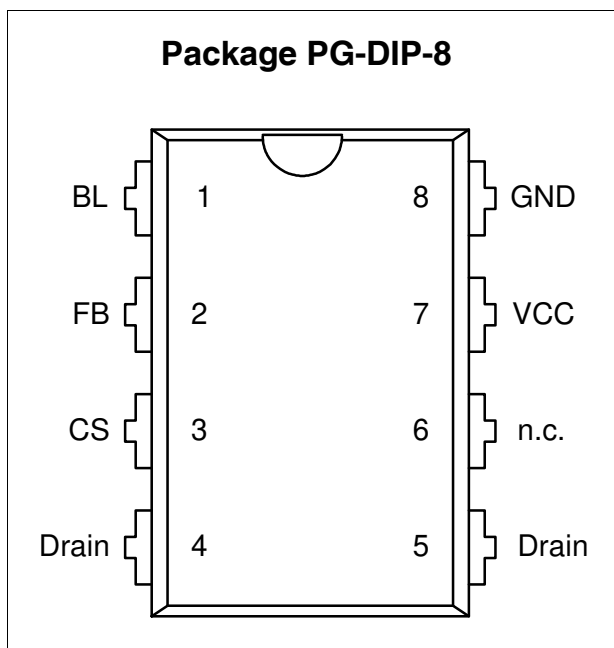


Figure 1 Pin Configuration PG-DIP-8(top view)

Note: Pin 4 and 5 are shorted within the DIP 8 package.

## 1.2 Pin Functionality

### BL (Blanking and Latch)

The BL pin combines the functions of extendable blanking time for entering the Auto Restart Mode and the external latch enable. The extendable blanking time function is to extend the built-in 20ms blanking time by adding an external capacitor at BL to ground. The external latch enable function is an external access to latch off the IC. It is triggered by pulling down the BL pin to less than 0.1V.

### FB (Feedback)

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle. The FB-Signal controls in case of light load the Active Burst Mode of the controller.

### CS (Current Sense)

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the integrated Depl. CoolMOS™. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.

### Drain (Drain of integrated Depl. CoolMOS™)

Pin Drain is the connection to the Drain of the internal Depl. CoolMOS™.

### VCC (Power supply)

The VCC pin is the positive supply of the IC. The operating range is between 10.5V and 26V.

### GND (Ground)

The GND pin is the ground of the controller.

## 2 Representative Blockdiagram

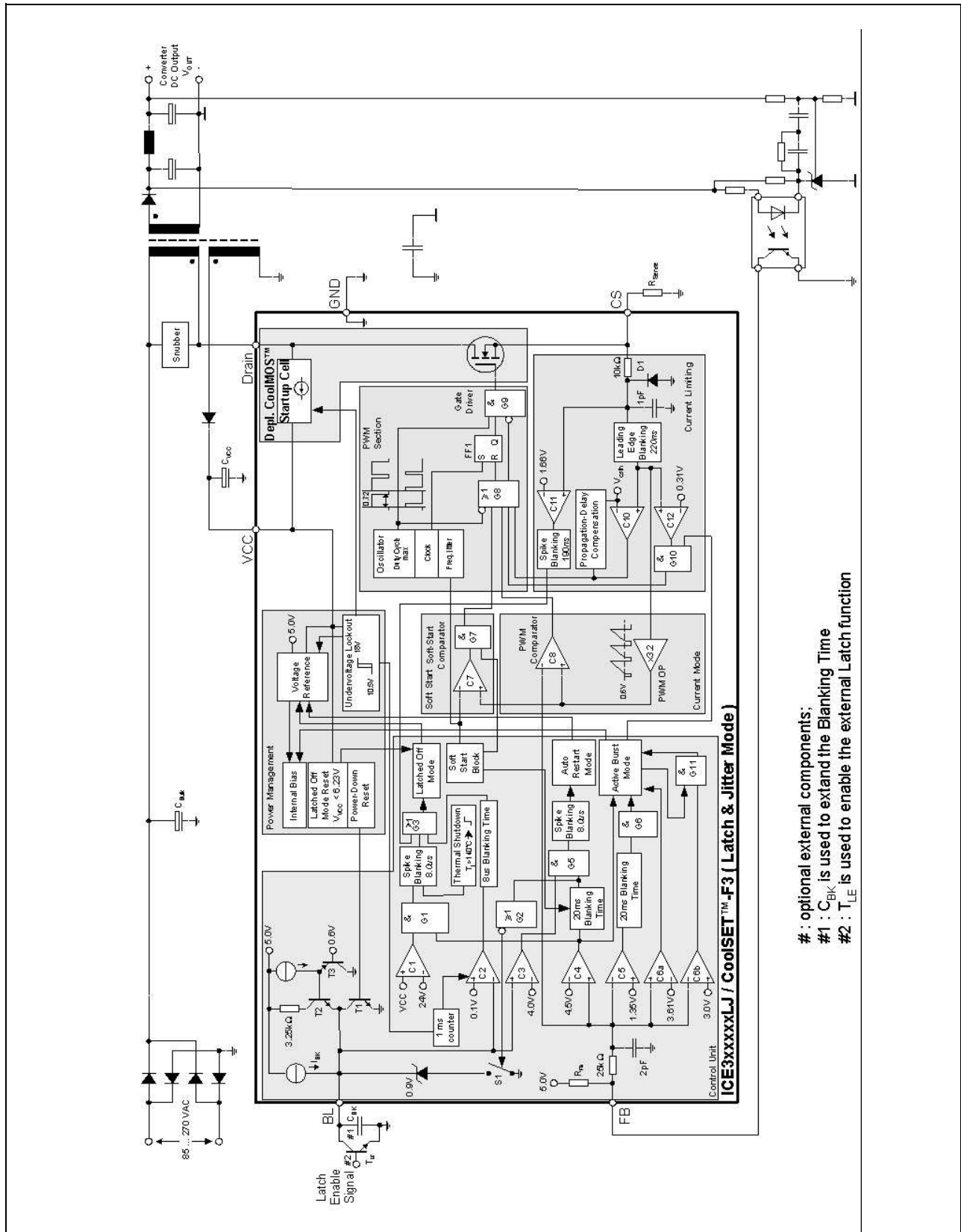


Figure 2 Representative Blockdiagram

### 3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

#### 3.1 Introduction

CoolSET™-F3 is the further development of the CoolSET™-F2 to meet the requirements for the lowest Standby Power at minimum load and no load conditions. A new fully integrated Standby Power concept is implemented into the IC in order to keep the application design easy. Compared to CoolSET™-F2 no further external parts are needed to achieve the lowest Standby Power. An intelligent Active Burst Mode is used for this Standby Mode. After entering this mode there is still a full control of the power conversion by the secondary side via the same optocoupler that is used for the normal PWM control. The response on load jumps is optimized. The voltage ripple on  $V_{out}$  is minimized.  $V_{out}$  is well controlled in this mode.

The usually external connected RC-filter in the feedback line after the optocoupler is integrated in the IC to reduce the external part count.

Furthermore a high voltage Startup Cell is integrated into the IC which is switched off once the Undervoltage Lockout on-threshold of 18V is exceeded. This Startup Cell is part of the integrated Depl. CoolMOS™. The external startup resistor is no longer necessary as this Startup Cell is connected to the Drain. Power losses are therefore reduced. This increases the efficiency under light load conditions drastically.

This version is adopting the BiCMOS technology and it can increase design flexibility as the  $V_{cc}$  voltage range is increased to 26V.

For this LJ version, the soft start is a built-in function. It is set at 20ms. Then it can save external component counts.

There are 2 modes of blanking time for high load jumps; the basic mode and the extendable mode. The blanking time for the basic mode is pre-set at 20ms while the extendable mode will increase the blanking time at basic mode by adding external capacitor at the BL pin. During this time window the overload detection is disabled. With this concept no further external components are necessary to adjust the blanking window.

In order to increase the robustness and safety of the system, the IC provides 2 levels of protection modes: Latched Off Mode and Auto Restart Mode. The Latched Off Mode is only entered under dangerous conditions which can damage the SMPS if not switched off immediately. A restart of the system can only be done by recycling the AC line. In addition, for this LJ version, there is an external Latch Enable function

provided to increase the flexibility in protection. When the BL pin is pulled down to less than 0.1V, the Latch Off Mode is triggered.

The Auto Restart Mode reduces the average power conversion to a minimum under unsafe operating conditions. This is necessary for a prolonged fault condition which could otherwise lead to a destruction of the SMPS over time. Once the malfunction is removed, normal operation is automatically retained after the next Start Up Phase.

The internal precise peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation. Therefore the maximum power is nearly independent on the input voltage which is required for wide range SMPS. There is no need for an extra over-sizing of the SMPS, e.g. the transformer or the secondary diode.

Furthermore, this LJ version implements the frequency jitter mode to the switching clock such that the EMI noise will be effectively reduced.

#### 3.2 Power Management

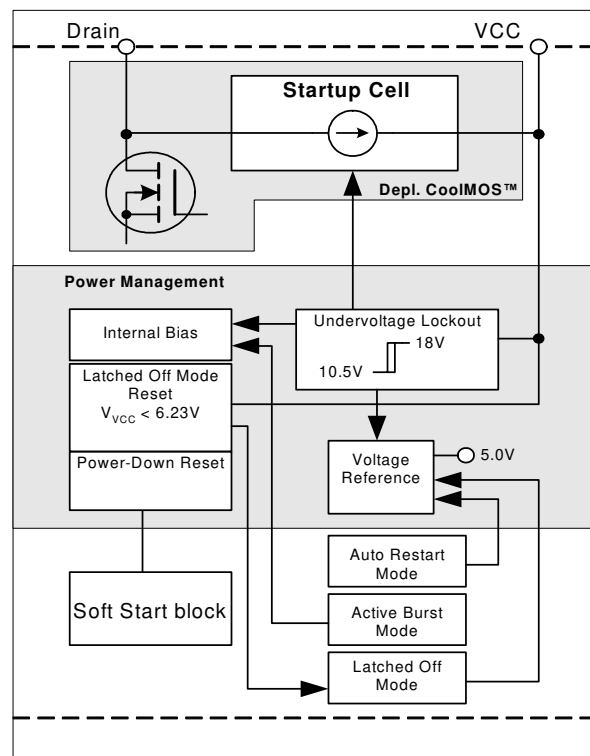


Figure 3 Power Management

The Undervoltage Lockout monitors the external supply voltage  $V_{VCC}$ . When the SMPS is plugged to the main line the internal Startup Cell is biased and starts



## Functional Description

to charge the external capacitor  $C_{VCC}$  which is connected to the VCC pin. This VCC charge current is controlled to 0.9mA by the Startup Cell. When the  $V_{VCC}$  exceeds the on-threshold  $V_{CCon}=18V$ , the bias circuit are switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore no power losses present due to the connection of the Startup Cell to the Drain voltage. To avoid uncontrolled ringing at switch-on a hysteresis start up voltage is implemented. The switch-off of the controller can only take place after Active Mode was entered and  $V_{VCC}$  falls below 10.5V. The maximum current consumption before the controller is activated is about  $250\mu A$ .

When  $V_{VCC}$  falls below the off-threshold  $V_{CCoff}=10.5V$ , the bias circuit switched off and the soft start counter is reset. Thus it is ensured that at every startup cycle the soft start starts at zero.

The internal bias circuit is switched off if Latched Off Mode or Auto Restart Mode is entered. The current consumption is then reduced to  $250\mu A$ .

Once the malfunction condition is removed, this block will then turn back on. The recovery from Auto Restart Mode does not require re-cycling the AC line. In case Latched Off Mode is entered, VCC needs to be lowered below 6.23V to reset the Latched Off Mode. This is done usually by re-cycling the AC line.

When Active Burst Mode is entered, the internal Bias is switched off most of the time but the Voltage Reference is kept alive in order to reduce the current consumption below  $450\mu A$ .

In the Startup Phase, the IC provides a Soft Start period to control the maximum primary current by means of a duty cycle limitation. The Soft Start function is a built-in function and it is controlled by an internal counter.

When the  $V_{VCC}$  exceeds the on-threshold voltage, the IC starts the Soft Start mode. The function is realized by an internal Soft Start resistor, a current sink and a counter. And the amplitude of the current sink is controlled by the counter.

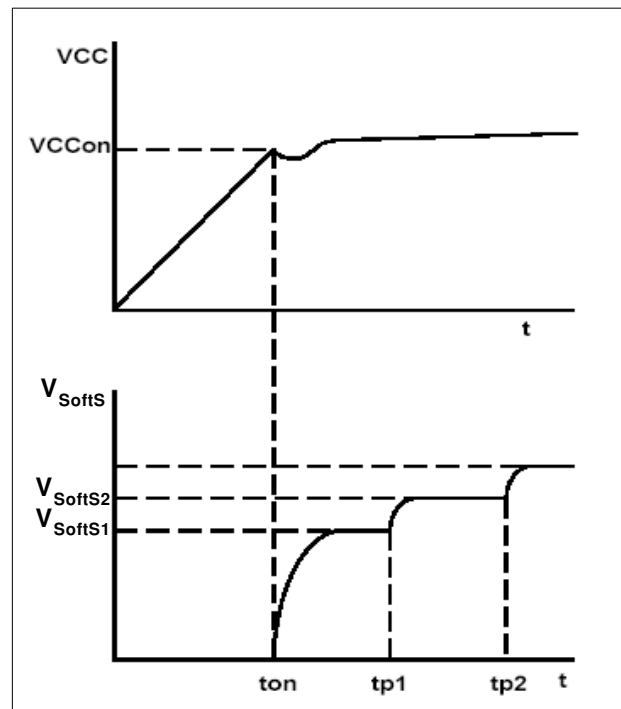


Figure 5 Soft Start Phase

### 3.3 Startup Phase

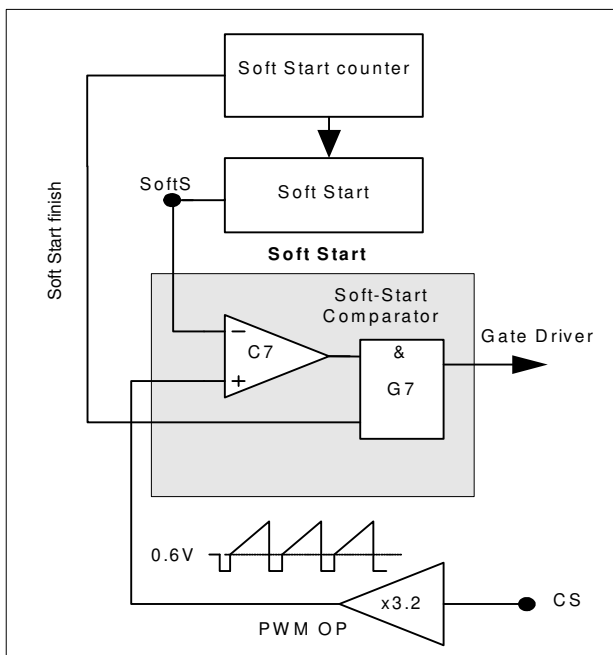


Figure 4 Soft Start

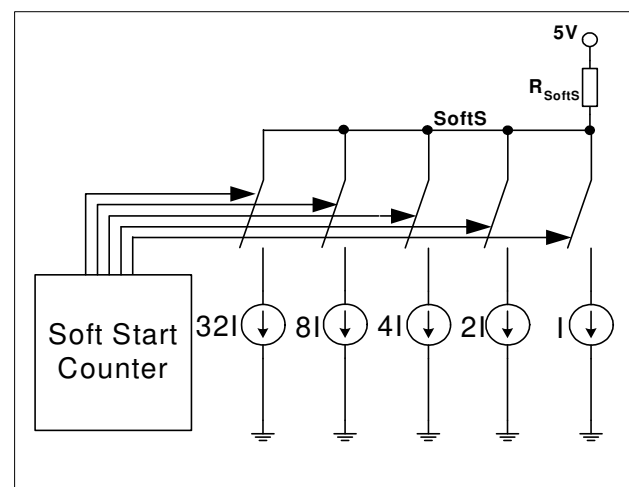


Figure 6 Soft Start Circuit

## Functional Description

After the IC is switched on, the  $V_{SoftS}$  voltage is controlled such that the voltage is increased stepwisely (32 steps) with the increase of the counts. The Soft Start counter would send a signal to the current sink control in every 600us such that the current sink decrease gradually and the duty ratio of the gate drive increase gradually. The Soft Start will be finished in 20ms after the IC is switched on. At the end of the Soft Start period, the current sink is switched off.

### 3.4 PWM Section

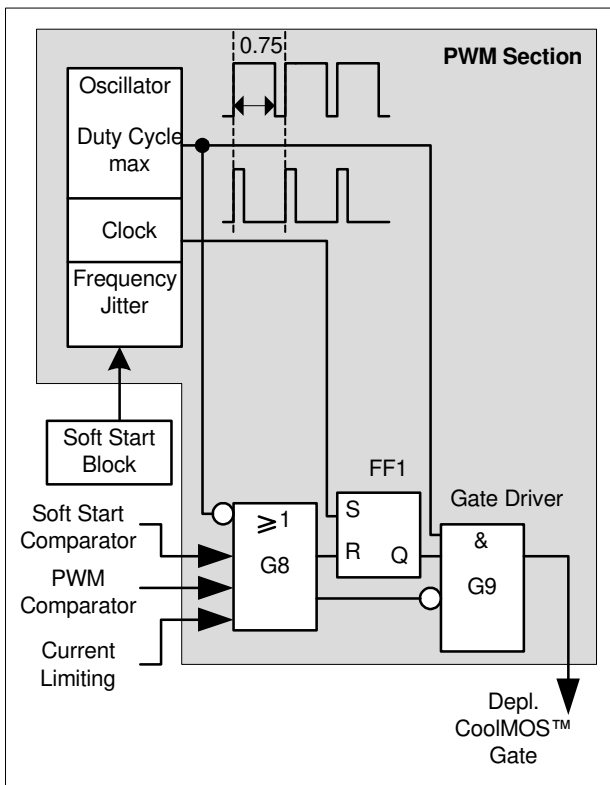


Figure 7 PWM Section Block

#### 3.4.1 Oscillator

The oscillator generates a fixed frequency of 100KHz with frequency jittering of  $\pm 4\%$  (which is  $\pm 4\text{KHz}$ ) at a jittering period of 4ms.

A capacitor, a current source and a current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of  $D_{max}=0.75$ .

Once the Soft Start period is over and when the IC goes into normal operating mode, the switching frequency of the clock is varied by the control signal from the Soft Start block. Then the switching frequency is varied in range of  $100\text{KHz} \pm 4\text{KHz}$  at period of 4ms.

#### 3.4.2 PWM-Latch FF1

The output of the oscillator block provides continuous pulse to the PWM-Latch which turns on/off the internal Depl. CoolMOS™. After the PWM-Latch is set, it is reset by the PWM comparator, the Soft Start comparator or the Current-Limit comparator. When it is in reset mode, the output of the driver is shut down immediately.

#### 3.4.3 Gate Driver

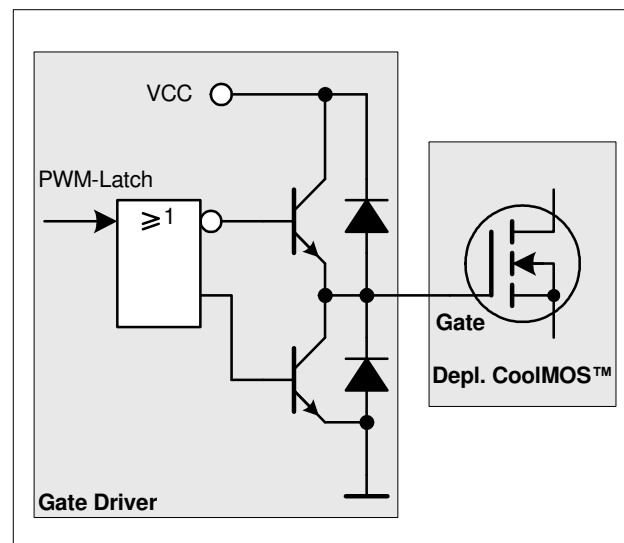


Figure 8 Gate Driver

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when exceeding the internal CoolMOS™ threshold. This is achieved by a slope control of the rising edge at the driver's output (see Figure 9).

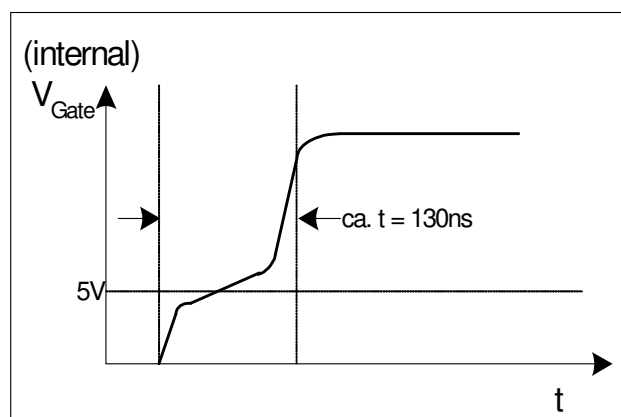


Figure 9 Gate Rising Slope

Thus the leading switch on spike is minimized. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

## Functional Description

During power up, when VCC is below the undervoltage lockout threshold  $V_{VCCoff}$ , the output of the Gate Driver is set to low in order to disable power transfer to the secondary side.

### 3.5 Current Limiting

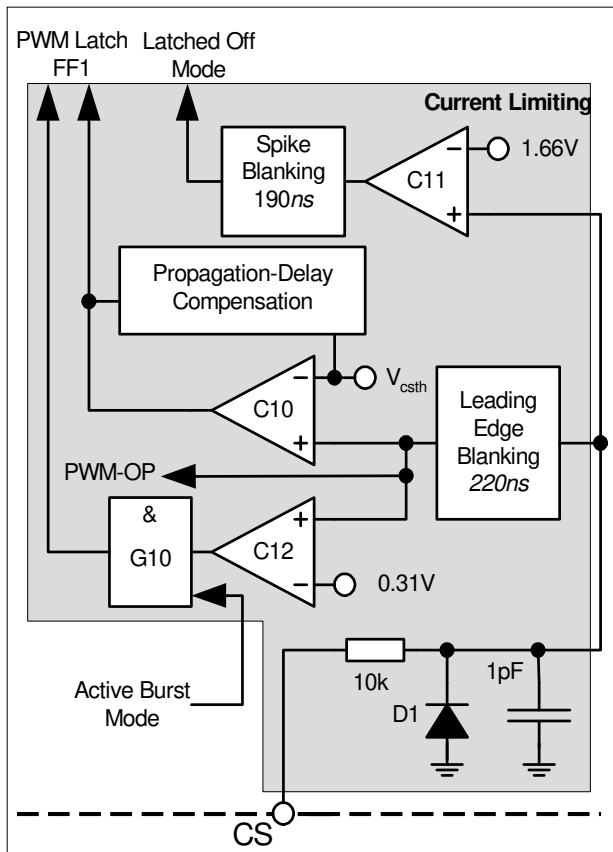


Figure 10 Current Limiting Block

There is a cycle by cycle peak current limiting operation realized by the Current-Limit comparator C10. The source current of the integrated Depl. CoolMOS™ is sensed via an external sense resistor  $R_{Sense}$ . By means of  $R_{Sense}$  the source current is transformed to a sense voltage  $V_{Sense}$  which is fed into the pin CS. If the voltage  $V_{Sense}$  exceeds the internal threshold voltage  $V_{csth}$ , the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1.

A Propagation Delay Compensation is added to support the immediate shut down of the integrated Depl. CoolMOS™ with very short propagation delay. Thus the influence of the AC input voltage on the maximum output power can be reduced to minimal.

In order to prevent the current limit from distortions caused by leading edge spikes, a Leading Edge Blanking is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the Gate G10 if Active Burst Mode is entered. When it is

activated, the current limiting is reduced to 0.31V. This voltage level determines the maximum power level in Active Burst Mode.

Furthermore, the comparator C11 is implemented to detect dangerous current levels which could occur if there is a short winding in the transformer or the secondary diode is shorted. To ensure that there is no accidentally entering of the Latched Mode by the comparator C11, a 190ns spike blanking time is integrated in the output path of comparator C11.

#### 3.5.1 Leading Edge Blanking

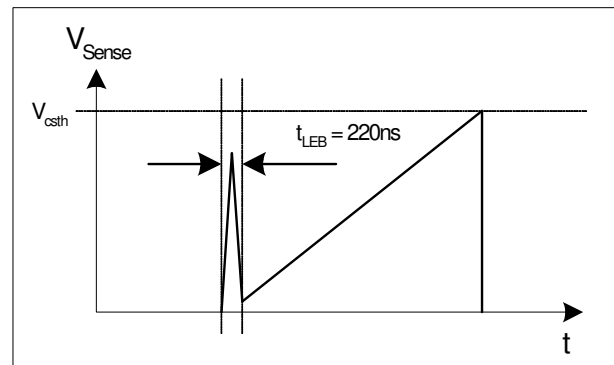


Figure 11 Leading Edge Blanking

Whenever the internal Depl. CoolMOS™ is switched on, a leading edge spike is generated due to the primary-side capacitances and reverse recovery time of the secondary-side rectifier. This spike can cause the gate drive to switch off unintentionally. In order to avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of  $t_{LEB} = 220ns$ .

#### 3.5.2 Propagation Delay Compensation

In case of overcurrent detection, there is always propagation delay to switch off the internal Depl. CoolMOS™. An overshoot of the peak current  $I_{peak}$  is induced to the delay, which depends on the ratio of  $dI/dt$  of the peak current (see Figure 12).

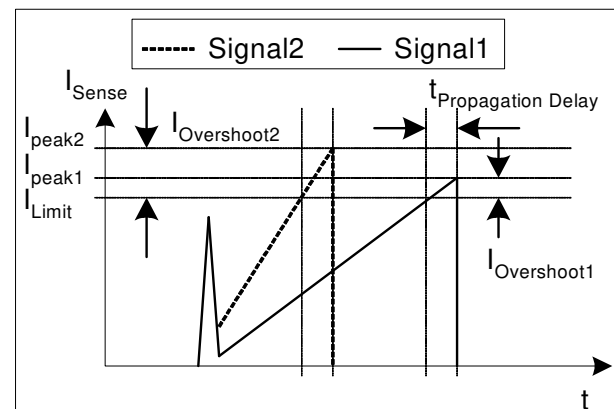


Figure 12 Current Limiting

## Functional Description

The overshoot of Signal2 is larger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to reduce the overshoot due to  $di/dt$  of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold  $V_{csth}$  and the switching off of the integrated internal Depl. CoolMOS™ is compensated over temperature within a wide range. Current Limiting is then very accurate.

For example,  $I_{peak} = 0.5A$  with  $R_{Sense} = 2$ . The current sense threshold is set to a static voltage level  $V_{csth} = 1V$  without Propagation Delay Compensation. A current ramp of  $di/dt = 0.4A/\mu s$ , or  $dV_{Sense}/dt = 0.8V/\mu s$ , and a propagation delay time of  $t_{Propagation\ Delay} = 180ns$  leads to an  $I_{peak}$  overshoot of 14.4%. With the propagation delay compensation, the overshoot is only around 2% (see Figure 13).

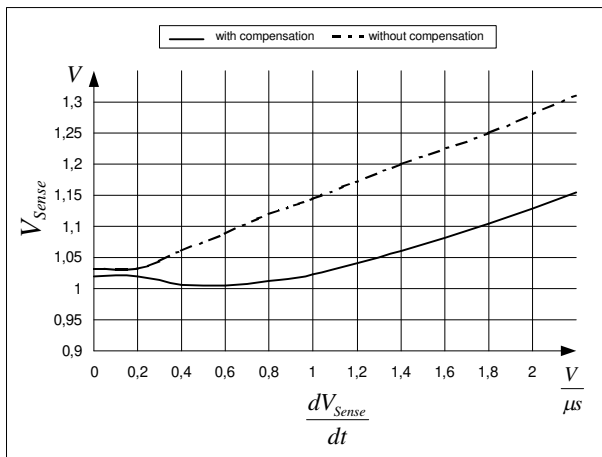


Figure 13 Overcurrent Shutdown

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage  $V_{csth}$  (see Figure 14). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

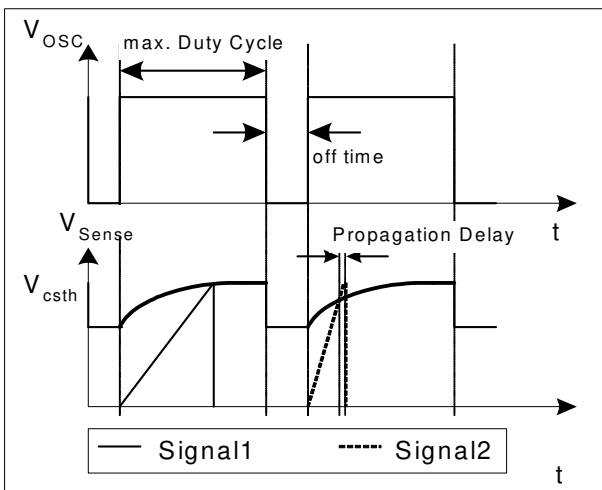


Figure 14 Dynamic Voltage Threshold  $V_{csth}$

### 3.6 Control Unit

The Control Unit contains the functions for Active Burst Mode, Auto Restart Mode and Latched Off Mode. The Active Burst Mode and the Auto Restart Mode both have 20ms internal Blanking Time. For the Auto Restart Mode, a further extendable Blanking Time is achieved by adding external capacitor at BL pin. By means of this Blanking Time, the IC avoids entering into these two modes accidentally. Furthermore those buffer time for the overload detection is very useful for the application that works in low current but requires a short duration of high current occasionally.

#### 3.6.1 Basic and Extendable Blanking Mode

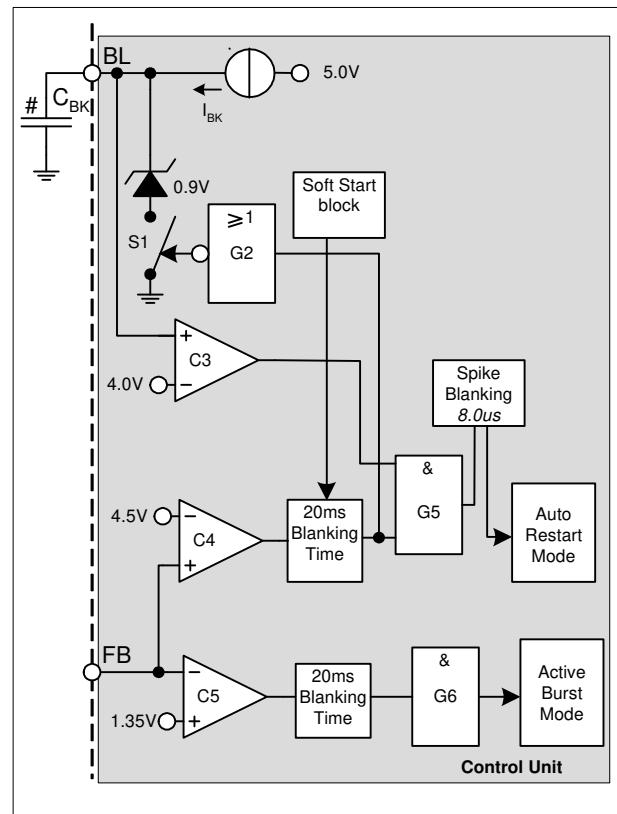


Figure 15 Basic and Extendable Blanking Mode

There are 2 kinds of Blanking mode; basic mode and the extendable mode. The basic mode has an internal pre-set 20ms blanking time while the extendable mode has extended blanking time to basic mode by connecting an external capacitor to the BL pin. For the extendable mode, the gate G5 is blocked even though the 20ms blanking time is reached if an external capacitor  $C_{BK}$  is added to BL pin. While the 20ms blanking time is passed, the switch S1 is opened by G2. Then the 0.9V clamped voltage at BL pin is charged to 4.0V through the internal  $I_{BK}$  constant current. Then G5 is enabled by comparator C3. After

## Functional Description

the 8.0us spike blanking time, the Auto Restart Mode is activated.

For example, if  $C_{BK} = 0.22\mu\text{F}$ ,  $I_{BK} = 8.4\mu\text{A}$

Blanking time = 20ms +  $C_{BK} \times (4.0 - 0.9) / I_{BK} = 100\text{ms}$

The 20ms blanking time circuit after C4 is disabled by the soft stat block such that the controller can start up properly.

The Active Burst Mode has basic blanking mode only while the Auto Restart Mode has both the basic and the extendable blanking mode.

### 3.6.2 Active Burst Mode

The IC enters Active Burst Mode under low load conditions. With the Active Burst Mode, the efficiency increases significantly at light load conditions while still maintaining a low ripple on  $V_{OUT}$  and a fast response on load jumps. During Active Burst Mode, the IC is controlled by the FB signal. Since the IC is always active, it can be a very fast response to the quick change at the FB signal. The Start up Cell is kept OFF in order to minimize the power loss.

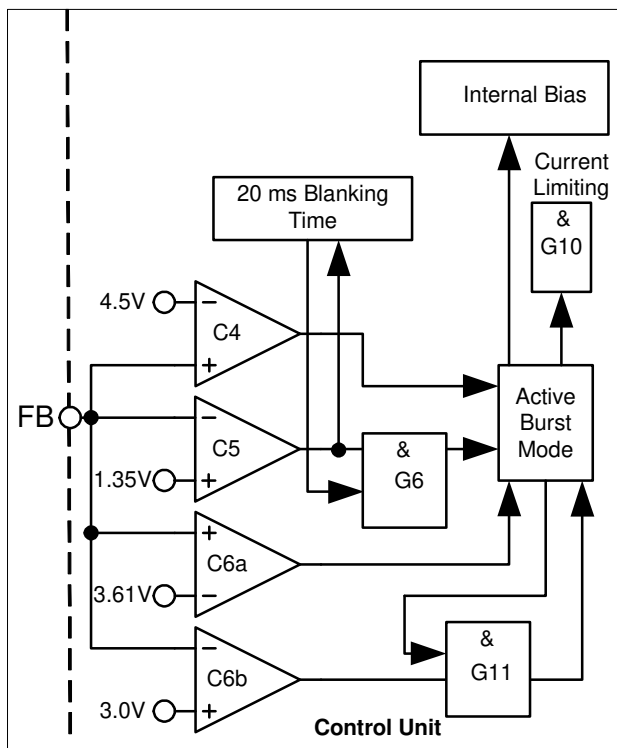


Figure 16 Active Burst Mode

The Active Burst Mode is located in the Control Unit. Figure 16 shows the related components.

#### 3.6.2.1 Entering Active Burst Mode

The FB signal is kept monitoring by the comparator C4. During normal operation, the internal blanking time counter is reset to 0. When FB signal falls below 1.35V,

it starts to count. When the counter reach 20ms and FB signal is still below 1.35V, the system enters the Active Burst Mode. This time window prevents a sudden entering into the Active Burst Mode due to large load jumps.

After entering Active Burst Mode, a burst flag is set and the internal bias is switched off in order to reduce the current consumption of the IC to approx. 450uA.

It needs the application to enforce the VCC voltage above the Undervoltage Lockout level of 10.5V such that the Startup Cell will not be switched on accidentally. Or otherwise the power loss will increase drastically. The minimum VCC level during Active Burst Mode depends on the load condition and the application. The lowest VCC level is reached at no load condition.

#### 3.6.2.2 Working in Active Burst Mode

After entering the Active Burst Mode, the FB voltage rises as  $V_{OUT}$  starts to decrease, which is due to the inactive PWM section. The comparator C6a monitors the FB signal. If the voltage level is larger than 3.61V, the internal circuit will be activated; the Internal Bias circuit resumes and starts to provide switching pulse. In Active Burst Mode the gate G10 is released and the current limit is reduced to 0.31V. In one hand, it can reduce the conduction loss and the other hand, it can reduce the audible noise. If the load at  $V_{OUT}$  is still kept unchanged, the FB signal will drop to 3.0V. At this level the C6b deactivates the internal circuit again by switching off the internal Bias. The gate G11 is active again as the burst flag is set after entering Active Burst Mode. In Active Burst Mode, the FB voltage is changing like a saw tooth between 3.0V and 3.61V (see figure 17).

#### 3.6.2.3 Leaving Active Burst Mode

The FB voltage will increase immediately if there is a high load jump. This is observed by the comparator C4. As the current limit is ca. 31% during Active Burst Mode, a certain load jump is needed so that the FB signal can exceed 4.5V. At that time the comparator C4 resets the Active Burst Mode control which in turn blocks the comparator C12 by the gate G10. The maximum current can then be resumed to stabilize  $V_{OUT}$ .



## Functional Description

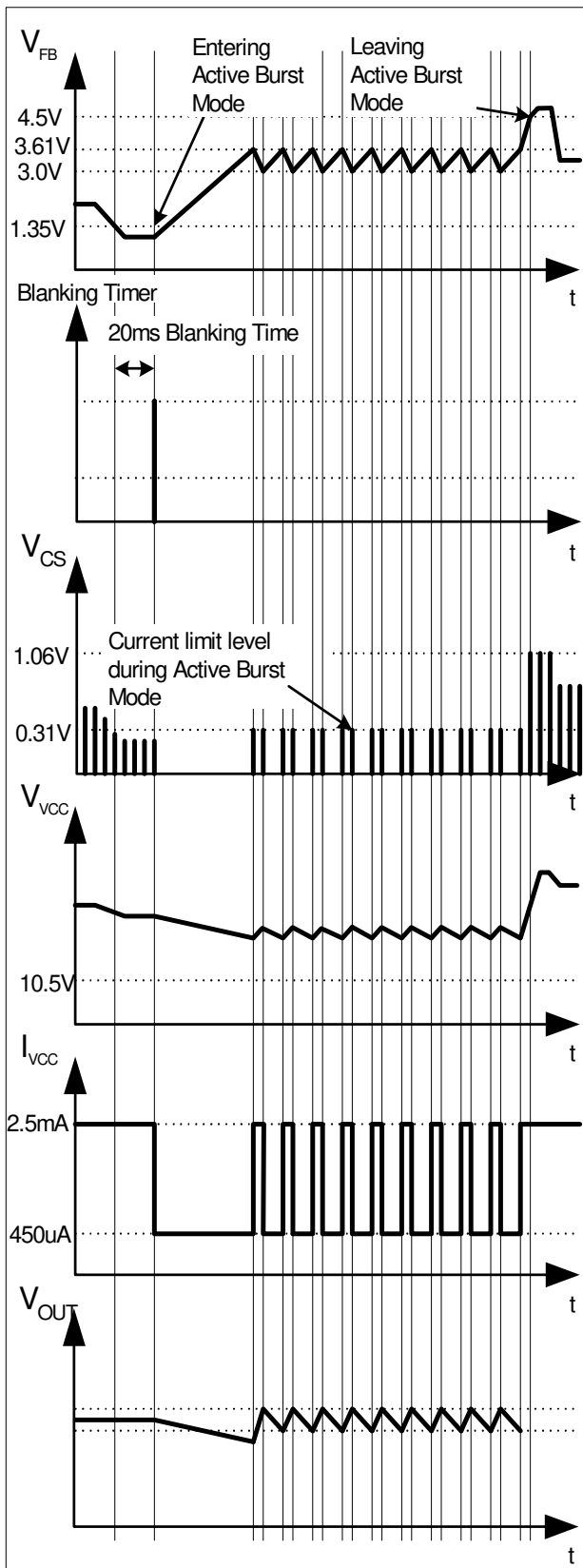


Figure 17 Signals in Active Burst Mode

### 3.6.3 Protection Modes

The IC provides several protection features which are separated into two categories. Some enter Latched Off Mode and the others enter Auto Restart Mode. Besides the pre-defined protection feature for the Latch off mode, there is also an external Latch off Enable pin for customer defined Latch off protection features. The Latched Off Mode can only be reset if VCC falls below 6.23V. Both modes prevent the SMPS from destructive states. The following table shows the relationship between possible system failures and the chosen protection modes.

VCC Overvoltage	Latched Off Mode
Overtemperature	Latched Off Mode
Short Winding/Short Diode	Latched Off Mode
BL pin < 0.1V	Latched Off Mode
Overload	Auto Restart Mode
Open Loop	Auto Restart Mode
VCC Undervoltage	Auto Restart Mode
Short Optocoupler	Auto Restart Mode

#### 3.6.3.1 Latched Off Mode

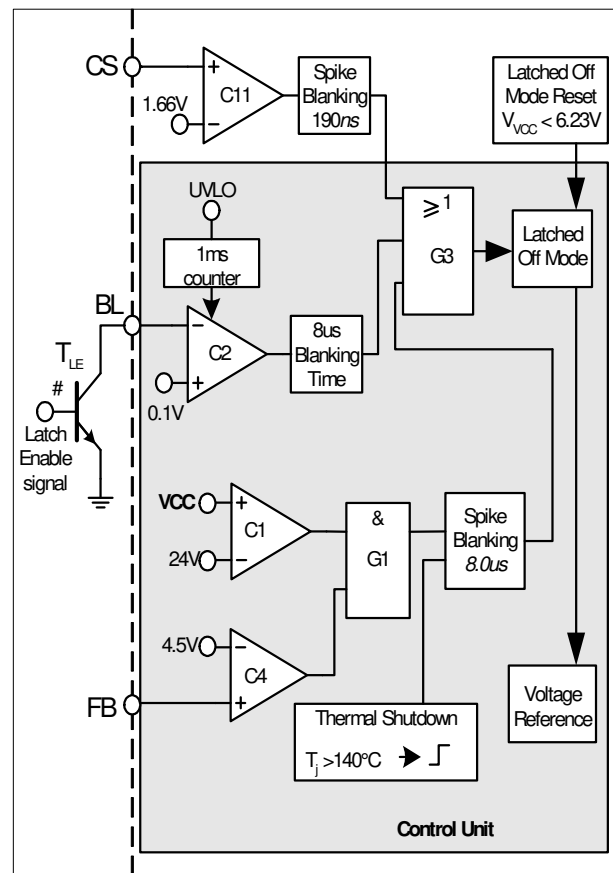


Figure 18 Latched Off Mode

## Functional Description

The VCC voltage is observed by comparator C1 while the FB voltage is monitored by the comparator C4. If the VCC voltage is > 24V and the FB is > 4.5V, the overvoltage detection is activated. That means the overvoltage detection is only activated if the FB signal is outside the operating range > 4.5V, e.g. when Open Loop happens. The logic can eliminate the possible of entering Latch off mode if there is a small voltage overshoots of  $V_{VCC}$  during normal operating.

The internal Voltage Reference is switched off most of the time once Latched Off Mode is entered in order to minimize the current consumption of the IC. This Latched Off Mode can only be reset if the  $V_{VCC} < 6.23V$ . In this mode, only the UVLO is working which controls the Startup Cell by switching on/off at  $V_{VCCon}/V_{VCCoff}$ . During this phase, the average current consumption is only 250 $\mu$ A. As there is no longer a self-supply by the auxiliary winding, the VCC drops. The Undervoltage Lockout switches on the integrated Startup Cell when VCC falls below 10.5V. The Startup Cell is switched off again when VCC has exceeded 18V. Once the Latched Off Mode was entered, there is no Start Up Phase whenever the VCC exceeds the switch-on level of the Undervoltage Lockout. Therefore the VCC voltage changes between the switch-on and switch-off levels of the Undervoltage Lockout with a saw tooth shape (see Figure 19).

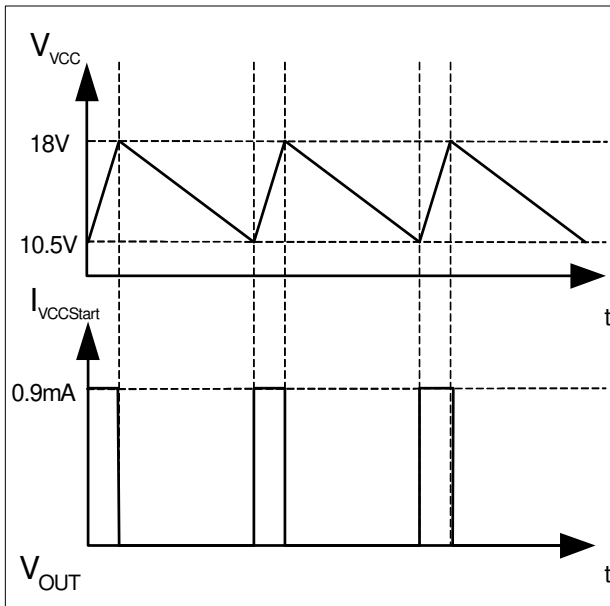


Figure 19 Signals in Latched Off Mode

The Thermal Shutdown block monitors the junction temperature of the IC. After detecting a junction temperature higher than latched thermal shutdown temperature;  $T_{jSD}$ , the Latched Off Mode is entered.

The signals coming from the temperature detection and VCC overvoltage detection are fed into a spike blanking with a time constant of 8.0 $\mu$ s in order to ensure the system reliability.

Furthermore, a short winding or short diode on the secondary side can be detected by the comparator C11 which is in parallel to the propagation delay compensated current limit comparator C10. In normal operating mode, comparator C10 controls the maximum level of the CS signal at 1.06V. If there is a failure such as short winding or short diode, C10 is no longer able to limit the CS signal at 1.06V. Instead the comparator C11 detects the peak current voltage > 1.66V and enters the Latched Off Mode immediately in order to keep the SMPS in a safe stage.

In case the pre-defined Latch Off features are not sufficient, there is a customer defined external Latch Enable feature. The Latch Off Mode can be triggered by pulling down the BL pin to < 0.1V. It can simply add a trigger signal to the base of the externally added transistor,  $T_{LE}$  at the BL pin. To ensure this latch function will not be mis-triggered during start up, a 1ms delay time is implemented to blank the unstable signal.

### 3.6.3.2 Auto Restart Mode

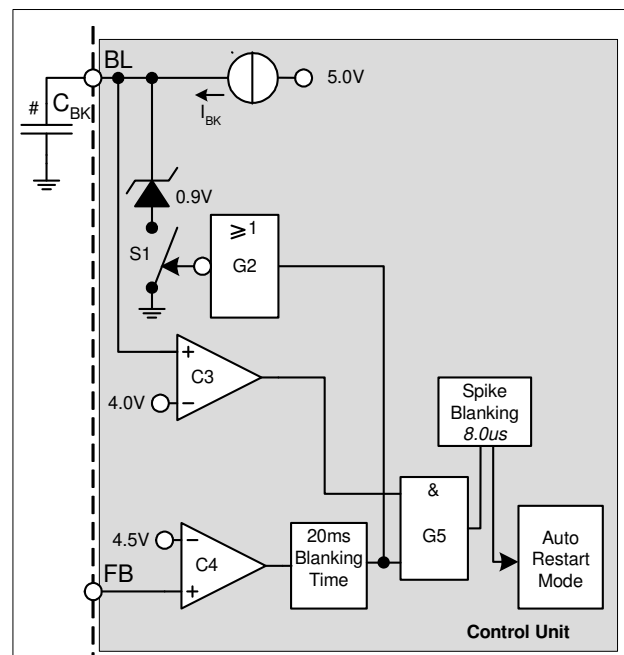


Figure 20 Auto Restart Mode

In case of Overload or Open Loop, the FB exceeds 4.5V which will be observed by comparator C4. Then the internal blanking counter starts to count. When it reaches 20ms, the switch S1 is released. Then the clamped voltage 0.9V at  $V_{BL}$  can increase. When there is no external capacitor  $C_{BK}$  connected, the  $V_{BL}$  will reach 4.0V immediately. When both the input signals at AND gate G5 is positive, the Auto-Restart Mode will be activated after the extra spike blanking time of 8.0 $\mu$ s is elapsed. However, when an extra blanking time is needed, it can be achieved by adding an external capacitor,  $C_{BK}$ . A constant current source of  $I_{BK}$  will start

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**Functional Description**

to charge the capacitor  $C_{BK}$  from 0.9V to 4.0V after the switch S1 is released. The charging time from 0.9V to 4.0V are the extendable blanking time. If  $C_{BK}$  is 0.22 $\mu$ F and  $I_{BK}$  is 8.4 $\mu$ A, the extendable blanking time is around 80ms and the total blanking time is 100ms. In combining the FB and blanking time, there is a blanking window generated which prevents the system to enter Auto Restart Mode due to large load jumps.

In case of VCC undervoltage, the IC enters into the Auto Restart Mode and starts a new startup cycle.

Short Optocoupler also leads to VCC undervoltage as there is no self supply after activating the internal reference and bias.

In contrast to the Latched Off Mode, there is always a Startup Phase with switching cycles in Auto Restart Mode. After this Start Up Phase, the conditions are again checked whether the failure mode is still present. Normal operation is resumed once the failure mode is removed that had caused the Auto Restart Mode.

## 4 Electrical Characteristics

Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.

### 4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Drain Source Voltage	$V_{DS}$	-	650	V	$T_j=110^\circ\text{C}$
Pulse drain current, $t_p$ limited by max. $T_j=150^\circ\text{C}$	$I_{D\_Puls}$	-	3.4	A	
Avalanche energy, repetitive $t_{AR}$ limited by max. $T_j=150^\circ\text{C}^{1)}$	$E_{AR}$	-	0.07	mJ	
Avalanche current, repetitive $t_{AR}$ limited by max. $T_j=150^\circ\text{C}$	$I_{AR}$	-	1.0	A	
VCC Supply Voltage	$V_{VCC}$	-0.3	27	V	
FB Voltage	$V_{FB}$	-0.3	5.0	V	
CS Voltage	$V_{CS}$	-0.3	5.0	V	
Junction Temperature	$T_j$	-40	150	$^\circ\text{C}$	Controller & CoolMOS™
Storage Temperature	$T_S$	-55	150	$^\circ\text{C}$	
Thermal Resistance Junction -Ambient	$R_{thJA1}$	-	90	K/W	PG-DIP-8
ESD Capability (incl. Drain Pin)	$V_{ESD}$	-	2	kV	Human body model <sup>2)</sup>

1) Repetitive avalanche causes additional power losses that can be calculated as  $P_{AV}=E_{AR} \cdot f$

2) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

### 4.2 Operating Range

Note: Within the operating range the IC operates as described in the functional description.

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
VCC Supply Voltage	$V_{VCC}$	$V_{VCCoff}$	26	V	
Junction Temperature of Controller	$T_{jCon}$	-25	130	$^\circ\text{C}$	Max value limited due to thermal shut down of controller
Junction Temperature of CoolMOS™	$T_{jCoolMOS}$	-25	150	$^\circ\text{C}$	

**Electrical Characteristics**
**4.3 Characteristics**
**4.3.1 Supply Section**

*Note: The electrical characteristics involve the spread of values within the specified supply voltage and junction temperature range  $T_j$  from  $-25\text{ °C}$  to  $130\text{ °C}$ . Typical values represent the median values, which are related to  $25\text{ °C}$ . If not otherwise stated, a supply voltage of  $V_{CC} = 18\text{ V}$  is assumed.*

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Start Up Current	$I_{VCCstart}$	-	150	250	$\mu\text{A}$	$V_{VCC} = 17\text{V}$
VCC Charge Current	$I_{VCCcharge1}$	-	-	5.0	mA	$V_{VCC} = 0\text{V}$
	$I_{VCCcharge2}$	0.55	0.90	1.60	mA	$V_{VCC} = 1\text{V}$
	$I_{VCCcharge3}$	-	0.7	-	mA	$V_{VCC} = 17\text{V}$
Leakage Current of Start Up Cell and CoolMOS™	$I_{StartLeak}$	-	0.2	50	$\mu\text{A}$	$V_{Drain} = 450\text{V}$ at $T_j = 100\text{ °C}$
Supply Current with Inactive Gate	$I_{VCCsup1}$	-	1.5	2.5	mA	
Supply Current with Active Gate	$I_{VCCsup2}$	-	2.5	4.2	mA	$I_{FB} = 0\text{A}$
Supply Current in Latched Off Mode	$I_{VCClatch}$	-	250	-	$\mu\text{A}$	$I_{FB} = 0\text{A}$
Supply Current in Auto Restart Mode with Inactive Gate	$I_{VCCrestart}$	-	250	-	$\mu\text{A}$	$I_{FB} = 0\text{A}$
Supply Current in Active Burst Mode with Inactive Gate	$I_{VCCburst1}$	-	450	950	$\mu\text{A}$	$V_{FB} = 2.5\text{V}$
	$I_{VCCburst2}$	-	450	950	$\mu\text{A}$	$V_{VCC} = 11.5\text{V}, V_{FB} = 2.5\text{V}$
VCC Turn-On Threshold	$V_{VCCon}$	17.0	18.0	19.0	V	
VCC Turn-Off Threshold	$V_{VCCoff}$	9.8	10.5	11.2	V	
VCC Turn-On/Off Hysteresis	$V_{VCChys}$	-	7.5	-	V	

**4.3.2 Internal Voltage Reference**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Trimmed Reference Voltage	$V_{REF}$	4.90	5.00	5.10	V	measured at pin FB $I_{FB} = 0$



**Electrical Characteristics**
**4.3.3 PWM Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Fixed Oscillator Frequency	$f_{OSC1}$	87	100	113	kHz	$T_j = 25^\circ\text{C}$
	$f_{OSC2}$	92	100	108		
Frequency Jittering Range	$f_{jitter}$	-	$\pm 4.0$	-	kHz	$T_j = 25^\circ\text{C}$
Max. Duty Cycle	$D_{max}$	0.70	0.75	0.80		
Min. Duty Cycle	$D_{min}$	0	-	-		$V_{FB} < 0.3\text{V}$
PWM-OP Gain	$A_v$	3.0	3.2	3.4		
Voltage Ramp Offset	$V_{Offset-Ramp}$	-	0.6	-	V	
$V_{FB}$ Operating Range Min Level	$V_{FBmin}$	-	0.5	-	V	
$V_{FB}$ Operating Range Max level	$V_{FBmax}$	-	-	4.3	V	CS=1V, limited by Comparator C4 <sup>1)</sup>
FB Pull-Up Resistor	$R_{FB}$	9	15.4	22	k $\Omega$	

<sup>1)</sup> The parameter is not subjected to production test - verified by design/characterization

**4.3.4 Soft Start time**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Soft Start time	$t_{SS}$	-	20.0	-	ms	

**4.3.5 Control Unit**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Clamped $V_{BL}$ voltage during Normal Operating Mode	$V_{BLclmp}$	0.85	0.90	0.95	V	$V_{FB} = 4\text{V}$
Blanking time voltage limit for Comparator C3	$V_{BKC3}$	3.85	4.00	4.15	V	
Over Load & Open Loop Detection Limit for Comparator C4	$V_{FBC4}$	4.28	4.50	4.72	V	
Active Burst Mode Level for Comparator C5	$V_{FBC5}$	1.23	1.35	1.43	V	
Active Burst Mode Level for Comparator C6a	$V_{FBC6a}$	3.48	3.61	3.76	V	After Active Burst Mode is entered

**Electrical Characteristics**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Active Burst Mode Level for Comparator C6b	$V_{FBC6b}$	2.88	3.00	3.12	V	After Active Burst Mode is entered
Overvoltage Detection Limit	$V_{VCCOVp}$	23	24	25	V	$V_{FB} = 5V$
Latch Enable level at BL pin	$V_{LE}$	0.07	0.1	0.2	V	$> 30\mu s$
Charging current at BL pin	$I_{BK}$	5.8	8.4	10.9	$\mu A$	Charge starts after the built-in 20ms blanking time elapsed
Latched Thermal Shutdown <sup>1)</sup>	$T_{jSD}$	130	140	150	$^{\circ}C$	
Built-in Blanking Time for Overload Protection or enter Active Burst Mode	$t_{BK}$	-	20	-	ms	without external capacitor at BL pin
Inhibit Time for Latch Enable function during Start up	$t_{IHLE}$	-	1.0	-	ms	Count when $V_{CC} > 18V$
Spike Blanking Time before Latch off or Auto Restart Protection	$t_{Spike}$	-	8.0	-	$\mu s$	
Power Down Reset for Latched Mode	$V_{VCCPD}$	5.2	6.23	7.8	V	After Latched Off Mode is entered

<sup>1)</sup> The parameter is not subjected to production test - verified by design/characterization. The thermal shut down temperature refers to the junction temperature of the controller.

*Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except  $V_{VCCOVp}$  and  $V_{VCCPD}$*

**4.3.6 Current Limiting**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Peak Current Limitation (incl. Propagation Delay)	$V_{csth}$	0.99	1.06	1.09	V	$dV_{sense} / dt = 0.6V/\mu s$ (see Figure 13)
Peak Current Limitation during Active Burst Mode	$V_{CS2}$	0.27	0.31	0.37	V	
Leading Edge Blanking	$t_{LEB}$	-	220	-	ns	
CS Input Bias Current	$I_{CSbias}$	-1.5	-0.2	-	$\mu A$	$V_{CS} = 0V$
Over Current Detection for Latched Off Mode	$V_{CS1}$	1.570	1.66	1.764	V	
CS Spike Blanking for Comparator C11	$t_{CSspike}$	-	190	-	ns	

**Electrical Characteristics**
**4.3.7 CoolMOS™ Section**

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Drain Source Breakdown Voltage	$V_{(BR)DSS}$	600	-	-	V	$T_j = 25^\circ\text{C}$
		650	-	-	V	$T_j = 110^\circ\text{C}$
Drain Source On-Resistance	$R_{DSon}$	-	2.95	3.42	$\Omega$	$T_j = 25^\circ\text{C}$
		-	6.60	7.56	$\Omega$	$T_j = 125^\circ\text{C}^{1)}$ at $I_D = 1.0\text{A}$
Effective output capacitance, energy related	$C_{o(er)}$	-	7.0	-	pF	$V_{DS} = 0\text{V to } 480\text{V}$
Rise Time	$t_{rise}$	-	30 <sup>2)</sup>	-	ns	
Fall Time	$t_{fall}$	-	30 <sup>2)</sup>	-	ns	

1) The parameter is not subjected to production test - verified by design/characterization

2) Measured in a Typical Flyback Converter Application

## 5 Temperature derating curve

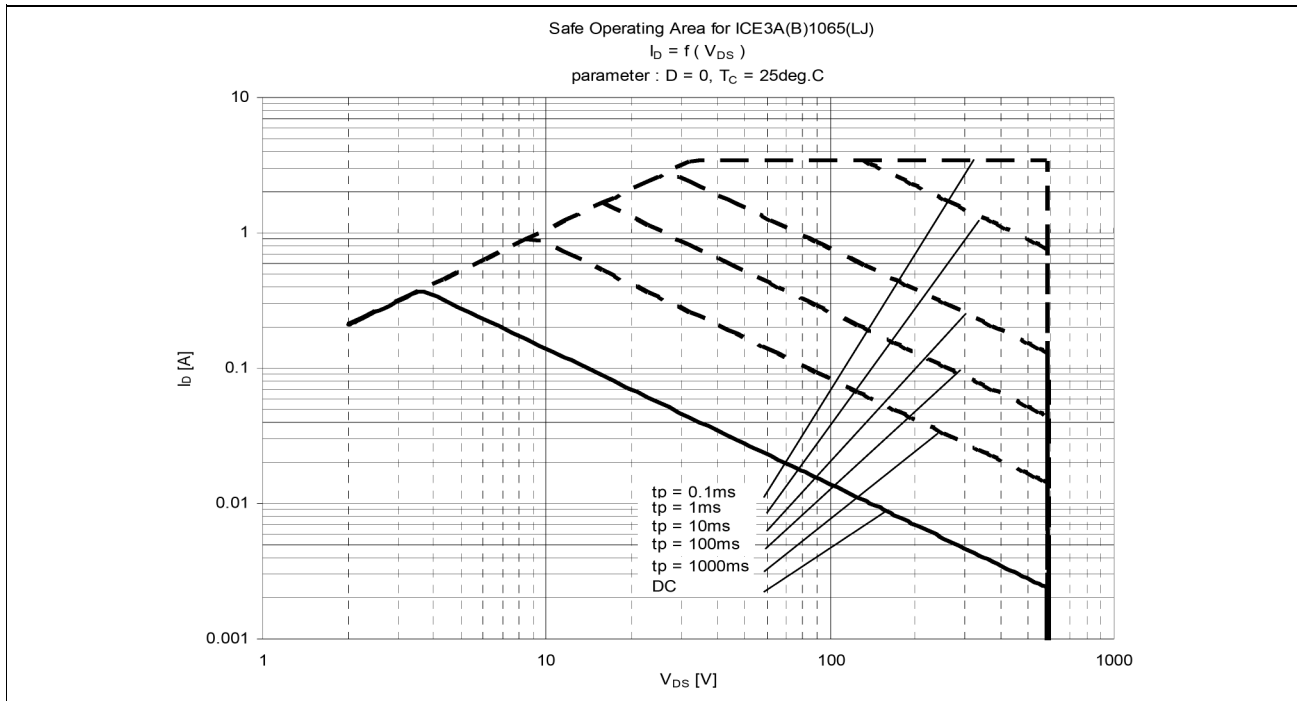


Figure 21 Safe Operating area ( SOA ) curve

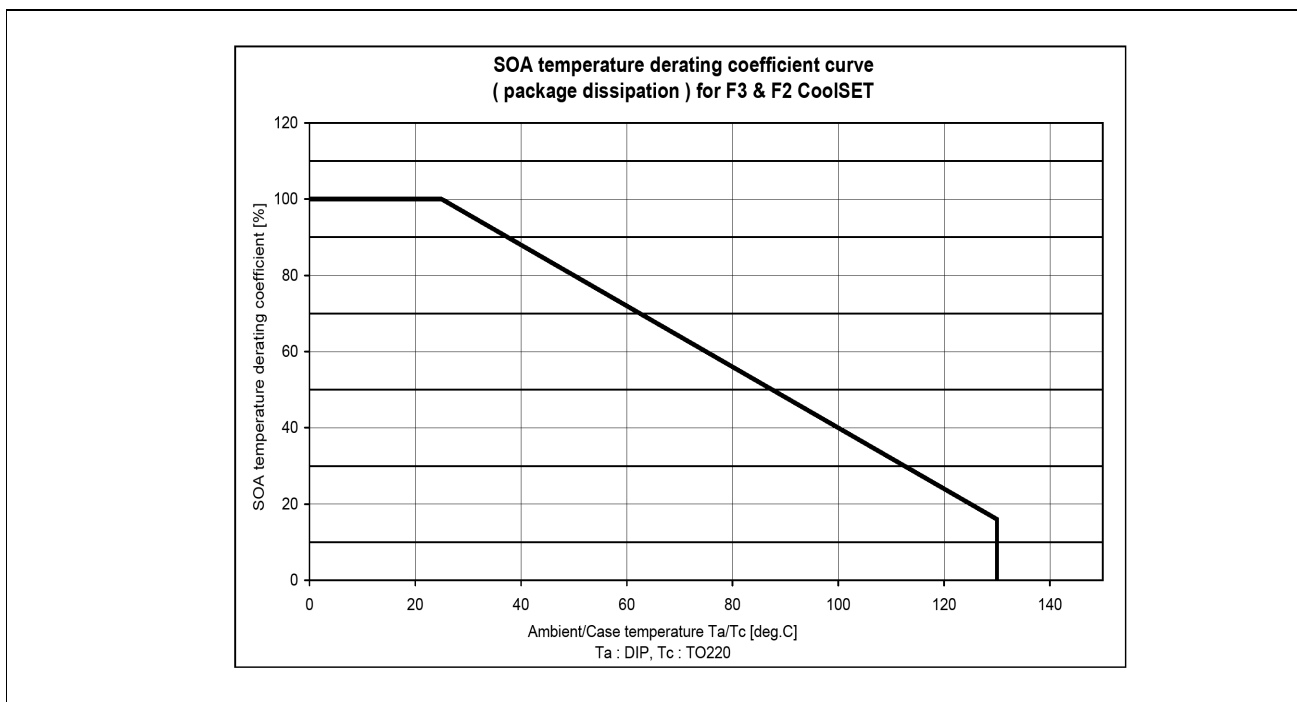
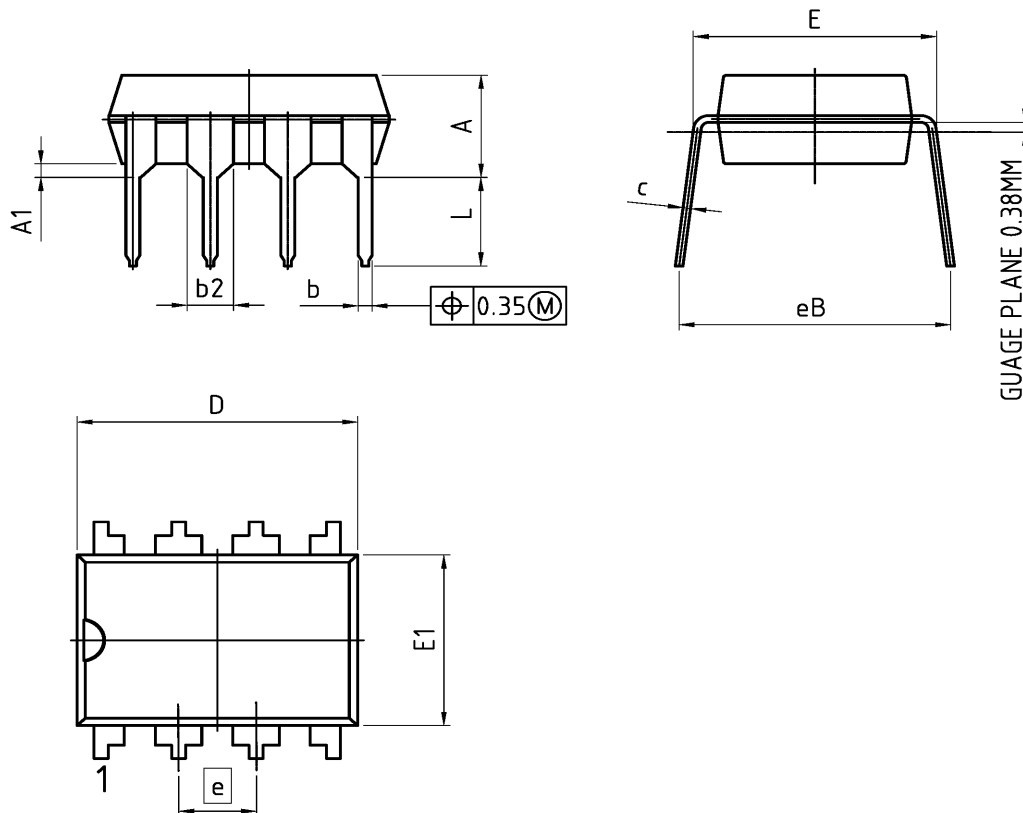


Figure 22 SOA temperature derating coefficient curve

## 6 Outline Dimension

### PG-DIP-8 (Plastic Dual In-Line Package)



1) DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	-	4.8	-	0.189
A1	0.38	-	0.015	-
b	0.36	0.56	0.014	0.022
b2	-	1.700	-	0.067
c	0.15	0.36	0.006	0.014
D	9.100	9.770	0.358	0.385
E	7.490	8.260	0.295	0.325
E1	6.100	6.600	0.150	0.157
e	2.54 BSC		0.1 BSC	
N	8		8	
eB	7.9	9.9	0.311	0.390
L	3	-	0.118	-

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SCALE

EUROPEAN PROJECTION

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Figure 23 PG-DIP-8 (PB-free Plating Plastic Dual In-Line Outline)



## 7 Marking

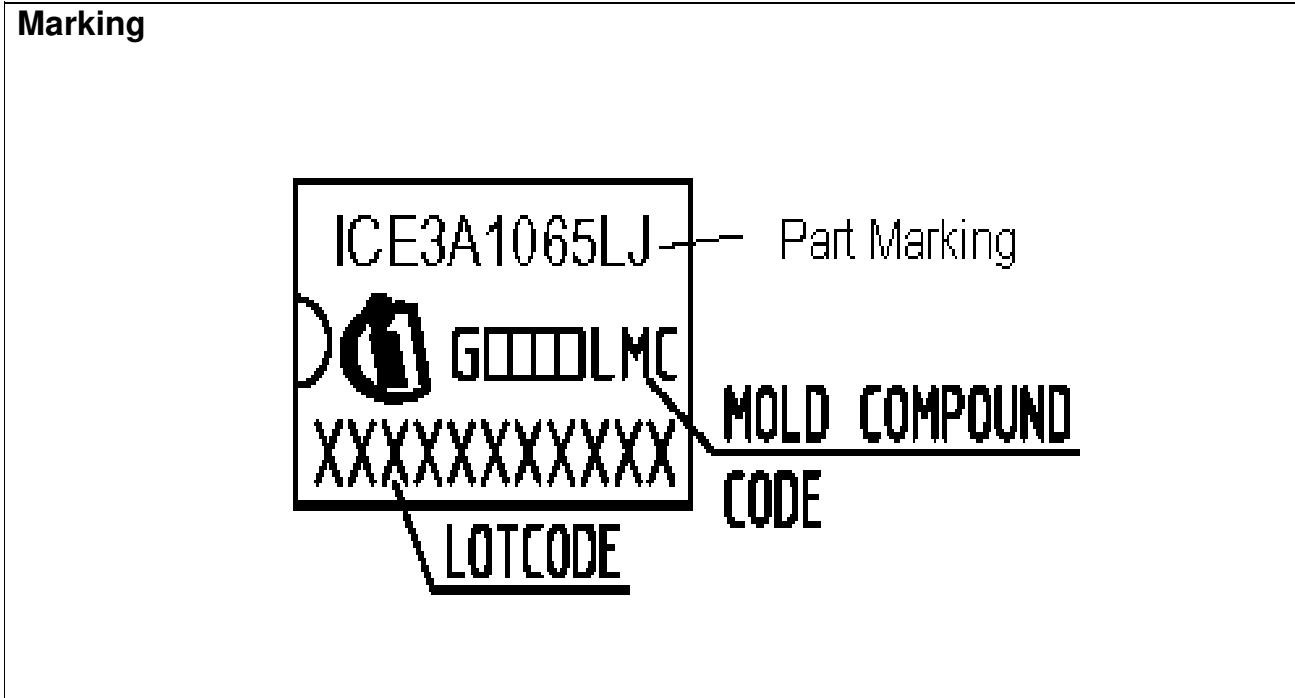
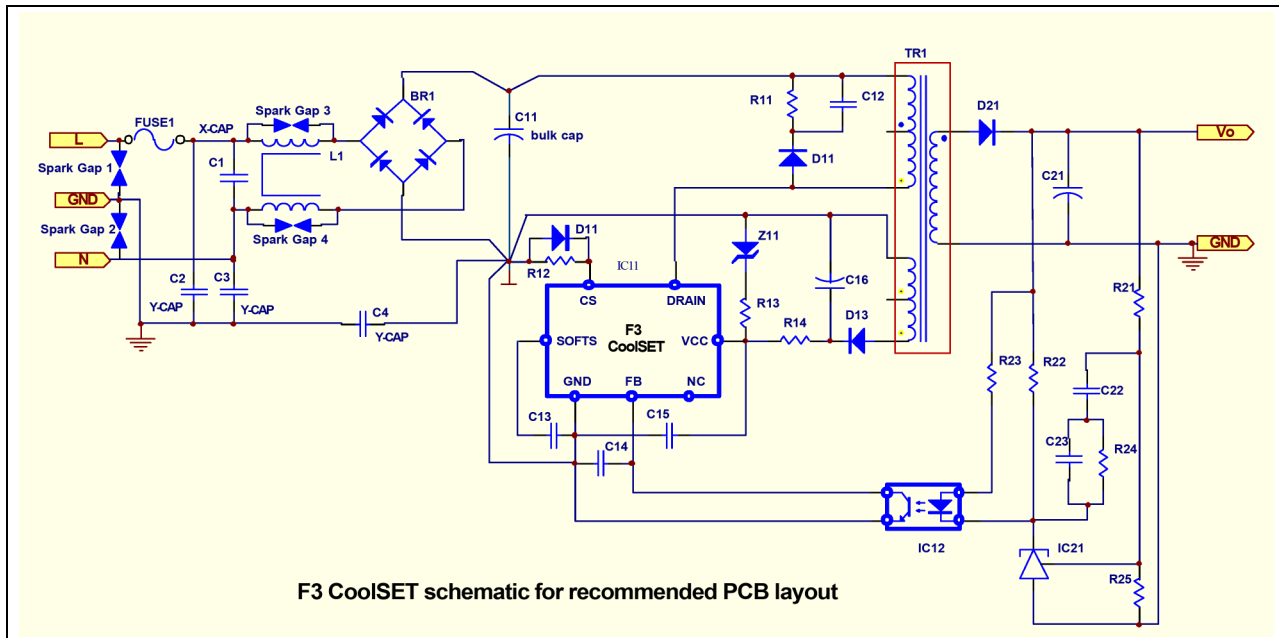


Figure 24 Marking

Schematic for recommended PCB layout

## 8 Schematic for recommended PCB layout



**Figure 25 Schematic for recommended PCB layout**

General guideline for PCB layout design using F3 CoolSET (refer to Figure 25):

1. "Star Ground" at bulk capacitor ground, C11:
 

"Star Ground" means all primary DC grounds should be connected to the ground of bulk capacitor C11 separately in one point. It can reduce the switching noise going into the sensitive pins of the CoolSET device effectively. The primary DC grounds include the followings.

  - a. DC ground of the primary auxiliary winding in power transformer, TR1, and ground of C16 and Z11.
  - b. DC ground of the current sense resistor, R12
  - c. DC ground of the CoolSET device, GND pin of IC11; the signal grounds from C13, C14, C15 and collector of IC12 should be connected to the GND pin of IC11 and then "star" connect to the bulk capacitor ground.
  - d. DC ground from bridge rectifier, BR1
  - e. DC ground from the bridging Y-capacitor, C4
2. High voltage traces clearance:
 

High voltage traces should keep enough spacing to the nearby traces. Otherwise, arcing would incur.

  - a. 400V traces (positive rail of bulk capacitor C11) to nearby trace: > 2.0mm
  - b. 600V traces (drain voltage of CoolSET IC11) to nearby trace: > 2.5mm
3. Filter capacitor close to the controller ground:
 

Filter capacitors, C13, C14 and C15 should be placed as close to the controller ground and the controller pin as possible so as to reduce the switching noise coupled into the controller.

Guideline for PCB layout design when >3KV lightning surge test applied (refer to Figure 25):

1. Add spark gap
 

Spark gap is a pair of saw-tooth like copper plate facing each other which can discharge the accumulated charge during surge test through the sharp point of the saw-tooth plate.

  - a. Spark Gap 3 and Spark Gap 4, input common mode choke, L1:
 

Gap separation is around 1.5mm (no safety concern)

---

**Schematic for recommended PCB layout**

b. Spark Gap 1 and Spark Gap 2, Live / Neutral to GROUND:

These 2 Spark Gaps can be used when the lightning surge requirement is >6KV.

230Vac input voltage application, the gap separation is around 5.5mm

115Vac input voltage application, the gap separation is around 3mm

2. Add Y-capacitor (C2 and C3) in the Live and Neutral to ground even though it is a 2-pin input

3. Add negative pulse clamping diode, D11 to the Current sense resistor, R12:

The negative pulse clamping diode can reduce the negative pulse going into the CS pin of the CoolSET and reduce the abnormal behavior of the CoolSET. The diode can be a fast speed diode such as IN4148.

The principle behind is to drain the high surge voltage from Live/Neutral to Ground without passing through the sensitive components such as the primary controller, IC11.