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Datasheet, Version 2.1, 15 Nov 2005

# PWM-FF IC

## ICE3DS01L

## ICE3DS01LG

Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell

Power Management & Supply

Never stop thinking.

**ICE3DS01L(G)**

| **Revision History:** | **2005-11-15** | Datasheet |
|---|---|---|
| Previous Version: | 2.0 | |

| Page | Subjects (major changes since last revision) |
|---|---|
| | update to PB-free package |
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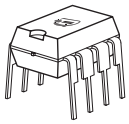
# F3

ICE3DS01L
ICE3DS01LG

# Off-Line SMPS Current Mode Controller with integrated 500V Startup Cell



PG-DIP-8-6

PG-DSO-8-8

## Product Highlights

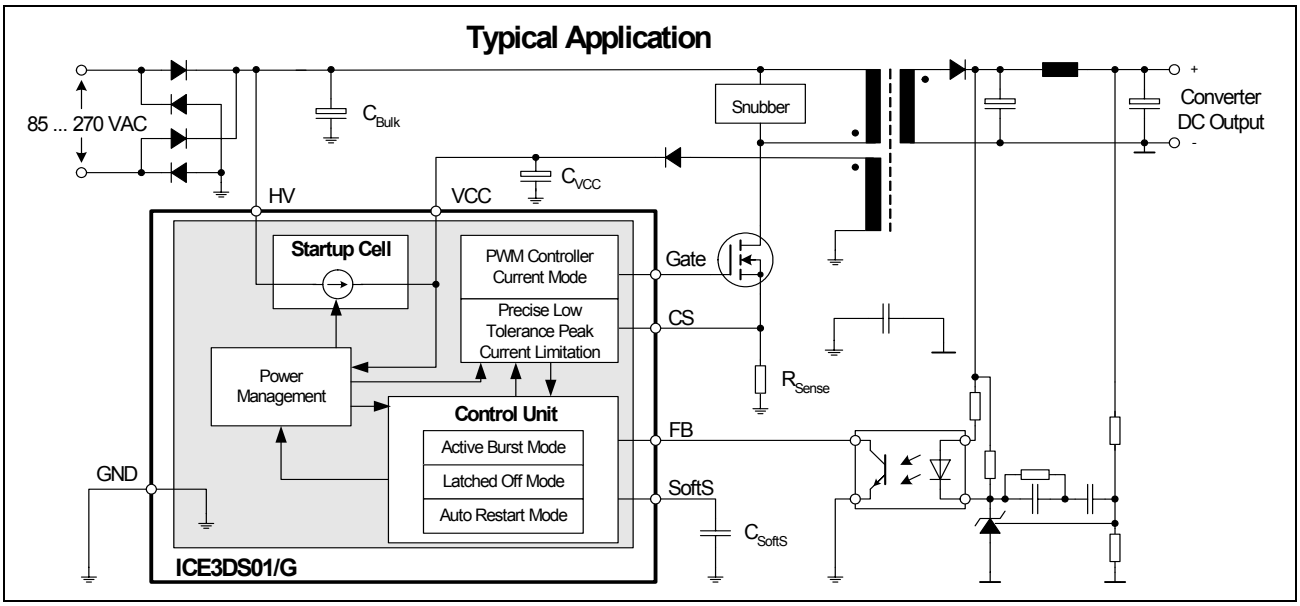
- **Active Burst Mode to reach the lowest Standby Power Requirements < 100mW**
- **Latched Off Mode to increase Robustness and Safety of the System**
- **Adjustable Blanking Window for High Load Jumps to increase Reliability**
- **PB-free Plating and RoHS compilance**

## Features

- Active Burst Mode for lowest Standby Power @ light load controlled by Feedback Signal
- Fast Load Jump Response in Active Burst Mode
- 500V Startup Cell switched off after Start Up
- 110kHz internally fixed Switching Frequency
- Latched Off Mode for Overtemperature Detection
- Latched Off Mode for Overvoltage Detection
- Latched Off Mode for Short Winding Detection
- Auto Restart Mode for Overload and Open Loop
- Auto Restart Mode for VCC Undervoltage
- User defined Soft Start
- Minimum of external Components required
- Max Duty Cycle 72%
- Overall Tolerance of Current Limiting < ±5%
- Internal Leading Edge Blanking
- Soft driving for Low EMI

## Description

The F3 Controller provides Active Burst Mode to reach the lowest Standby Power Requirements <100mW at no load. As during Active Burst Mode the controller is always active there is an immediate response on load jumps possible without any black out in the SMPS. In Active Burst Mode the ripple of the output voltage can be reduced <1%. Furthermore Latched Off Mode is entered in case of Overtemperature, Overvoltage or Short Winding. If Latched Off Mode is entered only the disconnection from the main line can reset the Controller. Auto Restart Mode is entered in case of failure modes like open loop or overload. By means of the internal precise peak current limitation the dimension of the transformer and the secondary diode can be lower which leads to more cost efficiency. An adjustable blanking window prevents the IC from entering Auto Restart Mode or Active Burst Mode in case of high Load Jumps.




| Type | $F_{OSC}$ | Package |
|---|---|---|
| ICE3DS01L | 110kHz | PG-DIP-8-6 |
| ICE3DS01LG | 110kHz | PG-DSO-8-8 |

**Table of Contents** **Page**

# 1 Pin Configuration and Functionality

## 1.1 Pin Configuration with PG-DIP-8-6

| Pin | Symbol | Function |
|---|---|---|
| 1 | SoftS | Soft-Start |
| 2 | FB | Feedback |
| 3 | CS | Current Sense |
| 4 | HV | High Voltage Input |
| 5 | HV | High Voltage Input |
| 6 | Gate | Driver Stage Output |
| 7 | VCC | Controller Supply Voltage |
| 8 | GND | Controller Ground |

## 1.2 Pin Configuration with PG-DSO-8-8

| Pin | Symbol | Function |
|---|---|---|
| 1 | SoftS | Soft-Start |
| 2 | FB | Feedback |
| 3 | CS | Current Sense |
| 4 | Gate | Driver Stage Output |
| 5 | HV | High Voltage Input |
| 6 | N.C. | Not connected |
| 7 | VCC | Controller Supply Voltage |
| 8 | GND | Controller Ground |

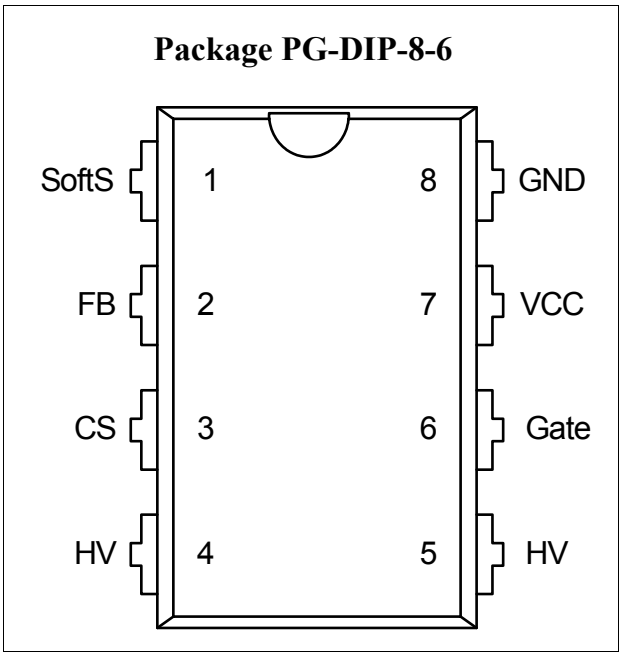



*Figure 1 Pin Configuration PG-DIP-8-6(top view)*

Note: Pin 4 and 5 are shorted within the DIP package.

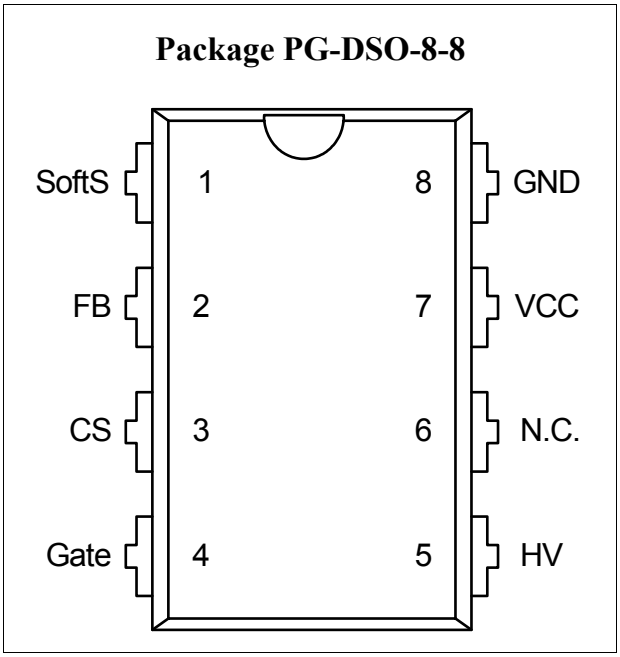



*Figure 2 Pin Configuration PG-DSO-8-8(top view)*

## 1.3 Pin Functionality

**SoftS (Soft Start & Auto Restart Control)**

The SoftS pin combines the function of Soft Start in case of Start Up and Auto Restart Mode and the controlling of the Auto Restart Mode in case of error detection. Furthermore the blanking window for high load jumps is adjusted by means of the external capacitor connected to SoftS.

**FB (Feedback)**

The information about the regulation is provided by the FB Pin to the internal Protection Unit and to the internal PWM-Comparator to control the duty cycle. The FB-Signal controls in case of light load the Active Burst Mode of the controller.

**CS (Current Sense)**

The Current Sense pin senses the voltage developed on the series resistor inserted in the source of the external PowerMOS. If CS reaches the internal threshold of the Current Limit Comparator, the Driver output is immediately switched off. Furthermore the current information is provided for the PWM-Comparator to realize the Current Mode.

**Gate**

The Gate pin is the output of the internal driver stage connected to the Gate of an external PowerMOS.

**HV (High Voltage)**

The HV pin is connected to the rectified DC input voltage. It is the input for the integrated 500V Startup Cell.

**VCC (Power supply)**

The VCC pin is the positive supply of the IC. The operating range is between 8.5V and 21V.

**GND (Ground)**

The GND pin is the ground of the controller.

# 2 Representative Blockdiagram

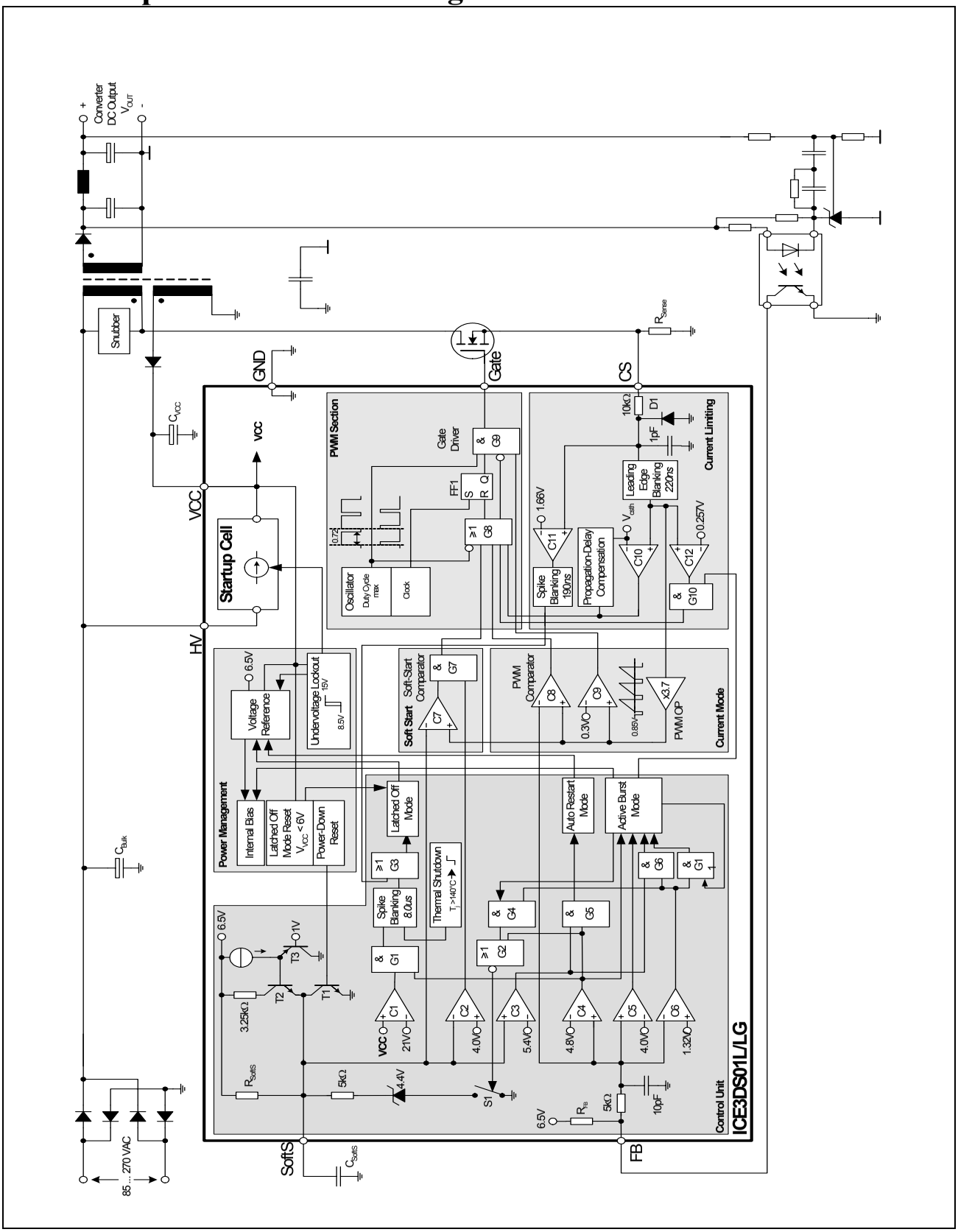



*Figure 3 Representative Blockdiagram*

# 3 Functional Description

All values which are used in the functional description are typical values. For calculating the worst cases the min/max values which can be found in section 4 Electrical Characteristics have to be considered.

## 3.1 Introduction

The F3 is the further development of the F2 to meet the requirements for the lowest Standby Power at minimum load and no load conditions. A new fully integrated Standby Power concept is implemented into the IC in order to keep the application design easy. Compared to F2 no further external parts are needed to achieve the lowest Standby Power. An intelligent Active Burst Mode is used for this Standby Mode. After entering this mode there is still a full control of the power conversion by the secondary side via the same optocoupler that is used for the normal PWM control. The response on load jumps is optimized. The voltage ripple on $V_{out}$ is minimized. $V_{out}$ is further on well controlled in this mode.

The usually external connected RC-filter in the feedback line after the optocoupler is integrated in the IC to reduce the external part count.

Furthermore a high voltage startup cell is integrated into the IC which is switched off once the Undervoltage Lockout on-threshold of 15V is exceeded. The external startup resistor is no longer necessary. Power losses are therefore reduced. This increases the efficiency under light load conditions dramatically.

The Soft-Start capacitor is also used for providing an adjustable blanking window for high load jumps. During this time window the overload detection is disabled. With this concept no further external components are necessary to adjust the blanking window.

A new Latched Off Mode is implemented into the IC in order to increase the robustness and safety of the system. Latched Off Mode is only entered if very dangerous conditions occur that damage the SMPS if not switched off immediately. A restart of the system can then only be done by disconnecting the AC line.

Auto Restart Mode reduces the average power conversion to a minimum. In this mode malfunctions are covered that could lead to a destruction of the SMPS if no dramatically reduced power limitation is provided over time. Once the malfunction is removed normal operation is immediately started after the next Start Up Phase.

The internal precise peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation. Therefore the maximum power is nearly independent on the input voltage that is required for wide range SMPS. There is no need for an extra over sizing of the SMPS, e.g. the transformer or PowerMOS.

## 3.2 Power Management

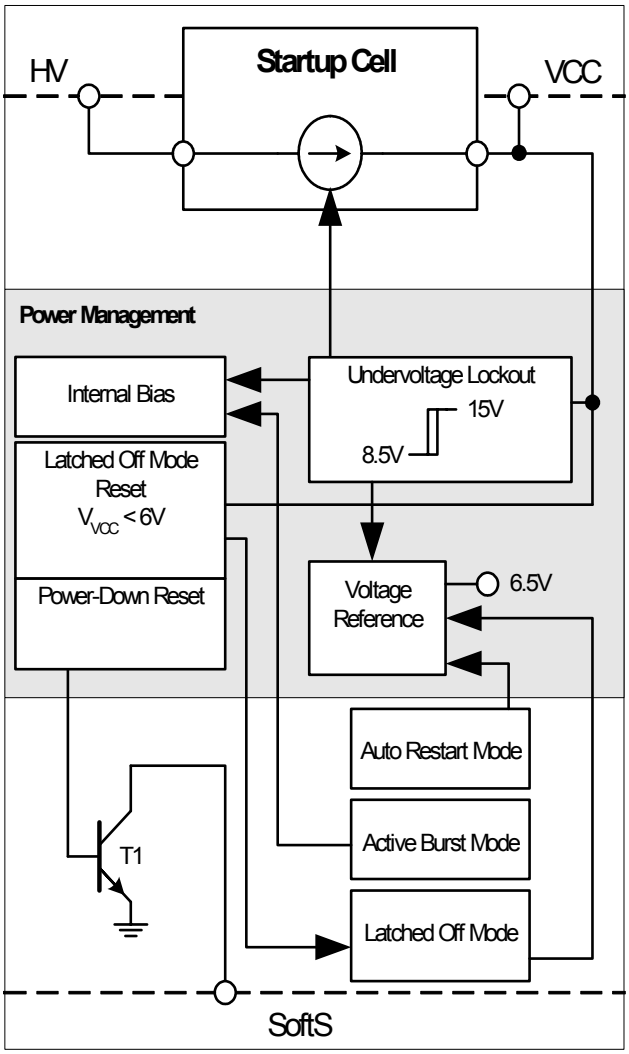



*Figure 4 Power Management*

The Undervoltage Lockout monitors the external supply voltage $V_{VCC}$. When the SMPS is plugged to the main line the internal Startup Cell is biased and starts to charge the external capacitor $C_{VCC}$ which is connected to the VCC pin. The VCC charge current that is provided by the Startup Cell from the HV pin is 1.05mA. When $V_{VCC}$ exceeds the on-threshold $V_{CCon}$=15V the internal voltage reference and bias circuit are switched on. Then the Startup Cell is switched off by the Undervoltage Lockout and therefore also the power losses are switched off caused by the Startup Cell which is connected to the bus voltage (HV). To avoid uncontrolled ringing at switch-on a hysteresis is implemented. The switch-off of the controller can only take place after Active Mode was entered and $V_{VCC}$ falls below 8.5V.

The maximum current consumption before the controller is activated is about 170µA.

When $V_{VCC}$ falls below the off-threshold $V_{CCoff}$=8.5V the internal reference is switched off and the Power Down reset

let T1 discharging the soft-start capacitor $C_{SoftS}$ at pin SoftS. Thus it is ensured that at every startup cycle the voltage ramp at pin SoftS starts at zero.

The internal Voltage Reference is switched off if Latched Off Mode or Auto Restart Mode is entered. The current consumption is then reduced to 300µA.

When Active Burst Mode is entered the internal Bias is switched off in order to reduce the current consumption below 1.1mA while keeping the Voltage Reference still active as this is necessary in this mode.

In case Latched Off Mode is entered VCC needs to be lowered below 6V to reset the Latched Off Mode. This is done usually by disconnecting the SMPS from the AC line.

## 3.3 Startup Phase

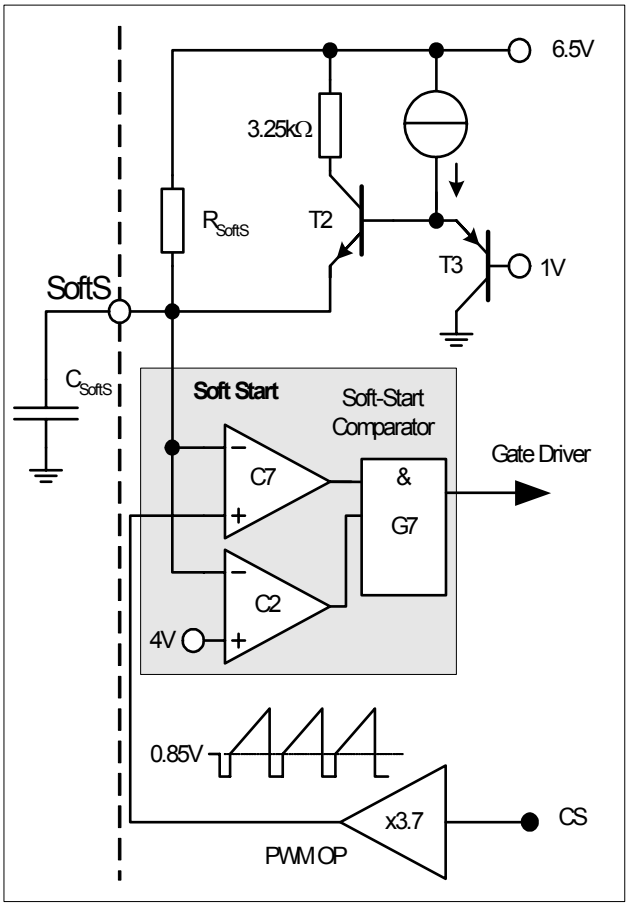



*Figure 5 Soft Start*

During the Startup Phase a Soft Start is provided. A signal $V_{SoftS}$ which is generated by the external capacitor $C_{Softs}$ in combination with the internal pull up resistor $R_{SoftS}$ determines the duty cycle until $V_{SoftS}$ exceeds 4V.

In the beginning $C_{SoftS}$ is immediately charged up to approx. 1V by T2. Therefore the Soft Start Phase takes place between 1V and 4V. Above $V_{SoftsS}$ = 4V there is no longer duty cycle limitation $DC_{max}$ is controlled by comparator C7 as comparator C2 blocks the gate G7 (see Figure 6).The maximum charge current in the very first phase when $V_{SoftS}$ is below 1V is limited to 1.9mA.

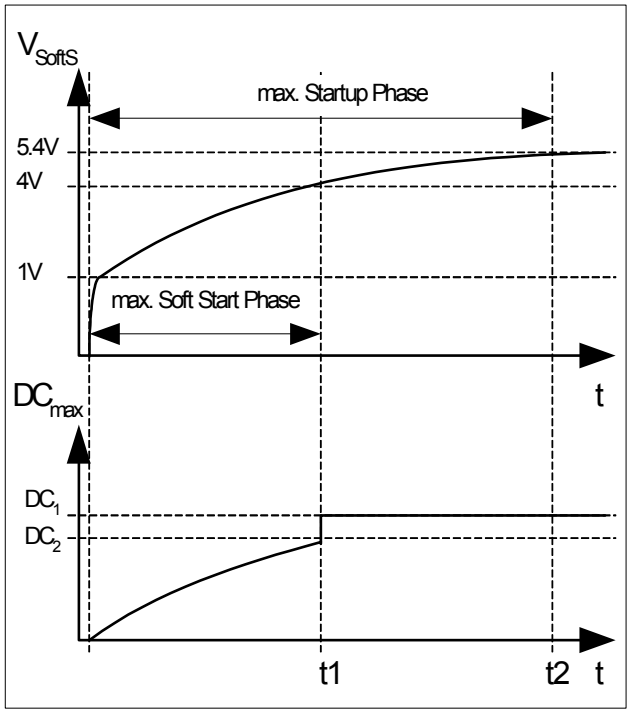



*Figure 6 Startup Phase*

By means of this extra charge stage there is no delay in the beginning of the Startup Phase when there is still no switching. Furthermore Soft Start is finished at 4V to have faster the maximum power capability. The duty cycles $DC_1$ and $DC_2$ are depending on the mains and the primary inductance of the transformer. The limitation of the primary current by $DC_2$ is related to $V_{SoftS}$ = 4V. But $DC_1$ is related to a maximum primary current which is limited by the internal Current Limiting with CS = 1V. Therefore the maximum Startup Phase is divided into a Soft Start Phase until t1 and a phase from t1 until t2 where maximum power is provided if demanded by the FB signal.

## 3.4 PWM Section

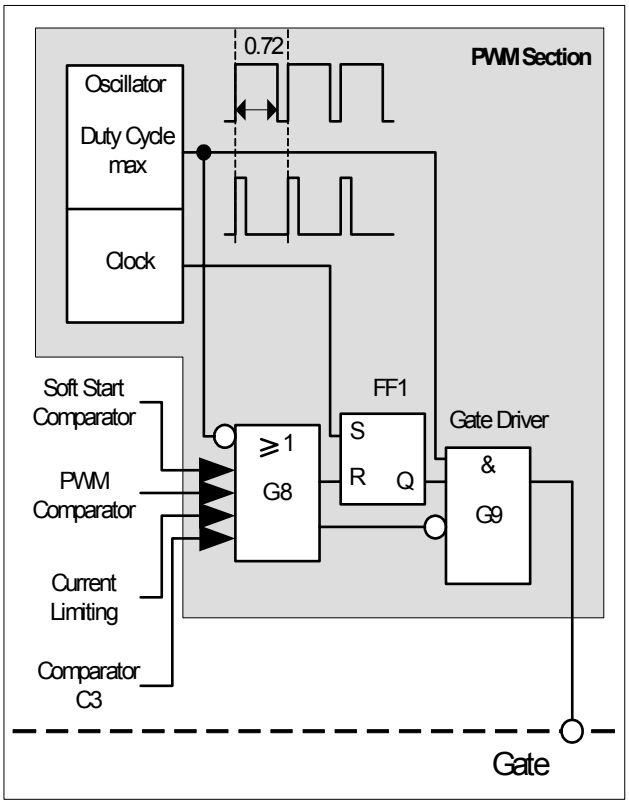



*Figure 7 PWM Section*

### 3.4.1 Oscillator

The oscillator generates a frequency $f_{switch}$ = 110kHz. A resistor, a capacitor and a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed, in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of $D_{max}$=0.72.

### 3.4.2 PWM-Latch FF1

The oscillator clock output provides a set pulse to the PWM-Latch when initiating the external Power Switch conduction. After setting the PWM-Latch can be reset by the PWM comparator, the Soft Start comparator, the Current-Limit comparator or comparator C3. In case of resetting the driver is shut down immediately.

### 3.4.3 Gate Driver

The Gate Driver is a fast totem pole gate drive which is designed to avoid cross conduction currents and which is equipped with a zener diode Z1 (see Figure 8) in order to improve the control of the Gate attached power transistors as well as to protect them against undesirable gate overvoltages.

The Gate Driver is active low at voltages below the undervoltage lockout threshold $V_{VCCoff}$.

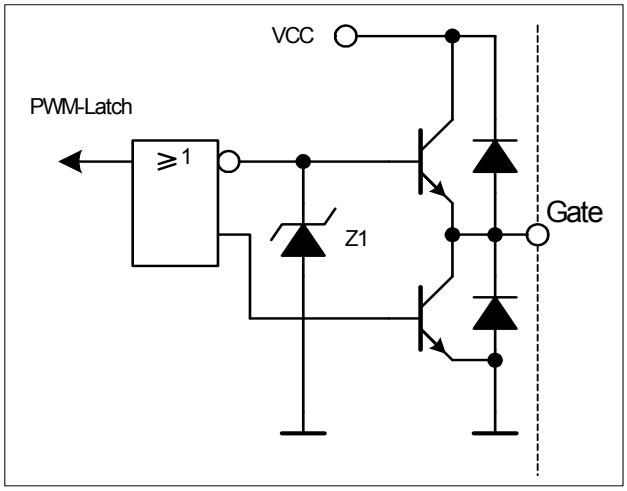



*Figure 8 Gate Driver*

The driver-stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch on slope when exceeding the external Power Switch threshold. This is achieved by a slope control of the rising edge at the driver's output (see Figure 9).

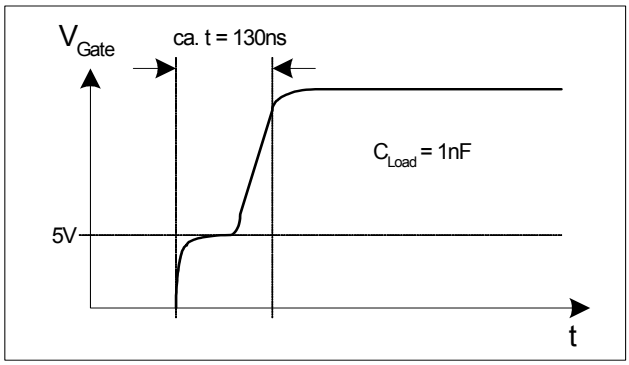



*Figure 9 Gate Rising Slope*

Thus the leading switch on spike is minimized. When the external Power Switch is switched off, the falling shape of the driver is slowed down when reaching 2V to prevent an overshoot below ground. Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

## 3.5 Current Limiting

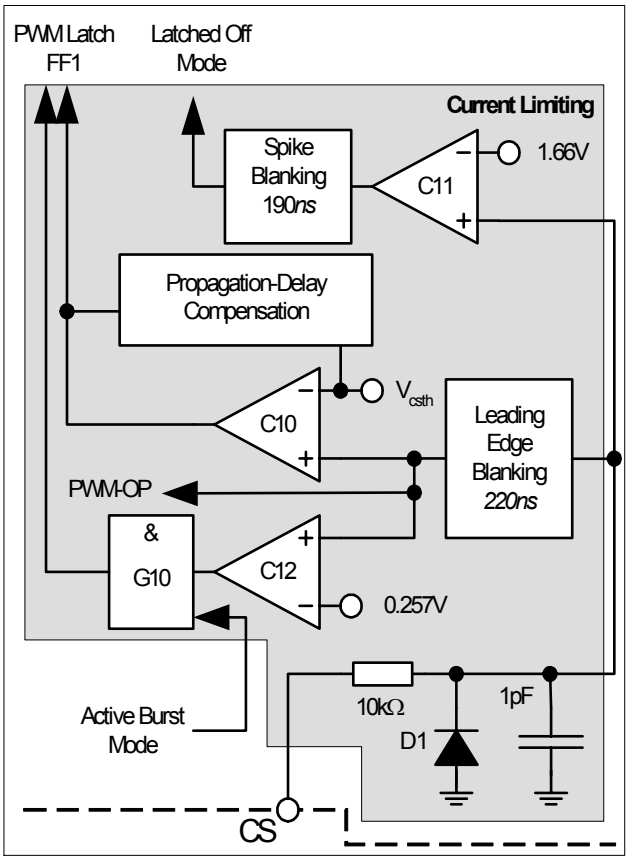



*Figure 10 Current Limiting*

There is a cycle by cycle Current Limiting realized by the Current-Limit comparator C10 to provide an overcurrent detection. The source current of the external Power Switch is sensed via an external sense resistor $R_{Sense}$ . By means of $R_{Sense}$ the source current is transformed to a sense voltage $V_{Sense}$ which is fed into the pin CS. If the voltage $V_{Sense}$ exceeds the internal threshold voltage $V_{csth}$ the comparator C10 immediately turns off the gate drive by resetting the PWM Latch FF1. A Propagation Delay Compensation is added to support the immediate shut down without delay of the Power Switch in case of Current Limiting. The influence of the AC input voltage on the maximum output power can thereby be avoided.

To prevent the Current Limiting from distortions caused by leading edge spikes a Leading Edge Blanking is integrated in the current sense path for the comparators C10, C12 and the PWM-OP.

A further comparator C11 is implemented to detect dangerous current levels which could occur if there is a short winding in the transformer or the secondary diode is shorten. To ensure that there is no accidentally entering of the Latched Mode by the comparator C11 a spike blanking with 190ns is integrated in the output path of comparator C11.

The output of comparator C12 is activated by the Gate G10 if Active Burst Mode is entered. Once activated the current limiting is thereby reduced to 0.257V. This voltage level determines the power level when the Active Burst Mode is left if there is a higher power demand.

### 3.5.1 Leading Edge Blanking

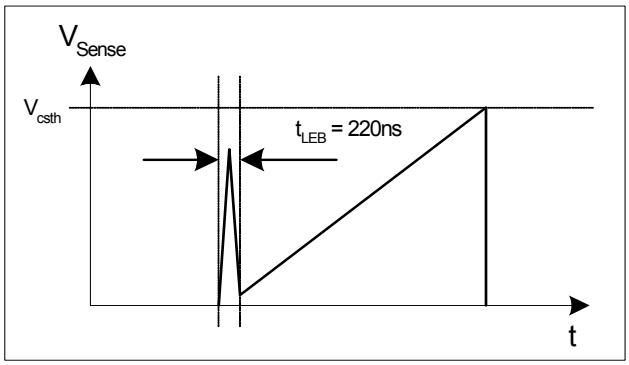



*Figure 11 Leading Edge Blanking*

Each time when the external Power Switch is switched on a leading edge spike is generated due to the primary-side capacitances and secondary-side rectifier reverse recovery time. To avoid a premature termination of the switching pulse this spike is blanked out with a time constant of $t_{LEB}$ = 220ns. During that time there can't be an accidentally switch off of the gate drive.

### 3.5.2 Propagation Delay Compensation

In case of overcurrent detection the shut down of the external Power Switch is delayed due to the propagation delay of the circuit. This delay causes an overshoot of the peak current $I_{peak}$ which depends on the ratio of dI/dt of the peak current (see Figure 12).

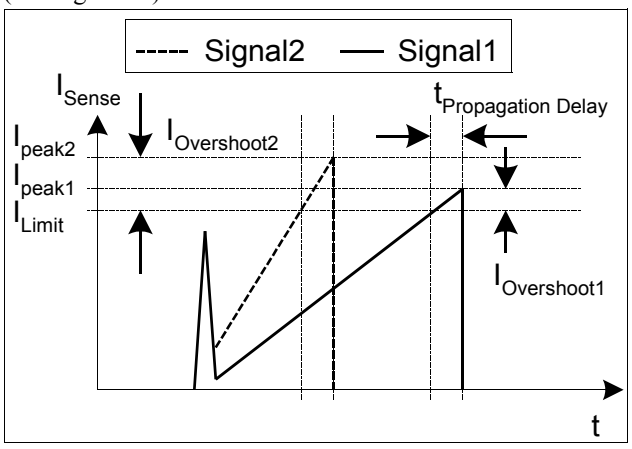



*Figure 12 Current Limiting*

The overshoot of Signal2 is bigger than of Signal1 due to the steeper rising waveform. This change in the slope is depending on the AC input voltage. Propagation Delay Compensation is integrated to limit the overshoot dependency on dI/dt of the rising primary current. That means the propagation delay time between exceeding the current sense threshold $V_{csth}$ and the switch off of the external Power Switch is compensated over temperature

within a wide range. Current Limiting is now possible in a very accurate way (see Figure 13).

E.g. $I_{peak}$ = 0.5A with $R_{Sense}$ = 2. Without Propagation Delay Compensation the current sense threshold is set to a static voltage level $V_{csth}$=1V. A current ramp of dI/dt = 0.4A/µs, that means $dV_{Sense}/dt$ = 0.8V/µs, and a propagation delay time of i.e. $t_{Propagation\ Delay}$ =180ns leads then to an $I_{peak}$ overshoot of 14.4%. By means of propagation delay compensation the overshoot is only about 2% (see Figure 13).

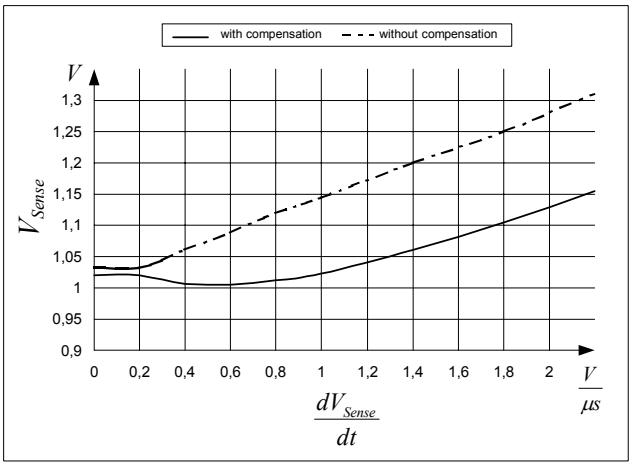



*Figure 13 Overcurrent Shutdown*

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage $V_{csth}$ (see Figure 14). In case of a steeper slope the switch off of the driver is earlier to compensate the delay.

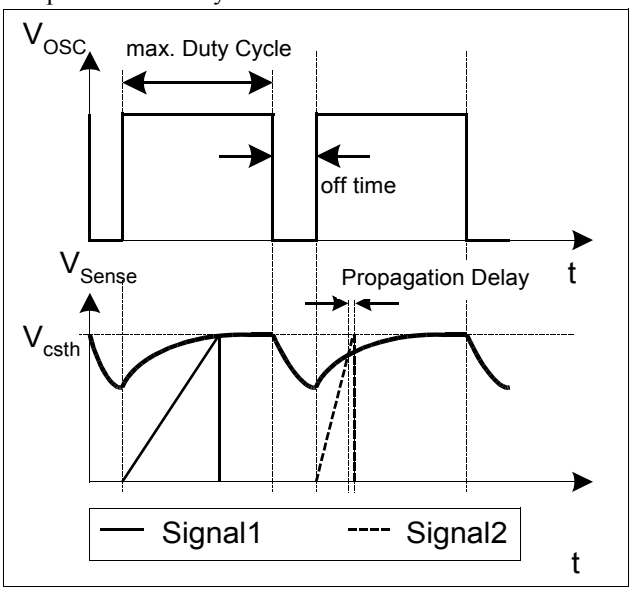



*Figure 14 Dynamic Voltage Threshold $V_{csth}$*

## 3.6 Control Unit

The Control Unit contains the functions for Active Burst Mode, Auto Restart Mode and Latched Off Mode. The Active Burst Mode and the Auto Restart Mode are combined with an Adjustable Blanking Window which is depending on the external Soft Start capacitor. By means of this Adjustable Blanking Window an accidentally entering of the Active Burst Mode is avoided. Furthermore the overload detection can be deactivated for a certain time.

### 3.6.1 Adjustable Blanking Window

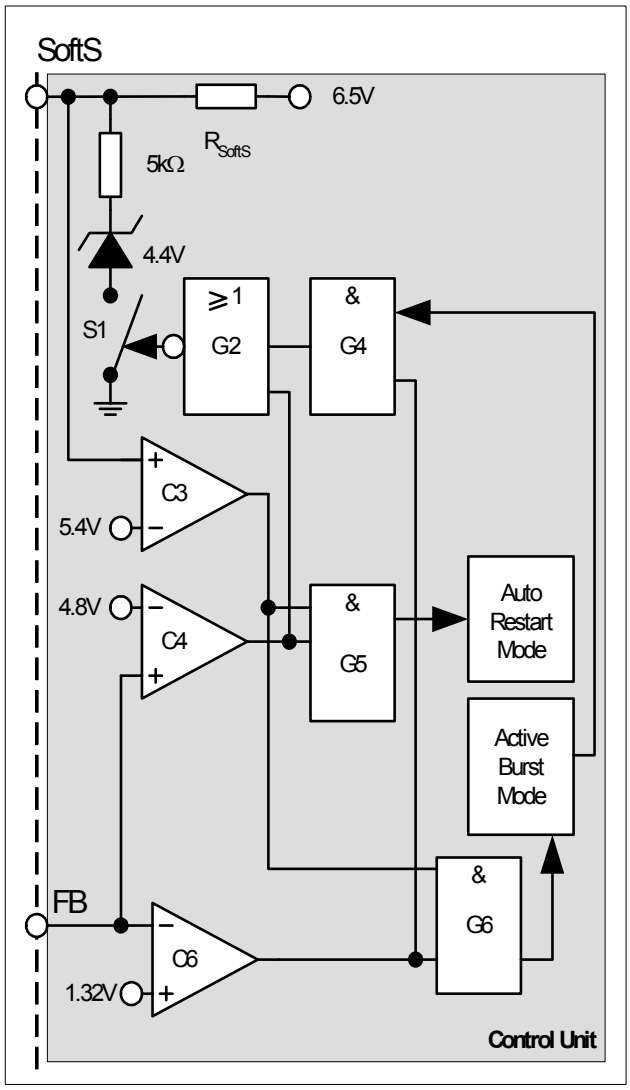



*Figure 15 Adjustable Blanking Window*

$V_{SoftS}$ is clamped at 4.4V by the closed switch S1 after the SMPS is settled. If overload occurs $V_{FB}$ is exceeding 4.8V. Auto Restart Mode can't be entered as the gate G5 is still blocked by the comparator C3. But after $V_{FB}$ has exceeded 4.8V the switch S1 is opened via the gate G2. The external Soft Start capacitor can now be charged further by the integrated pull up resistor $R_{SoftS}$. The comparator C3 releases the gates G5 and G6 once $V_{Softs}$ has exceeded 5.4V. Therefore there is no entering of Auto Restart Mode possible during this charging time of the external capacitor $C_{SoftS}$. The same procedure happens to the external Soft Start capacitor if a low load condition is detected by comparator C6 when $V_{FB}$ is falling below 1.32V. Only after $V_{SoftS}$ has exceeded

5.4V and $V_{FB}$ is still below 1.32V Active Burst Mode is entered. Once Active Burst Mode is entered gate G4 is blocked to ensure that the blanking window is only active before entering the Active Burst Mode.

### 3.6.2 Active Burst Mode

The controller provides Active Burst Mode for low load conditions at $V_{OUT}$. Active Burst Mode increases significantly the efficiency at light load conditions while supporting a low ripple on $V_{OUT}$ and fast response on load jumps. During Active Burst Mode which is controlled only by the FB signal the IC is always active and can therefore immediately response on fast changes at the FB signal. The Startup Cell is kept switched off to avoid increased power losses for the self supply.

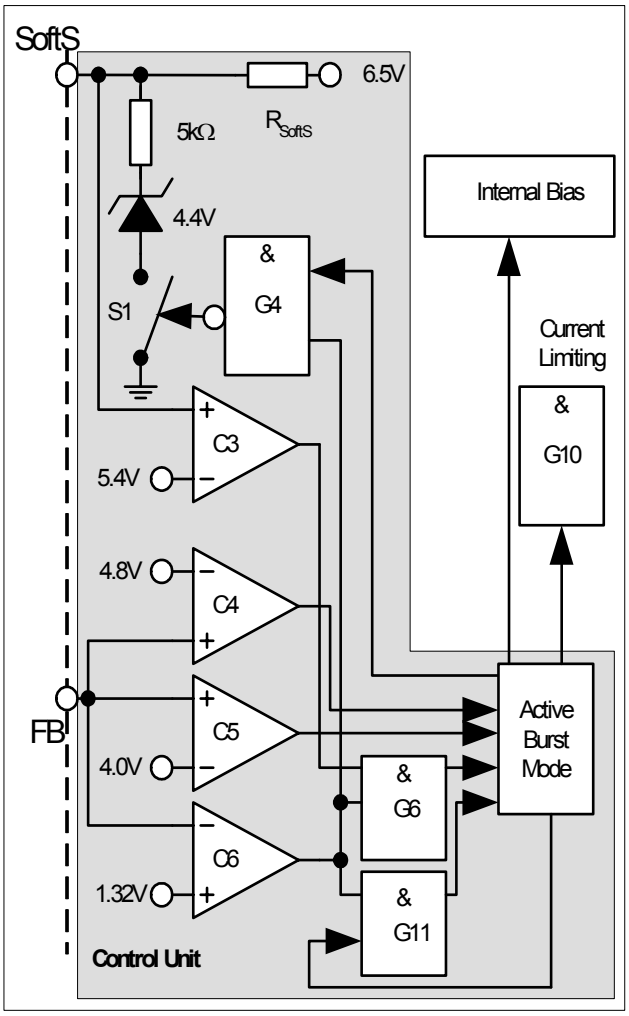



*Figure 16 Active Burst Mode*

The Active Burst Mode is located in the Control Unit. Figure 16 shows the related components.

#### 3.6.2.1 Entering Active Burst Mode

The FB signal is always observed by the comparator C6 if the voltage level falls below 1.32V. In that case the switch S1 is released which allows the capacitor $C_{SoftS}$ to be charged starting from the clamped voltage level at 4.4V in normal operating mode. The gate G11 is blocked before entering Active Burst Mode. If $V_{SoftS}$ exceeds 5.4V the comparator C3 releases the gate G6 to enter the Active Burst Mode. The time window that is generated by combining the FB and SoftS signals with gate G6 avoids a sudden entering of the Active Burst Mode due to large load jumps. This time window can be adjusted by the external capacitor $C_{SoftS}$.

After entering Active Burst Mode a burst flag is set which blocks the gate G4 and the internal bias is switched off in order to reduce the current consumption of the IC down to ca. 1.1mA. In this Off State Phase the IC is no longer self supplied so that therefore $C_{VCC}$ has to provide the VCC current (see Figure 17). Furthermore gate G11 is then released to start the next burst cycle once 1.32V is again exceeded.

It has to be ensured by the application that the VCC remains above the Undervoltage Lockout Level of 8.5V to avoid that the Startup Cell is accidentally switched on. Otherwise power losses are significantly increased. The minimum VCC level during Active Burst Mode is depending on the load conditions and the application. The lowest VCC level is reached at no load conditions at $V_{OUT}$.

#### 3.6.2.2 Working in Active Burst Mode

After entering the Active Burst Mode the FB voltage rises as $V_{OUT}$ starts to decrease due to the inactive PWM section. Comparator C5 observes the FB signal if the voltage level 4V is exceeded. In that case the internal circuit is again activated by the internal Bias to start with switching. As now in Active Burst Mode the gate G10 is released the current limit is only 0.257V to reduce the conduction losses and to avoid audible noise. If the load at $V_{OUT}$ is still below the starting level for the Active Burst Mode the FB signal decreases down to 1.32V. At this level C6 deactivates again the internal circuit by switching off the internal Bias. The gate G11 is released as after entering Active Burst Mode the burst flag is set. If working in Active Burst Mode the FB voltage is changing like a saw tooth between 1.32V and 4V (see figure 17).

#### 3.6.2.3 Leaving Active Burst Mode

The FB voltage immediately increases if there is a high load jump. This is observed by comparator C4. As the current limit is ca. 26% during Active Burst Mode a certain load jump is needed that FB can exceed 4.8V. At this time C4 resets the Active Burst Mode which also blocks C12 by the

gate G10. Maximum current can now be provided to stabilize $V_{OUT}$.

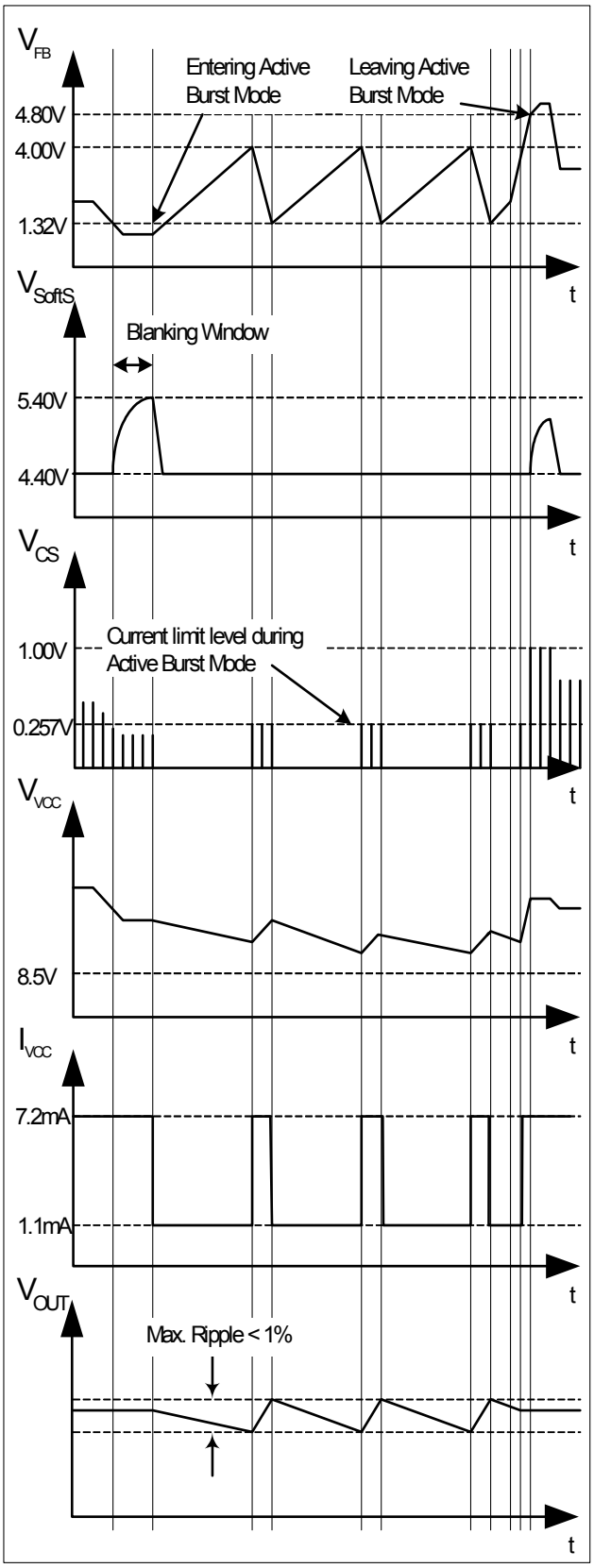



*Figure 17 Signals in Active Burst Mode*

### 3.6.3 Protection Modes

The IC provides several protection features which are separated into two categories. Some enter Latched Off Mode, the others enter Auto Restart Mode. The Latched Off Mode can only be reset if VCC is falling below 6V. Both modes prevent the SMPS from destructive states. The following table shows the relationship between possible system failures and the chosen protection modes.

| | |
|---|---|
| VCC Overvoltage | Latched Off Mode |
| Overtemperature | Latched Off Mode |
| Short Winding/Short Diode | Latched Off Mode |
| Overload | Auto Restart Mode |
| Open Loop | Auto Restart Mode |
| VCC Undervoltage | Auto Restart Mode |
| Short Optocoupler | Auto Restart Mode |

#### 3.6.3.1 Latched Off Mode

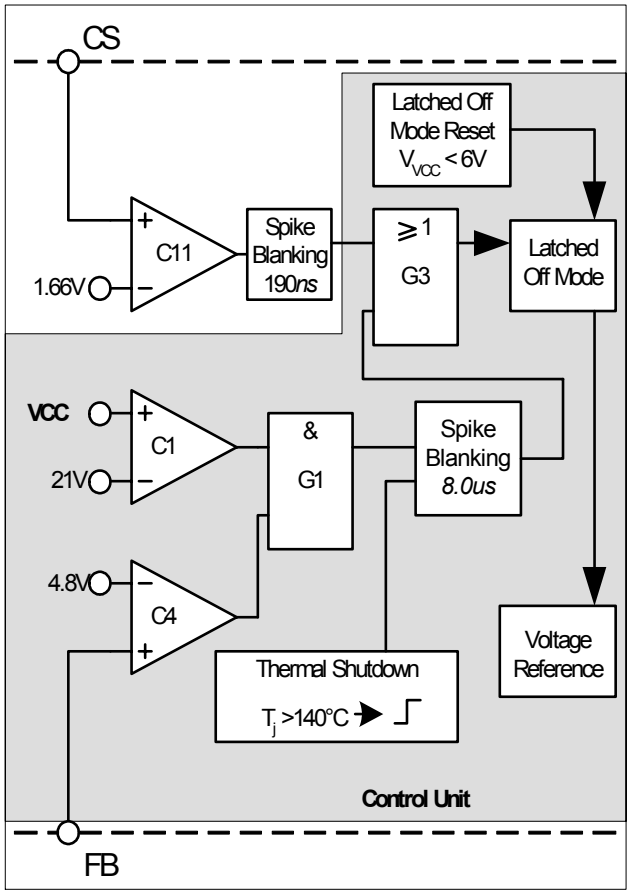



*Figure 18 Latched Off Mode*

The VCC voltage is observed by comparator C1 if 21V is exceeded. The output of C1 is combined with the output of C4 which observes FB signal if 4.8V is exceeded. Therefore the overvoltage detection is only activated if the FB signal is

outside the operating range > 4.8V, e.g. when Open Loop happens. Therewith small voltage overshoots of $V_{VCC}$ during normal operating can not start the Latched Off Mode.

The internal Voltage Reference is switched off once Latched Off Mode is entered in order to reduce the current consumption of the IC as much as possible. Latched Off Mode can only be reset by decreasing $V_{VCC}$ < 6V. In this stage only the UVLO is working which controls the Startup Cell by switching on/off at $V_{VCCon}$/$V_{VCCoff}$. In this phase the average current consumption is only 300µA. As there is no longer a self supply by the auxiliary winding VCC drops. The Undervoltage Lockout switches on the integrated Startup Cell when VCC falls below 8.5V. The Startup Cell is switched off again when VCC has exceeded 15V. As the Latched Off Mode was entered there is no Start Up Phase after VCC has exceeded the switch-on level of the Undervoltage Lockout. Therefore VCC changes between the switch-on and switch-off levels of the Undervoltage Lockout with a saw tooth shape (see Figure 19).

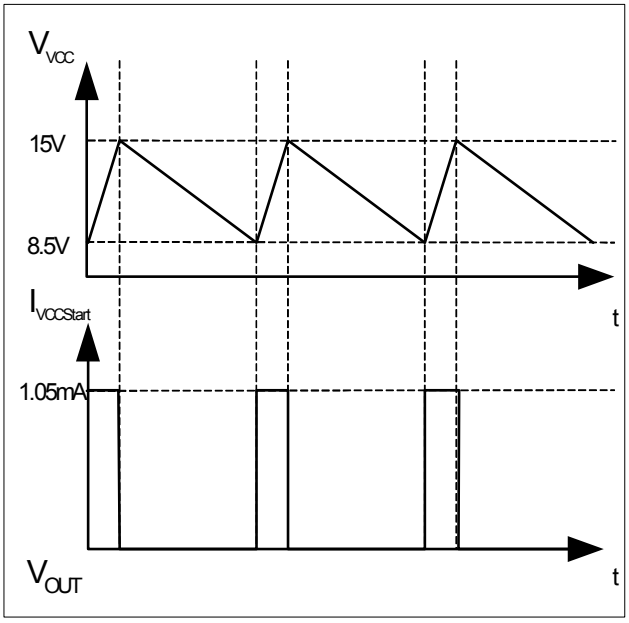



*Figure 19 Signals in Latched Off Mode*

After detecting a junction temperature higher than 140°C Latched Off Mode is entered.

The signals coming from the temperature detection and VCC overvoltage detection are fed into a spike blanking with a time constant of 8.0µs to ensure system reliability.

Furthermore short winding and short diode on the secondary side can be detected by the comparator C11 which is in parallel to the propagation delay compensated current limit comparator C10. In normal operating mode comparator C10 keeps the maximum level of the CS signal at 1V. If there is a failure such as short winding or short diode C10 is no longer able to limit the CS signal at 1V. C11 detects then the over current and enters immediately the Latched Off Mode to keep the SMPS in a safe stage.

### 3.6.3.2 Auto Restart Mode

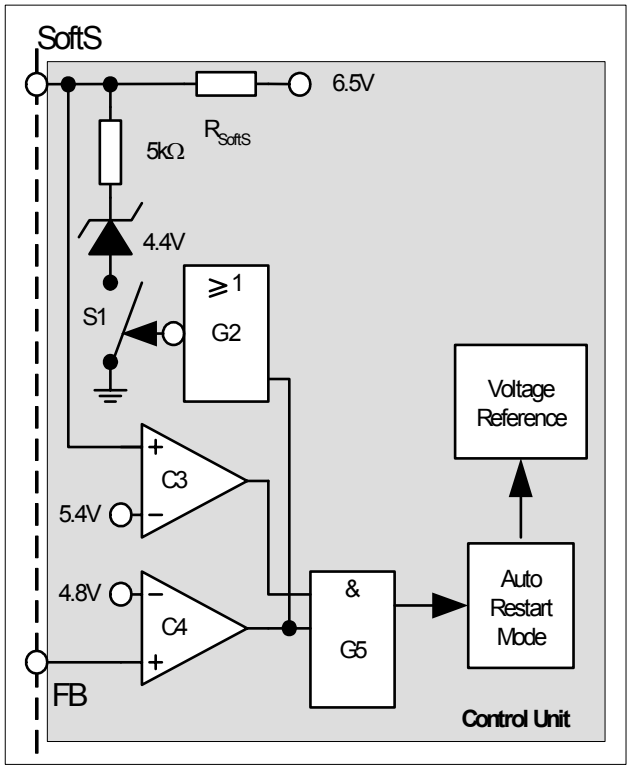



*Figure 20 Auto Restart Mode*

In case of Overload or Open Loop FB exceeds 4.8V which will be observed by C4. At this time S1 is released that $V_{SoftS}$ can increase. If $V_{SoftS}$ exceeds 5.4V which is observed by C3 Auto Restart Mode is entered as both inputs of the gate G5 are high. In combining the FB and SoftS signals there is a blanking window generated which prevents the system to enter Auto Restart Mode due to large load jumps. This time window is the same as for the Active Burst Mode and can therefore be adjusted by the external $C_{SoftS}$.

In case of VCC undervoltage the UVLO starts a new startup cycle.

Short Optocoupler leads to VCC undervoltage as there is now self supply after activating the internal reference and bias.

In contrast to the Latched Off Mode there is always a Startup Phase with switching cycles in Auto Restart Mode. After this Start Up Phase the conditions are again checked whether the failure is still present. Normal operation is proceeded once the failure mode is removed that leads to Auto Restart Mode.

# 4 Electrical Characteristics

*Note: All voltages are measured with respect to ground (Pin 8). The voltage levels are valid if other ratings are not violated.*

## 4.1 Absolute Maximum Ratings

*Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 7 (VCC) is discharged before assembling the application circuit.*

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| HV Voltage | $V_{HV}$ | - | 500V | V | |
| VCC Supply Voltage | $V_{VCC}$ | -0.3 | 22 | V | |
| FB Voltage | $V_{FB}$ | -0.3 | 6.5 | V | |
| SoftS Voltage | $V_{SoftS}$ | -0.3 | 6.5 | V | |
| Gate Voltage | $V_{Gate}$ | -0.3 | 22 | V | Internally clamped at 11.5V |
| CS Voltage | $V_{CS}$ | -0.3 | 6.5 | V | |
| Junction Temperature | $T_j$ | -40 | 150 | °C | |
| Storage Temperature | $T_S$ | -55 | 150 | °C | |
| Total Power Dissipation | $P_{totDSO8}$ | - | 0.45 | W | PG-DSO-8-8, $T_{amb}$ < 50°C |
| | $P_{totDIP8}$ | - | 0.90 | W | PG-DIP-8-6, $T_{amb}$ < 50°C |
| Thermal Resistance Junction-Ambient | $R_{thJADSO8}$ | - | 185 | K/W | PG-DSO-8-8 |
| | $R_{thJADIP8}$ | - | 90 | K/W | PG-DIP-8-6 |
| ESD capability (incl. Pin HV) | $V_{ESD}$ | - | 3 | kV | Human body model[1)] |

1) According to EIA/JESD22-A114-B (discharging a 100pF capacitor through a 1.5kΩ series resistor)

## 4.2 Operating Range

*Note: Within the operating range the IC operates as described in the functional description.*

| Parameter | Symbol | Limit Values | | Unit | Remarks |
|---|---|---|---|---|---|
| | | min. | max. | | |
| VCC Supply Voltage | $V_{VCC}$ | $V_{VCCoff}$ | 20 | V | |
| Junction Temperature of Controller | $T_{jCon}$ | -25 | 130 | °C | Max value limited due to thermal shut down of controller |

## 4.3 Characteristics

### 4.3.1 Supply Section

*Note: The electrical characteristics involve the spread of values guaranteed within the specified supply voltage and junction temperature range $T_J$ from – 25 °C to 130 °C. Typical values represent the median values, which are related to 25°C. If not otherwise stated, a supply voltage of $V_{CC}$ = 15 V is assumed.*

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Start Up Current | $I_{VCCstart}$ | - | 170 | 220 | µA | $V_{VCC}$=14V |
| VCC Charge Current | $I_{VCCcharge1}$ | -1.60 | -1.05 | -0.55 | mA | $V_{VCC}$= 0V |
| | $I_{VCCcharge2}$ | - | -0.88 | - | mA | $V_{VCC}$=14V |
| Start Up Cell Leakage Current | $I_{StartLeak}$ | - | 2 | 20 | µA | $V_{VCC}$>16V |
| Supply Current with Inactive Gate | $I_{VCCsup1}$ | - | 6.0 | 7.5 | mA | |
| Supply Current with Active Gate ($C_{Load}$=1nF) | $I_{VCCsup2}$ | - | 7.2 | 8.7 | mA | $V_{SoftS}$ = 4.4V<br>$I_{FB}$ = 0 |
| Supply Current in Latched Off Mode | $I_{VCClatch}$ | - | 300 | - | µA | $I_{FB}$ = 0<br>$I_{Softs}$ = 0 |
| Supply Current in Auto Restart Mode with Inactive Gate | $I_{VCCrestart}$ | - | 300 | - | µA | $I_{FB}$ = 0<br>$I_{Softs}$ = 0 |
| Supply Current in Active Burst Mode with Inactive Gate | $I_{VCCburst1}$ | - | 1.1 | 1.3 | mA | $V_{FB}$ = 2.5V<br>$V_{SoftS}$ = 4.4V |
| | $I_{VCCburst2}$ | - | 1.0 | 1.2 | mA | $V_{VCC}$ = 9V<br>$V_{FB}$ = 2.5V<br>$V_{SoftS}$ = 4.4V |
| VCC Turn-On Threshold<br>VCC Turn-Off Threshold<br>VCC Turn-On/Off Hysteresis | $V_{VCCon}$<br>$V_{VCCoff}$<br>$V_{VCChys}$ | 14.2<br>8.0<br>- | 15.0<br>8.5<br>6.5 | 15.8<br>9.0<br>- | V<br>V<br>V | |

### 4.3.2 Internal Voltage Reference

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Trimmed Reference Voltage | $V_{REF}$ | 6.37 | 6.50 | 6.63 | V | measured at pin FB<br>$I_{FB}$ = 0 |

### 4.3.3 PWM Section

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Fixed Oscillator Frequency | $f_{OSC1}$ | 98 | 110 | 119 | kHz | |
| | $f_{OSC2}$ | 102 | 110 | 117 | kHz | $T_j$ = 25°C |
| Max. Duty Cycle | $D_{max}$ | 0.67 | 0.72 | 0.77 | | |
| Min. Duty Cycle | $D_{min}$ | 0 | - | - | | $V_{FB}$ < 0.3V |
| PWM-OP Gain | $A_V$ | 3.5 | 3.7 | 3.9 | | |
| Max. Level of Voltage Ramp | $V_{Max-Ramp}$ | - | 0.85 | - | V | |
| $V_{FB}$ Operating Range Min Level | $V_{FBmin}$ | 0.3 | 0.7 | - | V | |
| $V_{FB}$ Operating Range Max level | $V_{FBmax}$ | - | - | 4.75 | V | CS=1V limited by Comparator C4[1)] |
| Feedback Pull-Up Resistor | $R_{FB}$ | 16 | 20 | 27 | kΩ | |
| Soft-Start Pull-Up Resistor | $R_{SoftS}$ | 39 | 50 | 62 | kΩ | |

1) Design characteristic (not meant for production testing)

### 4.3.4 Control Unit

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Deactivation Level for SoftS Comparator C7 by C2 | $V_{SoftSC2}$ | 3.85 | 4.00 | 4.15 | V | $V_{FB}$ > 5V |
| Clamped $V_{SoftS}$ Voltage during Normal Operating Mode | $V_{SoftSclmp}$ | 4.23 | 4.40 | 4.57 | V | $V_{FB}$ < 4.5V |
| Activation Limit of Comparator C3 | $V_{SoftSC3}$ | 5.20 | 5.40 | 5.60 | V | $V_{FB}$ > 5V |
| SoftS Startup Current | $I_{SoftSstart}$ | - | 1.9 | - | mA | $V_{SoftS}$ = 0V |
| Active Burst Mode Level for Comparator C6 | $V_{FBC6}$ | 1.23 | 1.32 | 1.40 | V | $V_{SoftS}$ > 5.6V |
| Active Burst Mode Level for Comparator C5 | $V_{FBC5}$ | 3.85 | 4.00 | 4.15 | V | After Active Burst Mode is entered |
| Over Load & Open Loop Detection Limit for Comparator C4 | $V_{FBC4}$ | 4.62 | 4.80 | 4.98 | V | $V_{SoftS}$ > 5.6V |
| Overvoltage Detection Limit | $V_{VCCOVP}$ | 20 | 21 | 22 | V | $V_{FB}$ > 5V |
| Latched Thermal Shutdown | $T_{jSD}$ | 130 | 140 | 150 | °C | guaranteed by design |
| Spike Blanking | $t_{Spike}$ | - | 8.0 | - | µs | |
| Power Down Reset for Latched Mode | $V_{VCCPD}$ | 4.0 | 6.0 | 7.5 | V | After Latched Off Mode is entered |

*Note: The trend of all the voltage levels in the Control Unit is the same regarding the deviation except* $V_{VCCOVP}$ *and* $V_{VCCPD}$

### 4.3.5 Current Limiting

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| Peak Current Limitation (incl. Propagation Delay Time) (see Figure 7) | $V_{csth}$ | 0.950 | 1.000 | 1.050 | V | $dV_{sense}$ / dt = 0.6V/µs |
| Over Current Detection for Latched Off Mode | $V_{CS1}$ | 1.570 | 1.66 | 1.764 | V | |
| Peak Current Limitation during Active Burst Mode | $V_{CS2}$ | 0.232 | 0.257 | 0.282 | V | $V_{FB}$ < 1.2V |
| Leading Edge Blanking | $t_{LEB}$ | - | 220 | - | ns | $V_{SoftS}$ = 4.4V |
| CS Spike Blanking for Comparator C11 | $t_{CSspike}$ | - | 190 | - | ns | |
| CS Input Bias Current | $I_{CSbias}$ | -1.0 | -0.2 | 0 | µA | $V_{CS}$ =0V |

### 4.3.6 Driver Section

| Parameter | Symbol | Limit Values | | | Unit | Test Condition |
|---|---|---|---|---|---|---|
| | | min. | typ. | max. | | |
| GATE Low Voltage | $V_{GATElow}$ | - | - | 1.2 | V | $V_{VCC}$ = 5 V<br>$I_{Gate}$ = 5 mA |
| | | - | - | 1.5 | V | $V_{VCC}$ = 5 V<br>$I_{Gate}$ = 20 mA |
| | | - | 0.8 | - | V | $I_{Gate}$ = 0 A |
| | | - | 1.6 | 2.0 | V | $I_{Gate}$ = 20 mA |
| | | -0.2 | 0.2 | - | V | $I_{Gate}$ = -20 mA |
| GATE High Voltage | $V_{GATEhigh}$ | - | 11.5 | - | V | $V_{VCC}$ = 20V<br>$C_L$ = 4.7nF |
| | | - | 10.5 | - | V | $V_{VCC}$ = 11V<br>$C_L$ = 4.7nF |
| | | - | 7.5 | - | V | $V_{VCC}$ = $V_{VCCoff}$ + 0.2V<br>$C_L$ = 4.7nF |
| GATE Rise Time (incl. Gate Rising Slope) | $t_{rise}$ | - | 150 | - | ns | $V_{Gate}$ = 2V ...9V[1)]<br>$C_L$ = 4.7nF |
| GATE Fall Time | $t_{fall}$ | - | 55 | - | ns | $V_{Gate}$ = 9V ...2V[1)]<br>$C_L$ = 4.7nF |
| GATE Current, Peak, Rising Edge | $I_{GATE}$ | -0.5 | - | - | A | $C_L$ = 4.7nF[2)] |
| GATE Current, Peak, Falling Edge | $I_{GATE}$ | - | - | 0.7 | A | $C_L$ = 4.7nF[2)] |

1) Transient reference value

2) Design characteristic (not meant for production testing)

# 5 Typical Performance Characteristics

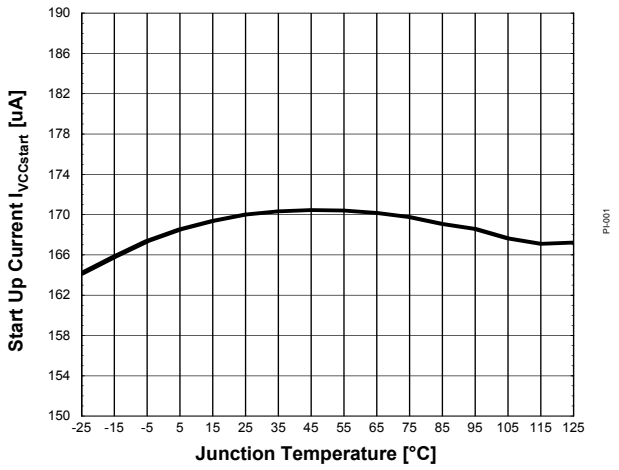



*Figure 21 Start Up Current $I_{VCCstart}$*

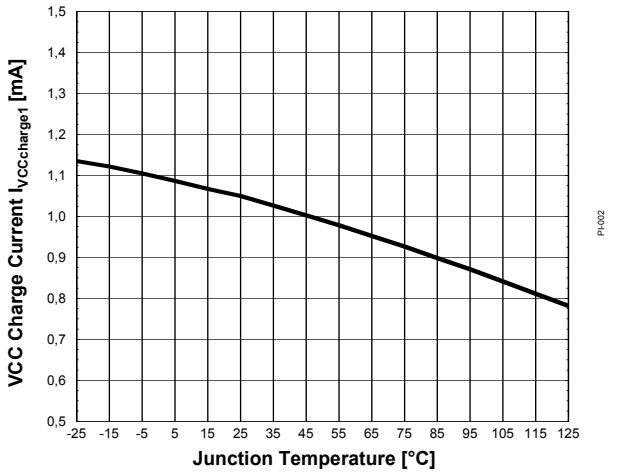



*Figure 22 VCC Charge Current $I_{VCCcharge1}$*

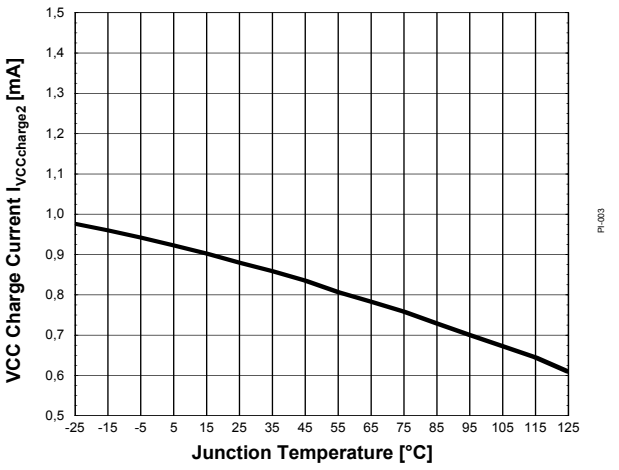



*Figure 23 VCC Charge Current $I_{VCCcharge2}$*

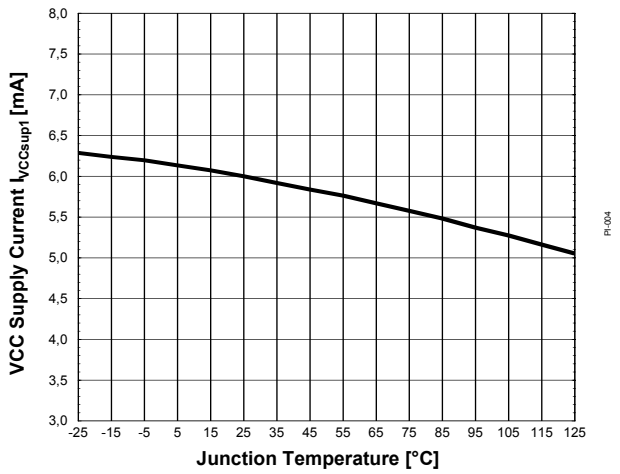



*Figure 24 VCC Supply Current $I_{VCCsup1}$*

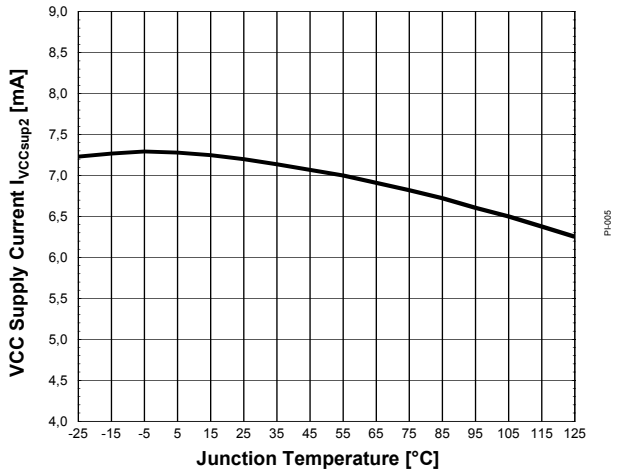



*Figure 25 VCC Supply Current $I_{VCCsup2}$*

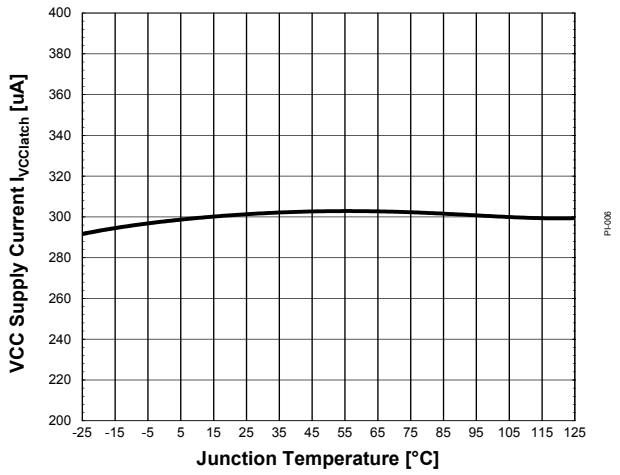



*Figure 26 VCC Supply Current $I_{VCClatch}$*

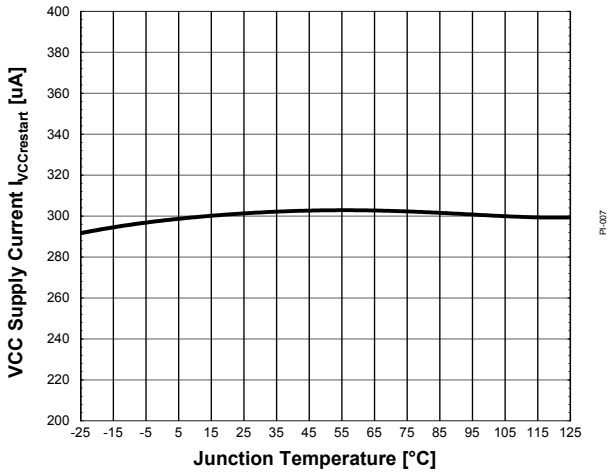



*Figure 27 VCC Supply Current $I_{VCCrestart}$*

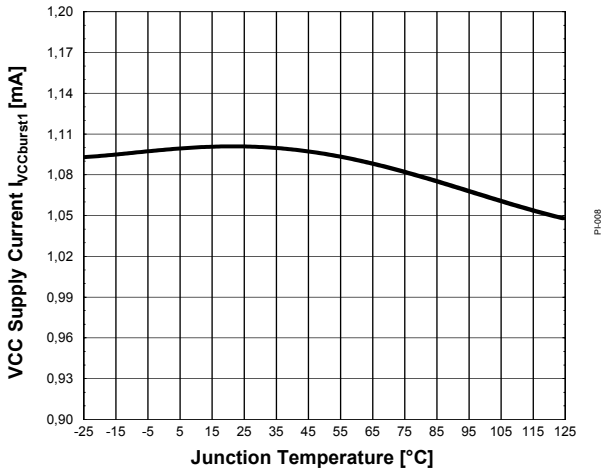



*Figure 28 VCC Supply Current $I_{VCCburst1}$*

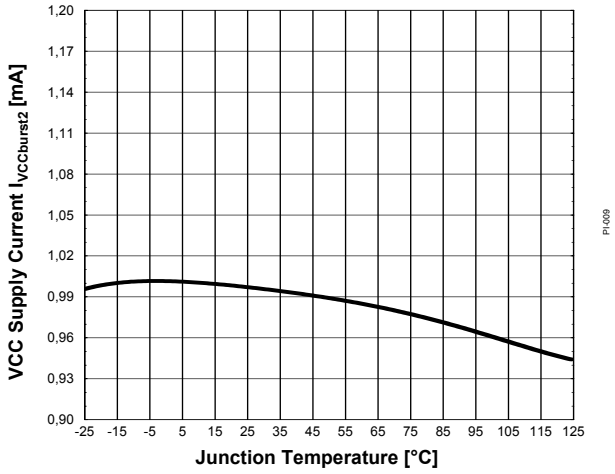



*Figure 29 VCC Supply Current $I_{VCCburst2}$*

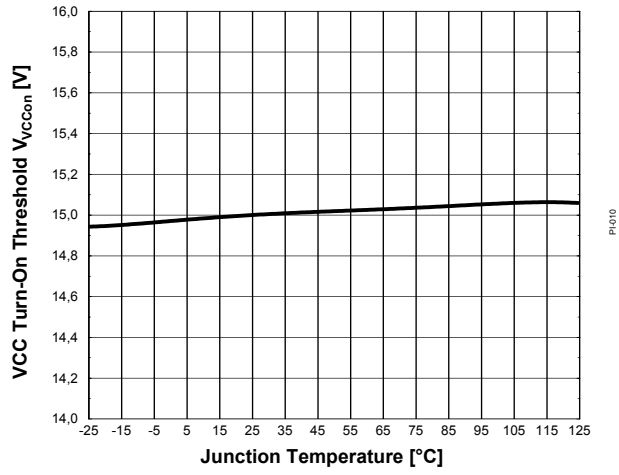



*Figure 30 VCC Turn-On Threshold $V_{VCCon}$*

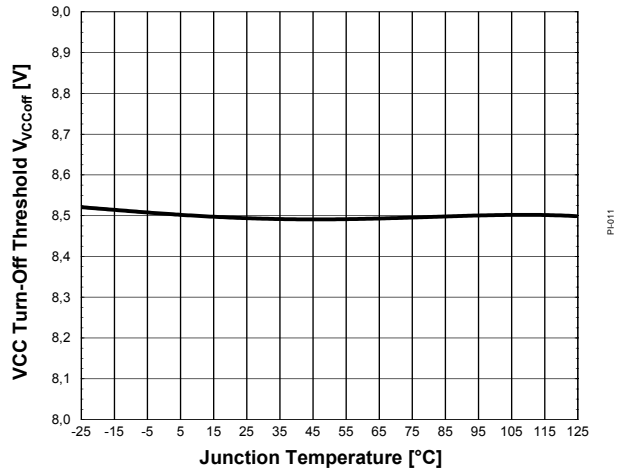



*Figure 31 VCC Turn-Off Threshold $V_{VCCoff}$*

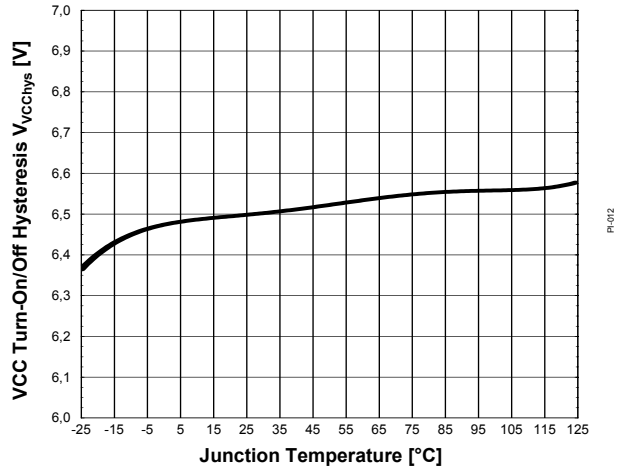



*Figure 32 VCC Turn-On/Off Hysteresis $V_{VCChys}$*

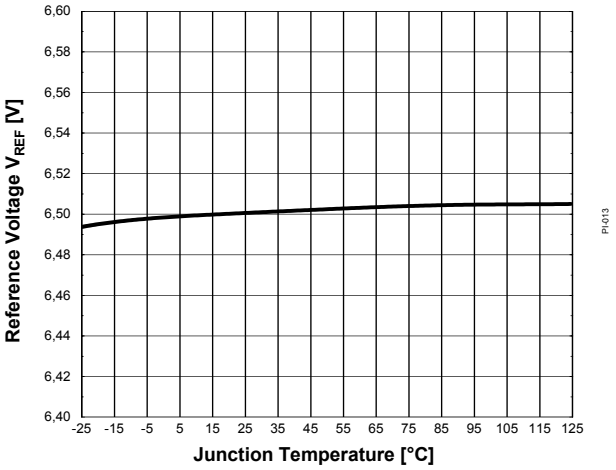



*Figure 33 Reference Voltage $V_{REF}$*

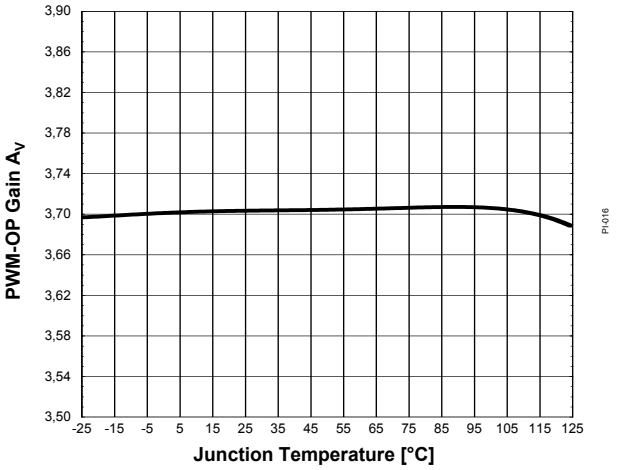



*Figure 36 PWM-OP Gain $A_V$*

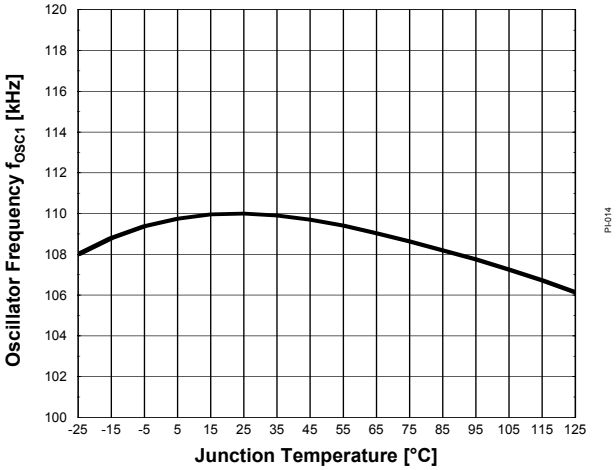



*Figure 34 Oscillator Frequency $f_{OSC1}$*

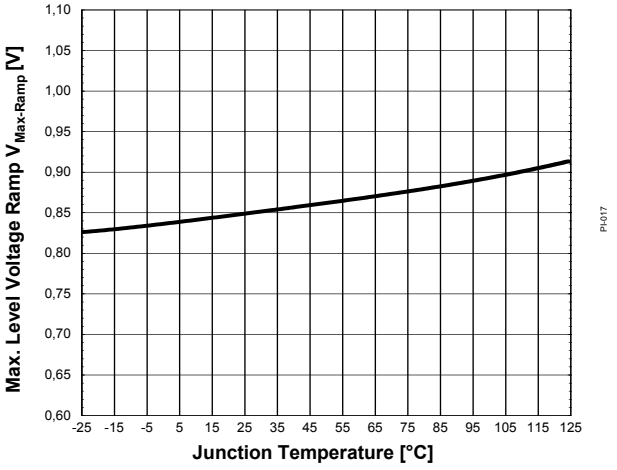



*Figure 37 Max. Level Voltage Ramp $V_{Max-Ramp}$*

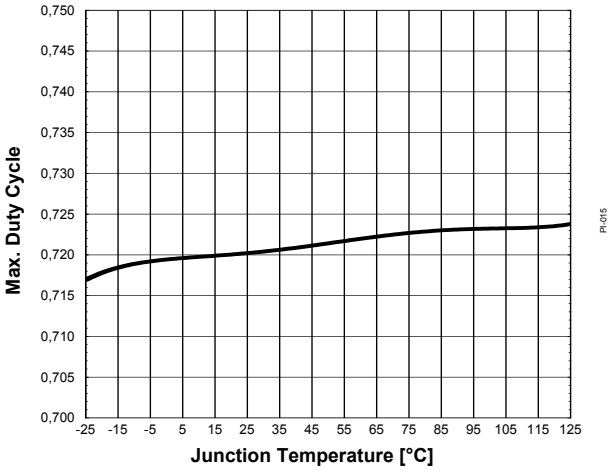



*Figure 35 Max. Duty Cycle $D_{max}$*

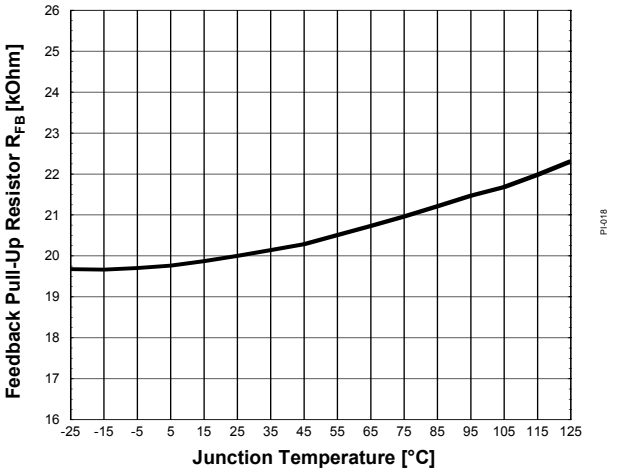



*Figure 38 Feedback Pull-Up Resistor $R_{FB}$*

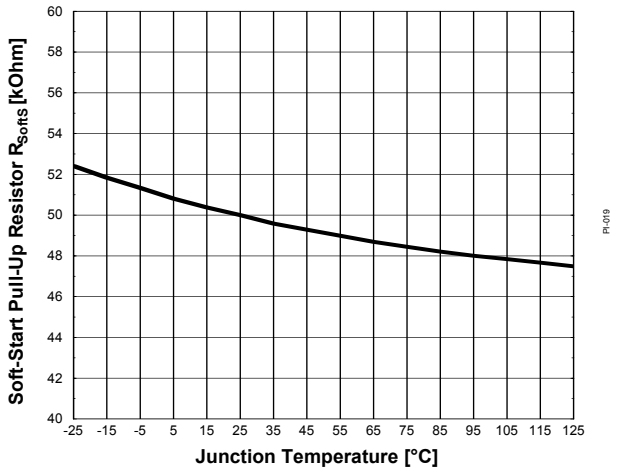



*Figure 39 Soft-Start Pull-Up Resistor $R_{SoftS}$*

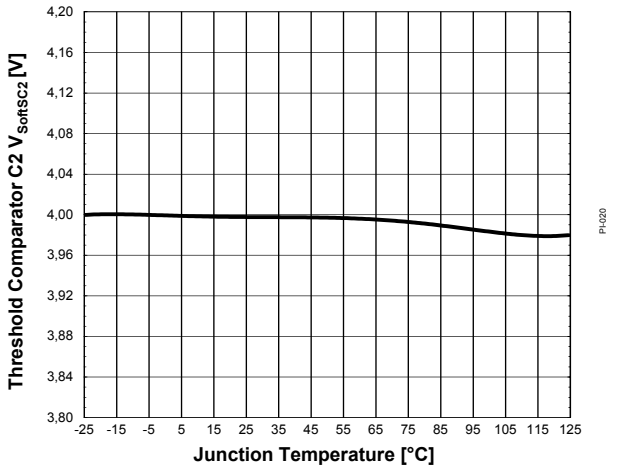



*Figure 40 Threshold Comparator C2 $V_{SoftSC2}$*

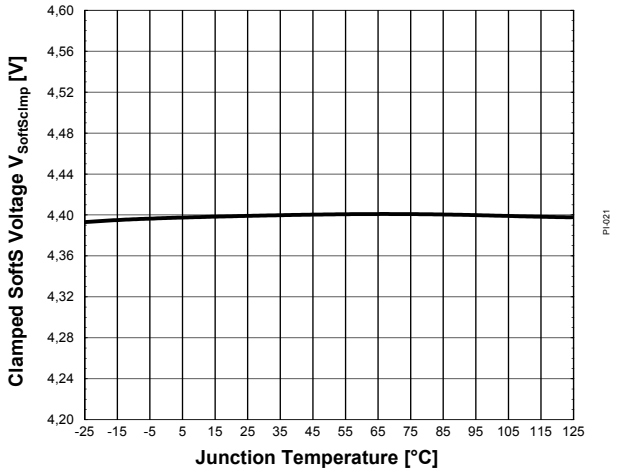



*Figure 41 Clamped SoftS Voltage $V_{SoftSclmp}$*

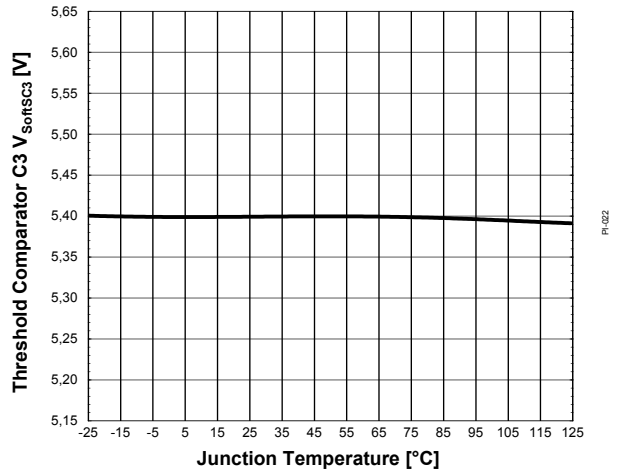



*Figure 42 Threshold Comparator C3 $V_{SoftSC3}$*

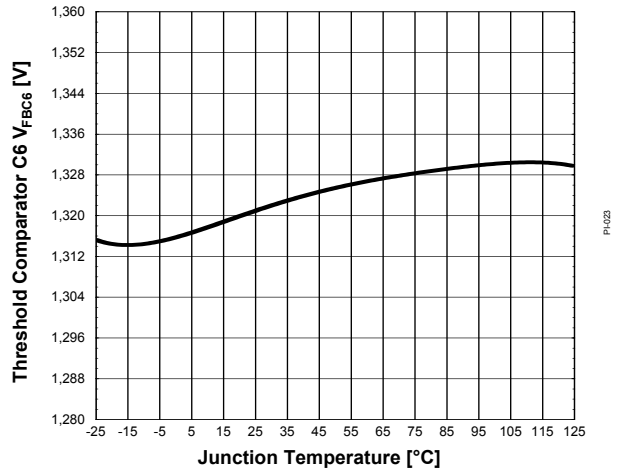



*Figure 43 Threshold Comparator C6 $V_{FBC6}$*

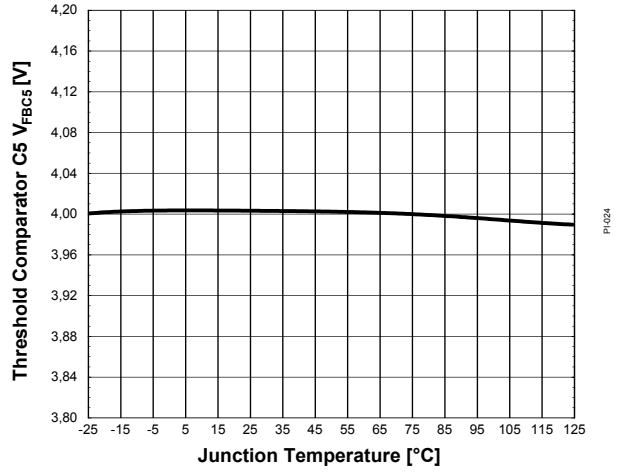



*Figure 44 Threshold Comparator C5 $V_{FBC5}$*

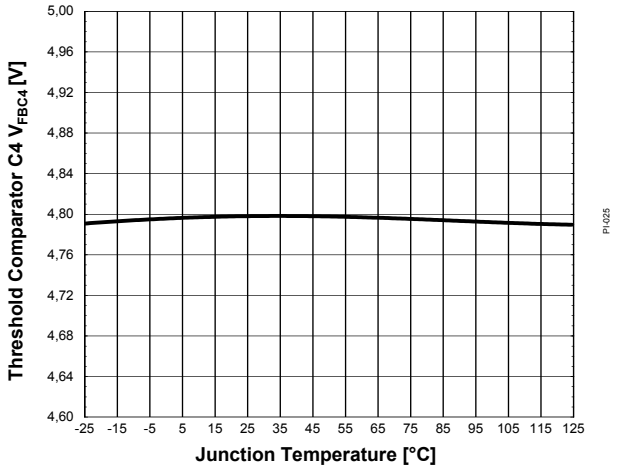



*Figure 45 Threshold Comparator C4 $V_{FBC4}$*

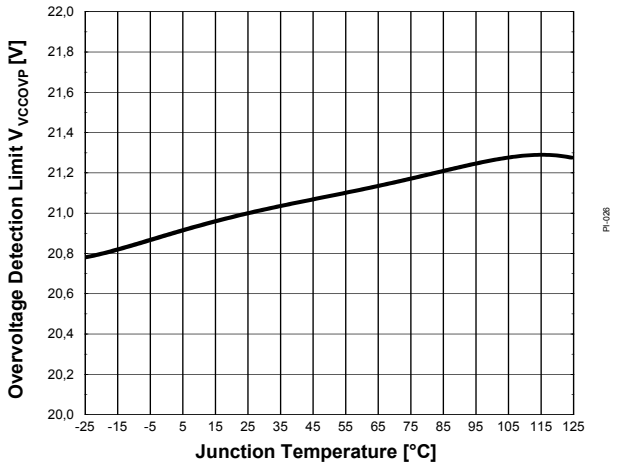



*Figure 46 Overvoltage Detection Limit $V_{VCCOVP}$*

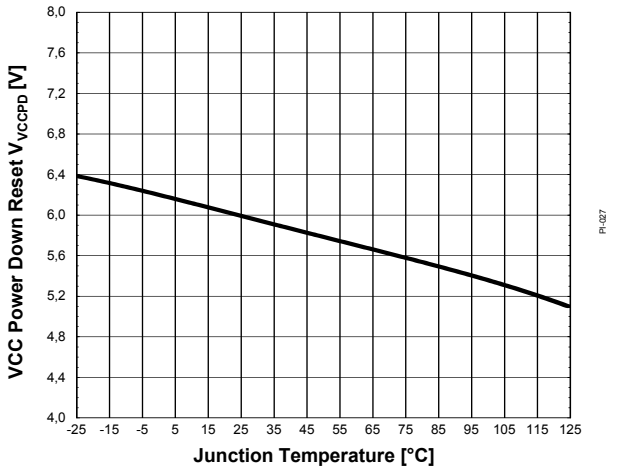



*Figure 47 Threshold Power Down Reset $V_{VCCPD}$*

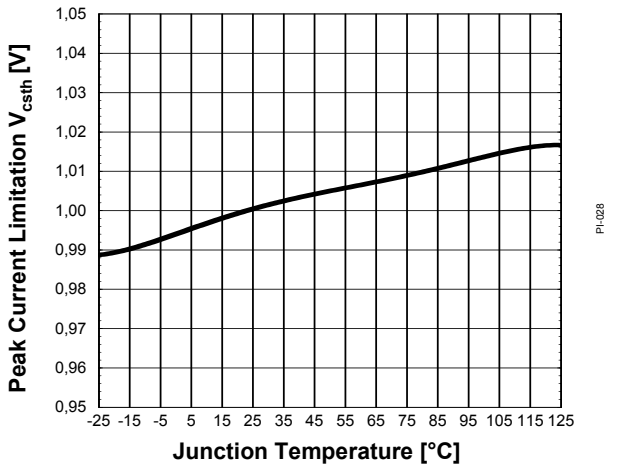



*Figure 48 Peak Current Limitation $V_{csth}$*

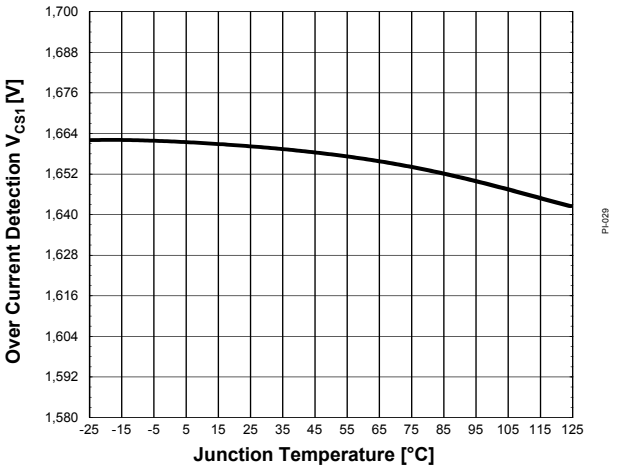



*Figure 49 Over Current Detection $V_{CS1}$*

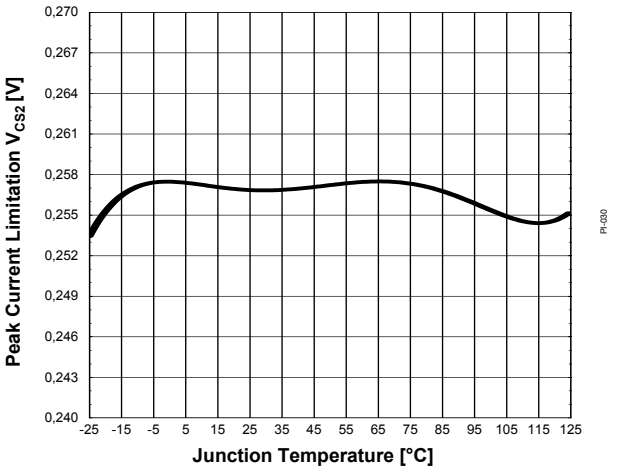



*Figure 50 Peak Current Limitation $V_{CS2}$*

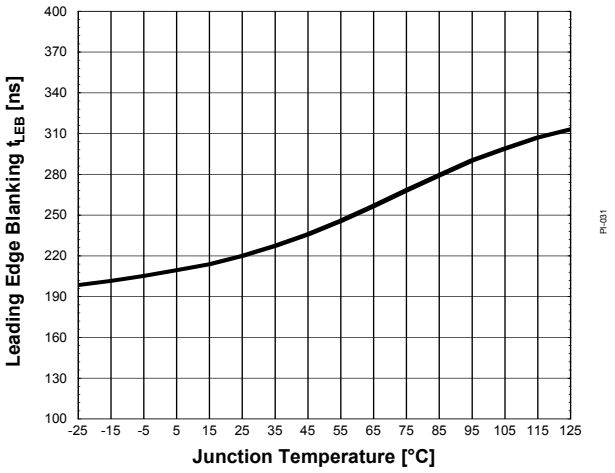



*Figure 51 Leading Edge Blanking $t_{LEB}$*

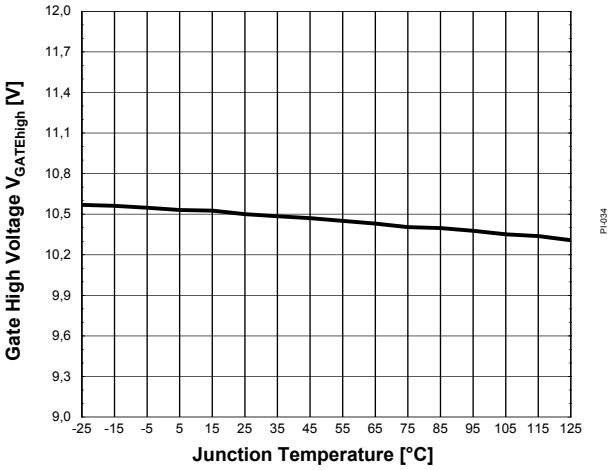



*Figure 54 GATE High Voltage $V_{GATEhigh}$*

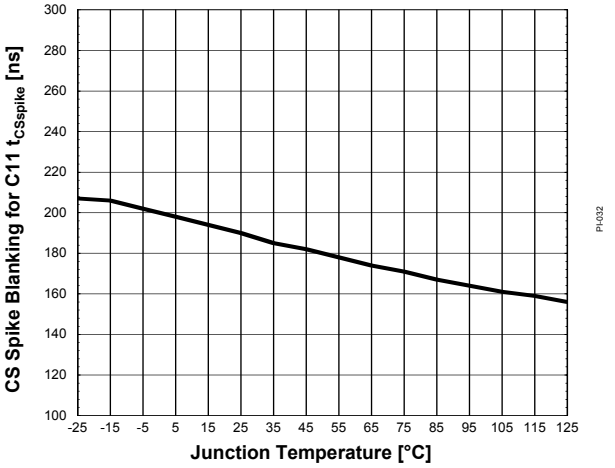



*Figure 52 CS Spike Blanking for C11 $t_{CSspike}$*

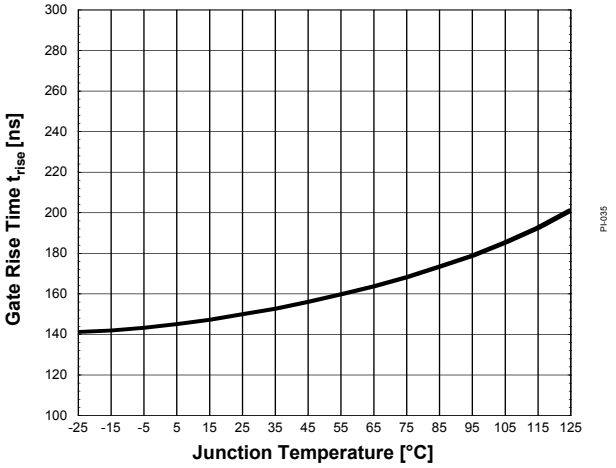



*Figure 55 GATE Rise Time $t_{rise}$*

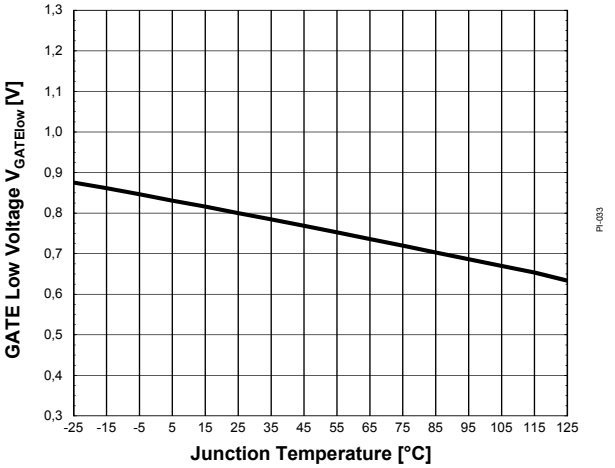



*Figure 53 GATE Low Voltage $V_{GATElow}$*

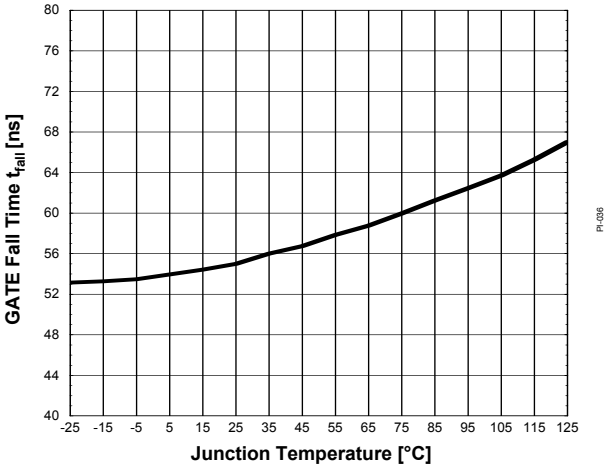



*Figure 56 GATE Fall Time $t_{fall}$*