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## **iCE40™ LP/HX Family Data Sheet**

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DS1040 Version 3.3, March 2017

## Features

- Flexible Logic Architecture**
  - Five devices with 384 to 7,680 LUT4s and 10 to 206 I/Os
- Ultra Low Power Devices**
  - Advanced 40 nm low power process
  - As low as 21  $\mu$ A standby power
  - Programmable low swing differential I/Os
- Embedded and Distributed Memory**
  - Up to 128 kbits sysMEM™ Embedded Block RAM
- Pre-Engineered Source Synchronous I/O**
  - DDR registers in I/O cells
- High Current LED Drivers**
  - Three High Current Drivers used for three different LEDs or one RGB LED
- High Performance, Flexible I/O Buffer**
  - Programmable sysIO™ buffer supports wide range of interfaces:
    - LVCMOS 3.3/2.5/1.8
    - LVDS25E, subLVDS
    - Schmitt trigger inputs, to 200 mV typical hysteresis
  - Programmable pull-up mode
- Flexible On-Chip Clocking**
  - Eight low-skew global clock resources
  - Up to two analog PLLs per device
- Flexible Device Configuration**
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- Broad Range of Package Options**
  - WLCSP, QFN, VQFP, TQFP, ucBGA, caBGA, and csBGA package options
  - Small footprint package options
    - As small as 1.40 mm x 1.48 mm
  - Advanced halogen-free packaging

**Table 1-1. iCE40 Family Selection Guide**

Part Number	LP384	LP640	LP1K	LP4K	LP8K	HX1K	HX4K	HX8K
Logic Cells (LUT + Flip-Flop)	384	640	1,280	3,520	7,680	1,280	3,520	7,680
RAM4K Memory Blocks	0	8	16	20	32	16	20	32
RAM4K RAM bits	0	32K	64K	80K	128K	64K	80K	128K
Phase-Locked Loops (PLLs)	0	0	1 <sup>1</sup>	2 <sup>2</sup>	2 <sup>2</sup>	1 <sup>1</sup>	2	2
Maximum Programmable I/O Pins	63	25	95	167	178	95	95	206
Maximum Differential Input Pairs	8	3	12	20	23	11	12	26
High Current LED Drivers	0	3	3	0	0	0	0	0
Package	Code	Programmable I/O: Max Inputs (LVDS25)						
16 WLCSP (1.40 mm x 1.48 mm, 0.35 mm)	SWG16		10(0) <sup>1</sup>	10(0) <sup>1</sup>				
32 QFN (5 mm x 5 mm, 0.5 mm)	SG32	21(3)						
36 ucBGA (2.5 mm x 2.5 mm, 0.4 mm)	CM36	25(3)		25(3) <sup>1</sup>				
49 ucBGA (3 mm x 3 mm, 0.4 mm)	CM49	37(6)		35(5) <sup>1</sup>				
81 ucBGA (4 mm x 4 mm, 0.4 mm)	CM81			63(8)	63(9) <sup>2</sup>	63(9) <sup>2</sup>		
81 csBGA (5 mm x 5 mm, 0.5 mm)	CB81			62(9) <sup>1</sup>				

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**Table 1-1. iCE40 Family Selection Guide (continued)**

84 QFN (7 mm x 7 mm, 0.5 mm)	QN84			67(7) <sup>1</sup>					
100 VQFP (14 mm x 14 mm, 0.5 mm)	VQ100						72(9) <sup>1</sup>		
121 ucBGA (5 mm x 5 mm, 0.4 mm)	CM121			95(12)	93(13)	93(13)			
121 csBGA (6 mm x 6 mm, 0.5 mm)	CB121			92(12)					
121 caBGA (9 mm x 9 mm, 0.8 mm)	BG121							93(13)	93(13)
132 csBGA (8 mm x 8 mm, 0.5 mm)	CB132						95(11)	95(12)	95(12)
144 TQFP (20 mm x 20 mm, 0.5 mm)	TQ144						96(12)	107(14)	
225 ucBGA (7 mm x 7 mm, 0.4 mm)	CM225				178(23)	178(23)			178(23)
256-ball caBGA (14 mm x 14 mm, 0.8 mm)	CT256								206(26)

1. No PLL available on the 16 WLCSP, 36 ucBGA, 81 csBGA, 84 QFN and 100 VQFP packages.

2. Only one PLL available on the 81 ucBGA package.

3. High Current I/Os only available on the 16 WLCSP package.

## Introduction

The iCE40 family of ultra-low power, non-volatile FPGAs has five devices with densities ranging from 384 to 7680 Look-Up Tables (LUTs). In addition to LUT-based, low-cost programmable logic, these devices feature Embedded Block RAM (EBR), Non-volatile Configuration Memory (NVCM) and Phase Locked Loops (PLLs). These features allow the devices to be used in low-cost, high-volume consumer and system applications. Select packages offer High-Current drivers that are ideal to drive three white LEDs, or one RGB LED.

The iCE40 devices are fabricated on a 40 nm CMOS low power process. The device architecture has several features such as programmable low-swing differential I/Os and the ability to turn off on-chip PLLs dynamically. These features help manage static and dynamic power consumption, resulting in low static power for all members of the family. The iCE40 devices are available in two versions – ultra low power (LP) and high performance (HX) devices.

The iCE40 FPGAs are available in a broad range of advanced halogen-free packages ranging from the space saving 1.40x1.48 mm WLCSP to the PCB-friendly 20x20 mm TQFP. Table 1-1 shows the LUT densities, package and I/O options, along with other key parameters.

The iCE40 devices offer enhanced I/O features such as pull-up resistors. Pull-up features are controllable on a “per-pin” basis.

The iCE40 devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash or be configured by an external master such as a CPU.

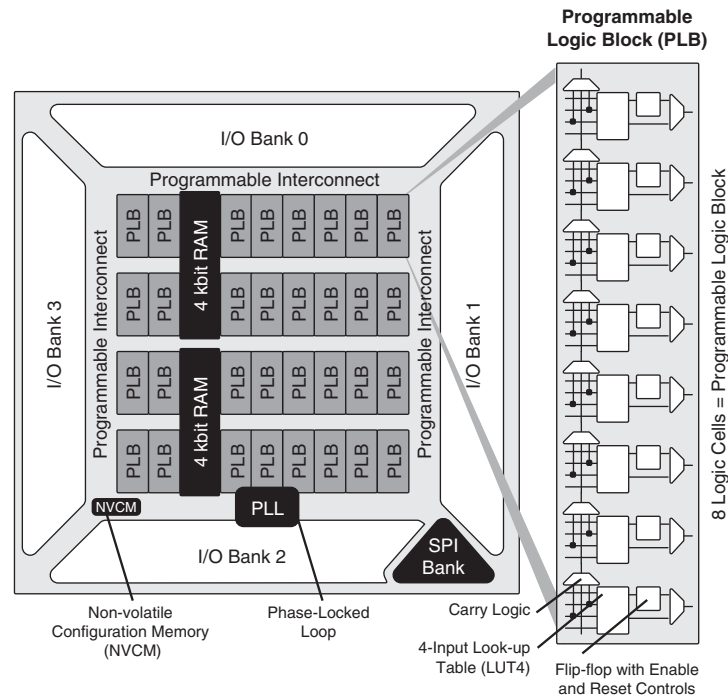
Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 family of devices. Popular logic synthesis tools provide synthesis library support for iCE40. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 FPGA family. By using these configurable soft core IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing their productivity.

## Architecture Overview

The iCE40 family architecture contains an array of Programmable Logic Blocks (PLB), sysCLOCK™ PLLs, Non-volatile Programmable Configuration Memory (NVCM) and blocks of sysMEM™ Embedded Block RAM (EBR) surrounded by Programmable I/O (PIO). Figure 2-1 shows the block diagram of the iCE40LP/HX1K device.

**Figure 2-1. iCE40LP/HX1K Device, Top View**



The logic blocks, Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either logic blocks or EBR blocks. The PIO cells are located at the periphery of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 family, there are up to four independent sysIO banks. Note on some packages  $V_{CCIO}$  banks are tied together. There are different types of I/O buffers on the different banks. Refer to the details in later sections of this document. The sysMEM EBRs are large 4 kbit, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO.

The iCE40 architecture also provides up to two sysCLOCK Phase Locked Loop (PLL) blocks. The PLLs have multiply, divide, and phase shifting capabilities that are used to manage the frequency and phase relationships of the clocks.

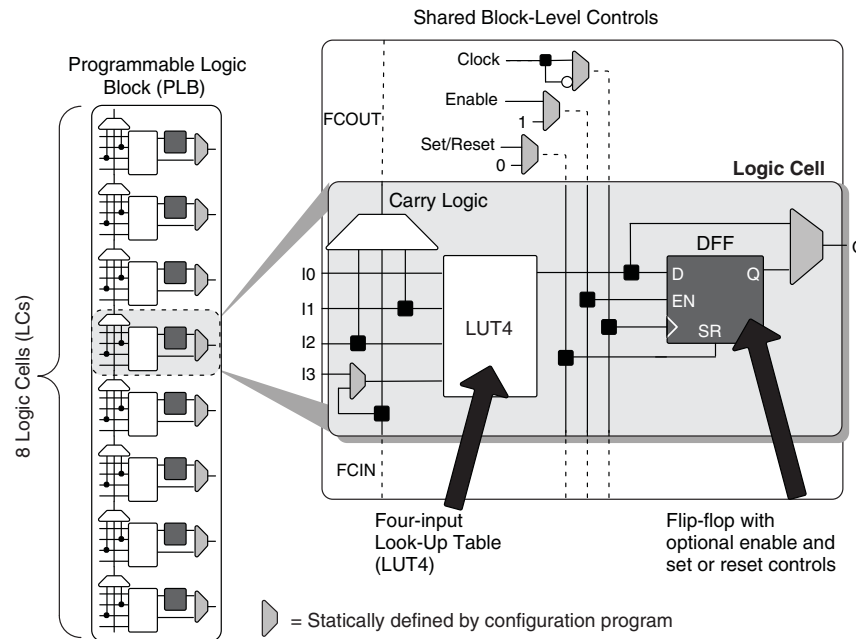
Every device in the family has a SPI port that supports programming and configuration of the device. The iCE40 includes on-chip, Nonvolatile Configuration Memory (NVCM).

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## PLB Blocks

The core of the iCE40 device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 2-2. Each LC contains one LUT and one register.

**Figure 2-2. PLB Block Diagram**



## Logic Cells

Each Logic Cell includes three primary logic elements shown in Figure 2-2.

- A four-input Look-Up Table (LUT4) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT4 element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUT4s to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtractors, comparators, binary counters and some wide, cascaded logic functions.

**Table 2-1. Logic Cell Signal Descriptions**

Function	Type	Signal Names	Description
Input	Data signal	I0, I1, I2, I3	Inputs to LUT4
Input	Control signal	Enable	Clock enable shared by all LCs in the PLB
Input	Control signal	Set/Reset <sup>1</sup>	Asynchronous or synchronous local set/reset shared by all LCs in the PLB.
Input	Control signal	Clock	Clock one of the eight Global Buffers, or from the general-purpose interconnects fabric shared by all LCs in the PLB
Input	Inter-PLB signal	FCIN	Fast carry in
Output	Data signals	O	LUT4 or registered output
Output	Inter-PFU signal	FCOUT	Fast carry out

1. If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

## Routing

There are many resources provided in the iCE40 devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

## Clock/Control Distribution Network

Each iCE40 device has eight global inputs, two pins on each side of the device. Note that not all GBINs are available in all packages.

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as GBIN[7:0] and the global buffers are identified as-GBUF[7:0]. These eight inputs may be used as general purpose I/O if they are not used to drive the clock nets. Global buffer GBUF7 in I/O Bank 3 also provides an optional direct LVDS25 or subLVDS differential clock input.

Table 2-2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input.

**Table 2-2. Global Buffer (GBUF) Connections to Programmable Logic Blocks**

Global Buffer	LUT Inputs	Clock	Reset	Clock Enable
GBUF0	Yes, any 4 of 8 GBUF Inputs	Yes	Yes	
GBUF1		Yes		Yes
GBUF2		Yes	Yes	
GBUF3		Yes		Yes
GBUF4		Yes	Yes	
GBUF5		Yes		Yes
GBUF6		Yes	Yes	
GBUF7		Yes		Yes

The maximum frequency for the global buffers are shown in the iCE40 External Switching Characteristics tables later in this document.

## Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

**Global Reset Control**

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

**sysCLOCK Phase Locked Loops (PLLs)**

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 devices have one or more sysCLOCK PLLs. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin or from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 6. The PLLOUT outputs can all be used to drive the iCE40 global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 2-3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the  $t_{LOCK}$  parameter has been satisfied.

For more details on the PLL, see TN1251, [iCE40 sysCLOCK PLL Design and Usage Guide](#).

**Figure 2-3. PLL Diagram**

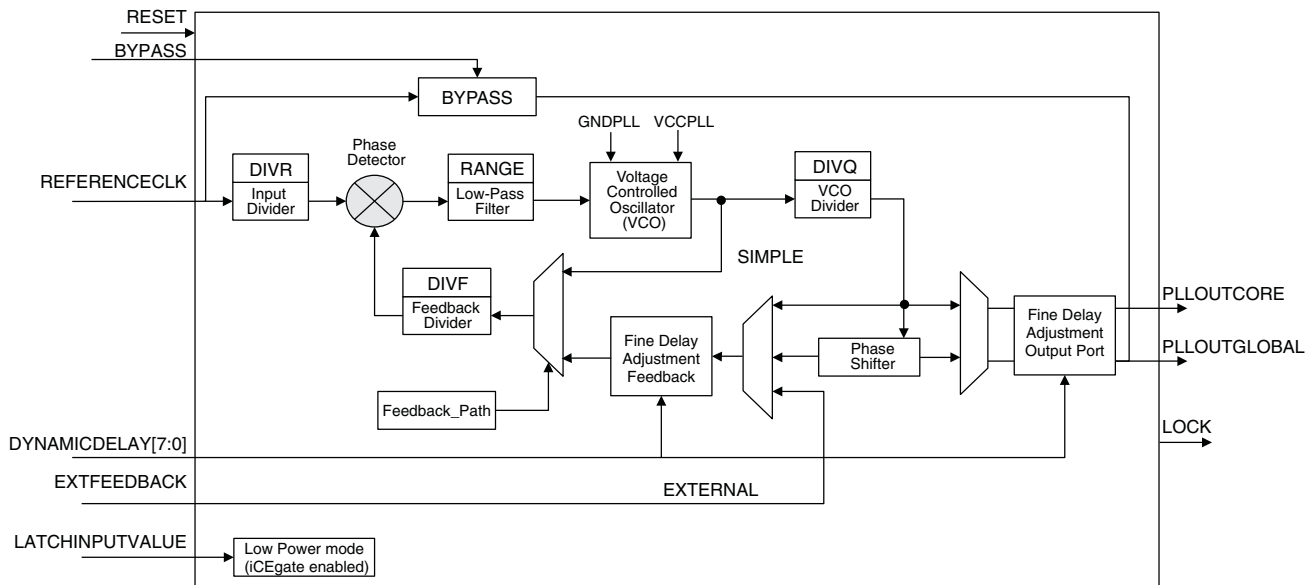


Table 2-3 provides signal descriptions of the PLL block.



**Table 2-3. PLL Signal Descriptions**

Signal Name	Direction	Description
REFERENCECLK	Input	Input reference clock
BYPASS	Input	When FEEDBACK_PATH is set to SIMPLE, the BYPASS control selects which clock signal connects to the PLLOUT output. 0 = PLL generated signal 1 = REFERENCECLK
EXTFEEDBACK	Input	External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL.
DYNAMICDELAY[3:0]	Input	Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC.
LATCHINPUTVALUE	Input	When enabled, forces the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable.
PLLOUTGLOBAL	Output	Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5.
PLLOUTCORE	Output	Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTGLOBAL port.
LOCK	Output	When High, indicates that the PLL output is phase aligned or locked to the input reference clock.
RESET	Input	Active low reset.

### sysMEM Embedded Block RAM Memory

Larger iCE40 device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering, and FIFO.

### sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as shown in Table 2-4.

**Table 2-4. sysMEM Block Configurations<sup>1</sup>**

Block RAM Configuration	Block RAM Configuration and Size	WADDR Port Size (Bits)	WDATA Port Size (Bits)	RADDR Port Size (Bits)	RDATA Port Size (Bits)	MASK Port Size (Bits)
SB_RAM256x16 SB_RAM256x16NR SB_RAM256x16NW SB_RAM256x16NRNW	256x16 (4K)	8 [7:0]	16 [15:0]	8 [7:0]	16 [15:0]	16 [15:0]
SB_RAM512x8 SB_RAM512x8NR SB_RAM512x8NW SB_RAM512x8NRNW	512x8 (4K)	9 [8:0]	8 [7:0]	9 [8:0]	8 [7:0]	No Mask Port
SB_RAM1024x4 SB_RAM1024x4NR SB_RAM1024x4NW SB_RAM1024x4NRNW	1024x4 (4K)	10 [9:0]	4 [3:0]	10 [9:0]	4 [3:0]	No Mask Port
SB_RAM2048x2 SB_RAM2048x2NR SB_RAM2048x2NW SB_RAM2048x2NRNW	2048x2 (4K)	11 [10:0]	2 [1:0]	11 [10:0]	2 [1:0]	No Mask Port

1. For iCE40 EBR primitives with a negative-edged Read or Write clock, the base primitive name is appended with a 'N' and a 'R' or 'W' depending on the clock that is affected.

**RAM Initialization and ROM Operation**

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

Note the sysMEM Embedded Block RAM Memory address 0 cannot be initialized.

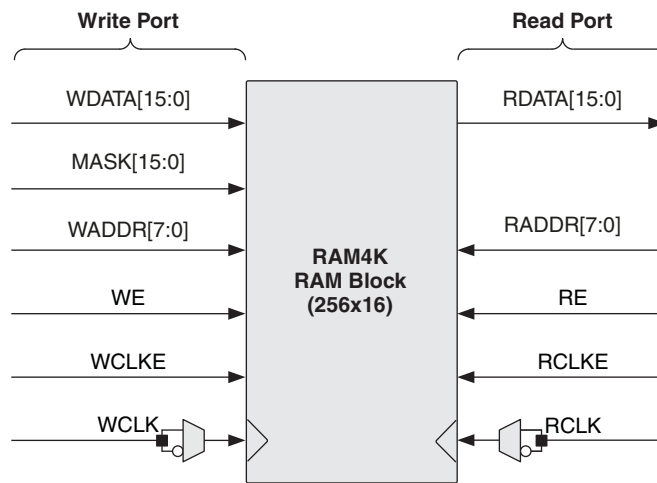
**Memory Cascading**

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

**RAM4k Block**

Figure 2-4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

**Figure 2-4. sysMEM Memory Primitives**



**Table 2-5. EBR Signal Descriptions**

Signal Name	Direction	Description
WDATA[15:0]	Input	Write Data input.
MASK[15:0]	Input	Masks write operations for individual data bit-lines. 0 = write bit; 1 = don't write bit
WADDR[7:0]	Input	Write Address input. Selects one of 256 possible RAM locations.
WE	Input	Write Enable input.
WCLKE	Input	Write Clock Enable input.
WCLK	Input	Write Clock input. Default rising-edge, but with falling-edge option.
RDATA[15:0]	Output	Read Data output.
RADDR[7:0]	Input	Read Address input. Selects one of 256 possible RAM locations.
RE	Input	Read Enable input.
RCLKE	Input	Read Clock Enable input.
RCLK	Input	Read Clock input. Default rising-edge, but with falling-edge option.

For further information on the sysMEM EBR block, please refer to TN1250, [Memory Usage Guide for iCE40 Devices](#).

## sysIO

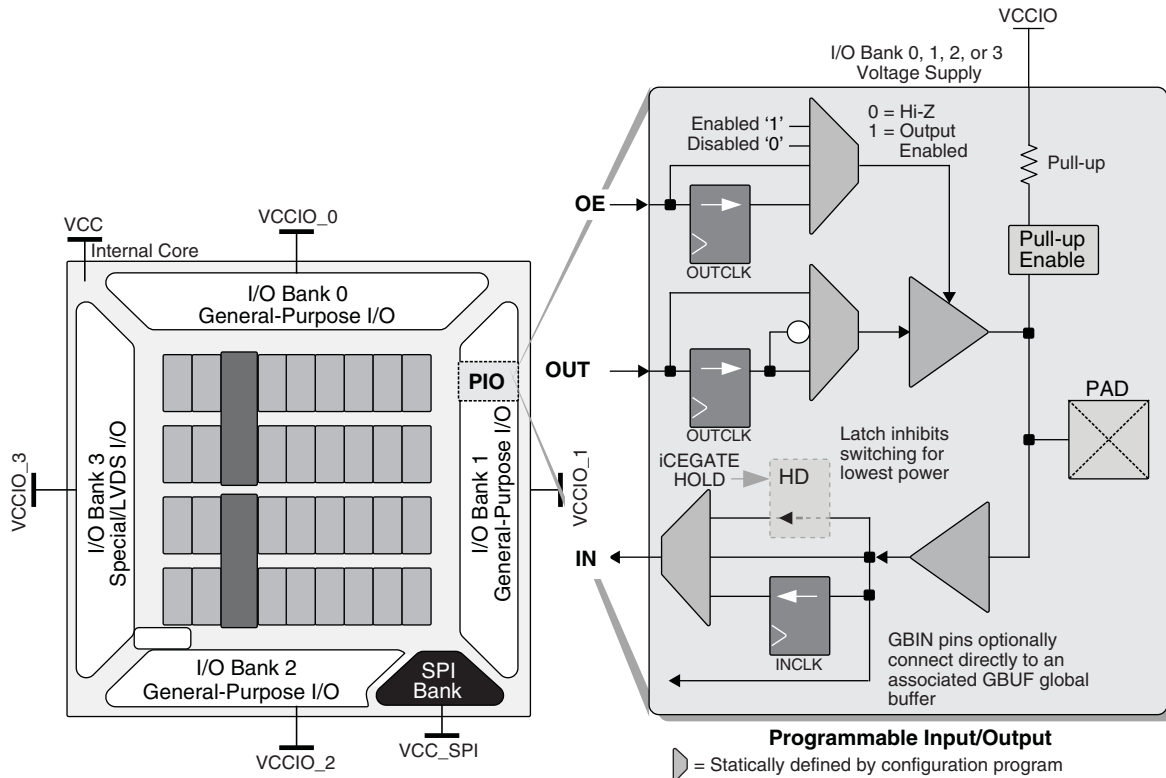
### Buffer Banks

iCE40 devices have up to four I/O banks with independent  $V_{CCIO}$  rails with an additional configuration bank  $V_{CC\_SPI}$  for the SPI I/Os.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysIO buffers and pads. The PIOs are placed on all four sides of the device.

**Figure 2-5. I/O Bank and Programmable I/O Cell**



The PIO contains three blocks: an input register block, output register block iCEgate™ and tri-state register block. To save power, the optional iCEgate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core. In Generic DDR mode, two registers are used to sample the data on the positive and negative edges of the system clock signal, creating two data streams.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers. In Generic DDR mode, two registers are used to capture the data on the positive and negative edge of the system clock and then muxed creating one data stream.

Figure 2-6 shows the input/output register block for the PIOs.

Figure 2-6. iCE I/O Register Block Diagram

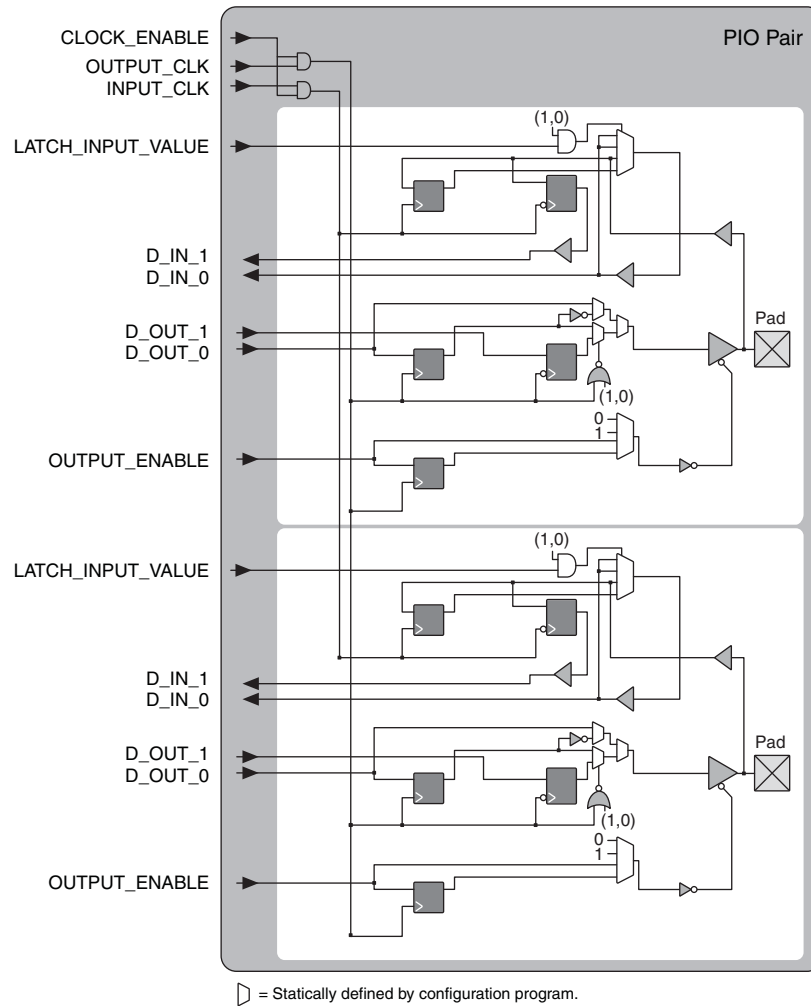


Table 2-6. PIO Signal List

Pin Name	I/O Type	Description
OUTPUT_CLK	Input	Output register clock
CLOCK_ENABLE	Input	Clock enable
INPUT_CLK	Input	Input register clock
OUTPUT_ENABLE	Input	Output enable
D_OUT_0/1	Input	Data from the core
D_IN_0/1	Output	Data to the core
LATCH_INPUT_VALUE	Input	Latches/holds the Input Value

### sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems including LVCMOS and LVDS25.

High Current LED Drivers combine three sysIO buffers together. This allows for programmable drive strength. This also allows for high current drivers that are ideal to drive three white LEDs, or one RGB LED. Each bank is capable of supporting multiple I/O standards including single-ended LVCMOS buffers and differential LVDS25E output buf-

fers. Bank 3 additionally supports differential LVDS25 input buffers. Each sysIO bank has its own dedicated power supply.

**Typical I/O Behavior During Power-up**

The internal power-on-reset (POR) signal is deactivated when  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  have reached the level defined in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. After the POR signal is deactivated, the FPGA core logic becomes active. It is the user's responsibility to ensure that all  $V_{CCIO}$  banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to  $V_{CCIO}$ . The I/O pins will maintain the pre-configuration state until  $V_{CC}$  and  $V_{CCIO}$  (for I/O banks containing configuration I/Os) have reached levels, at which time the I/Os will take on the software user-configured settings only after a proper download/configuration. Unused IOs are automatically blocked and the pullup termination is disabled.

**Supported Standards**

The iCE40 sysIO buffer supports both single-ended and differential input standards. The single-ended standard supported is LVC MOS. The buffer supports the LVC MOS 1.8, 2.5, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none). The High Current output buffer have individually configurable options for drive strength.

Table 2-7 and Table 2-8 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 devices.

**Table 2-7. Supported Input Standards**

Input Standard	$V_{CCIO}$ (Typical)		
	3.3 V	2.5 V	1.8 V
<b>Single-Ended Interfaces</b>			
LVC MOS33	Yes		
LVC MOS25		Yes	
LVC MOS18			Yes
<b>Differential Interfaces</b>			
LVDS25 <sup>1</sup>		Yes	
subLVDS <sup>1</sup>			Yes

1. Bank 3 only.

**Table 2-8. Supported Output Standards**

Output Standard	$V_{CCIO}$ (Typical)
<b>Single-Ended Interfaces</b>	
LVC MOS33	3.3
LVC MOS25	2.5
LVC MOS18	1.8
<b>Differential Interfaces</b>	
LVDS25E <sup>1</sup>	2.5
subLVDSSE <sup>1</sup>	1.8

1. These interfaces can be emulated with external resistors in all devices.

**Non-Volatile Configuration Memory**

All iCE40 devices provide a Non-Volatile Configuration Memory (NVCM) block which can be used to configure the device.

For more information on the NVCM, please refer to TN1248, [iCE40 Programming and Configuration Usage Guide](#).

## Power On Reset

iCE40 devices have power-on reset circuitry to monitor  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  voltage levels during power-up and operation. At power-up, the POR circuitry monitors  $V_{CC}$ ,  $V_{CCIO\_2}$ ,  $V_{PP\_2V5}$ , and  $V_{CC\_SPI}$  (controls configuration) voltage levels. It then triggers download from the on-chip NVCM or external Flash memory after reaching the power-up levels specified in the Power-On-Reset Voltage table in the DC and Switching Characteristics section of this data sheet. Before and during configuration, the I/Os are held in tri-state. I/Os are released to user functionality once the device has finished configuration.

## Programming and Configuration

This section describes the programming and configuration of the iCE40 family.

### Device Programming

The NVCM memory can be programmed through the SPI port.

### Device Configuration

There are various ways to configure the Configuration RAM (CRAM) including:

1. Internal NVCM Download
2. From a SPI Flash (Master SPI mode)
3. System microprocessor to drive a Serial Slave SPI port (SSPI mode)

The image to configure the CRAM can be selected by the user on power up (Cold Boot) or once powered up (Warm Boot).

For more details on programming and configuration, see TN1248, [iCE40 Programming and Configuration Usage Guide](#).

## Power Saving Options

iCE40 devices are available in two options for maximum flexibility: LP and HX devices. The LP devices have ultra low static and dynamic power consumption. HX devices are designed to provide high performance. Both the LP and the HX devices operate at 1.2 V  $V_{CC}$ .

iCE40 devices feature iCEGate and PLL low power mode to allow users to meet the static and dynamic power requirements of their applications. While these features are available in both device types, these features are mainly intended for use with iCE40 LP devices to manage power consumption.

**Table 2-9. iCE40 Power Saving Features Description**

Device Subsystem	Feature Description
PLL	When LATCHINPUTVALUE is enabled, forces the PLL into low-power mode; PLL output held static at last input clock value.
iCEGate	To save power, the optional iCEgate latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Registered inputs are effectively frozen by their associated clock or clock-enable control.

### Absolute Maximum Ratings<sup>1, 2, 3, 4</sup>

#### iCE40 LP/HX

Supply Voltage $V_{CC}$ . . . . .	-0.5 V to 1.42 V
Output Supply Voltage $V_{CCIO}$ , $V_{CC\_SPI}$ . . . . .	-0.5 V to 3.60 V
NVCM Supply Voltage $V_{PP\_2V5}$ . . . . .	-0.5 V to 3.60 V
PLL Supply Voltage $V_{CCPLL}$ . . . . .	-0.5 V to 1.30 V
I/O Tri-state Voltage Applied . . . . .	-0.5 V to 3.60 V
Dedicated Input Voltage Applied . . . . .	-0.5 V to 3.60 V
Storage Temperature (Ambient) . . . . .	-65 °C to 150 °C
Junction Temperature ( $T_J$ ) . . . . .	-55 °C to 125 °C

1. Stress above those listed under the “Absolute Maximum Ratings” may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.
2. Compliance with the Lattice [Thermal Management](#) document is required.
3. All voltages referenced to GND.
4. IOs can support a 200 mV Overshoot above the Recommend Operating Conditions  $V_{CCIO}$  (Max) and -200mV Undershoot below  $V_{IL}$  (Min). Overshoot and Undershoot is permitted for 25% duty cycle but must not exceed 1.6 ns.

### Recommended Operating Conditions<sup>1</sup>

Symbol	Parameter	Min.	Max.	Units	
$V_{CC}$ <sup>1</sup>	Core Supply Voltage	1.14	1.26	V	
$V_{PP\_2V5}$	$V_{PP\_2V5}$ NVCM Programming and Operating Supply Voltage	Slave SPI Configuration	1.71	3.46	V
		Master SPI Configuration	2.30	3.46	V
		Configure from NVCM	2.30	3.46	V
		NVCM Programming	2.30	3.00	V
$V_{PP\_FAST}$ <sup>4</sup>	Optional fast NVCM programming supply. Leave unconnected.	N/A	N/A	V	
$V_{CCPLL}$ <sup>5,6</sup>	PLL Supply Voltage	1.14	1.26	V	
$V_{CCIO}$ <sup>1,2,3</sup>	I/O Driver Supply Voltage	$V_{CCIO0-3}$	1.71	3.46	V
		$V_{CC\_SPI}$	1.71	3.46	V
$t_{JIND}$	Junction Temperature Industrial Operation	-40	100	°C	
$t_{PROG}$	Junction Temperature NVCM Programming	10	30	°C	

1. Like power supplies must be tied together. For example, if  $V_{CCIO}$  and  $V_{CC\_SPI}$  are both the same voltage, they must also be the same supply.
2. See recommended voltages by I/O standard in subsequent table.
3.  $V_{CCIO}$  pins of unused I/O banks should be connected to the  $V_{CC}$  power supply on boards.
4.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO_0}$  ball externally.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

**Power Supply Ramp Rates<sup>1, 2</sup>**

Symbol	Parameter	Min.	Max.	Units	
$t_{RAMP}$	Power supply ramp rates for all power supplies.	All configuration modes. No power supply sequencing.	0.40	10	V/ms
		Configuring from Slave SPI. No power supply sequencing.	0.01	10	V/ms
		Configuring from NVCM. $V_{CC}$ and $V_{PP\_2V5}$ to be powered 0.25 ms before $V_{CC\_SPI}$ .	0.01	10	V/ms
		Configuring from MSPI. $V_{CC}$ and $V_{PP\_SPI}$ to be powered 0.25 ms before $V_{PP\_2V5}$ .	0.01	10	V/ms

1. Assumes monotonic ramp rates.

2. iCE40LP384 requires  $V_{CC}$  to be greater than 0.7V when  $V_{CCIO}$  and  $V_{CC\_SPI}$  are above GND.

**Power-On-Reset Voltage Levels<sup>1</sup>**

Symbol	Device	Parameter	Min.	Max.	Units	
$V_{PORUP}$	iCE40LP384	Power-On-Reset ramp-up trip point (band gap based circuit monitoring $V_{CC}$ , $V_{CCIO\_2}$ , $V_{CC\_SPI}$ and $V_{PP\_2V5}$ )	$V_{CC}$	0.67	0.99	V
			$V_{CCIO\_2}$	0.70	1.59	V
			$V_{CC\_SPI}$	0.70	1.59	V
			$V_{PP\_2V5}$	0.70	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-up trip point (band gap based circuit monitoring $V_{CC}$ , $V_{CCIO\_2}$ , $V_{CC\_SPI}$ and $V_{PP\_2V5}$ )	$V_{CC}$	0.55	0.75	V
			$V_{CCIO\_2}$	0.86	1.29	V
			$V_{CC\_SPI}$	0.86	1.29	V
			$V_{PP\_2V5}$	0.86	1.33	V
$V_{PORDN}$	iCE40LP384	Power-On-Reset ramp-down trip point (band gap based circuit monitoring $V_{CC}$ , $V_{CCIO\_2}$ , $V_{CC\_SPI}$ and $V_{PP\_2V5}$ )	$V_{CC}$	—	0.64	V
			$V_{CCIO\_2}$	—	1.59	V
			$V_{CC\_SPI}$	—	1.59	V
			$V_{PP\_2V5}$	—	1.59	V
	iCE40LP640, iCE40LP/HX1K, iCE40LP/HX4K, iCE40LP/HX8K	Power-On-Reset ramp-down trip point (band gap based circuit monitoring $V_{CC}$ , $V_{CCIO\_2}$ , $V_{CC\_SPI}$ and $V_{PP\_2V5}$ )	$V_{CC}$	—	0.75	V
			$V_{CCIO\_2}$	—	1.29	V
			$V_{CC\_SPI}$	—	1.29	V
			$V_{PP\_2V5}$	—	1.33	V

1. These POR trip points are only provided for guidance. Device operation is only characterized for power supply voltages specified under recommended operating conditions.

**ESD Performance**

Please refer to the [iCE40 Product Family Qualification Summary](#) for complete qualification data, including ESD performance.



## DC Electrical Characteristics

### Over Recommended Operating Conditions

Symbol	Parameter	Condition	Min.	Typ.	Max.	Units
$I_{IL}, I_{IH}^{1,3,4,5,6,7}$	Input or I/O Leakage	$0V < V_{IN} < V_{CCIO} + 0.2 V$	—	—	+/-10	$\mu A$
$C_1^{6,7}$	I/O Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = \text{Typ.}, V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
$C_2^{6,7}$	Global Input Buffer Capacitance <sup>2</sup>	$V_{CCIO} = 3.3 V, 2.5 V, 1.8 V$ $V_{CC} = \text{Typ.}, V_{IO} = 0 \text{ to } V_{CCIO} + 0.2 V$	—	6	—	pf
$V_{HYST}$	Input Hysteresis	$V_{CCIO} = 1.8 V, 2.5 V, 3.3 V$	—	200	—	mV
$I_{PU}^{6,7}$	Internal PIO Pull-up Current	$V_{CCIO} = 1.8 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-3	—	-31	$\mu A$
		$V_{CCIO} = 2.5 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-8	—	-72	$\mu A$
		$V_{CCIO} = 3.3 V, 0 < V_{IN} <= 0.65 V_{CCIO}$	-11	—	-128	$\mu A$

1. Input or I/O leakage current is measured with the pin configured as an input or as an I/O with the output driver tri-stated. It is not measured with the output driver active. Internal pull-up resistors are disabled.
2.  $T_J = 25^\circ C, f = 1.0 \text{ MHz}$ .
3. Please refer to  $V_{IL}$  and  $V_{IH}$  in the sysIO Single-Ended DC Electrical Characteristics table of this document.
4. Only applies to IOs in the SPI bank following configuration.
5. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .
6. High current IOs has three sysIO buffers connected together.
7. The iCE40LP640 and iCE40LP1K SWG16 package has CDONE and a sysIO buffer are connected together.

## Static Supply Current – LP Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^4$	Units
$I_{CC}$	Core Power Supply	iCE40LP384	21	$\mu A$
		iCE40LP640	100	$\mu A$
		iCE40LP1K	100	$\mu A$
		iCE40LP4K	250	$\mu A$
		iCE40LP8K	250	$\mu A$
$I_{CCPLL}^{5,6}$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	1.0	$\mu A$
$I_{CCIO}, I_{CC\_SPI}$	Bank Power Supply <sup>4</sup> $V_{CCIO} = 2.5 V$	All devices	3.5	$\mu A$

1. Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
2. Frequency = 0 MHz.
3.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
4. Does not include pull-up.
5. No PLL available on the iCE40LP384 and iCE40LP640 device.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

### Static Supply Current – HX Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^4$	Units
$I_{CC}$	Core Power Supply	iCE40HX1K	296	$\mu A$
		iCE40HX4K	1140	$\mu A$
		iCE40HX8K	1140	$\mu A$
$I_{CCPLL}^5$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	1.0	$\mu A$
$I_{CCIO}, I_{CC\_SPI}$	Bank Power Supply <sup>4</sup> $V_{CCIO} = 2.5 V$	All devices	3.5	$\mu A$

- Assumes blank pattern with the following characteristics: all outputs are tri-stated, all inputs are configured as LVCMOS and held at  $V_{CCIO}$  or GND, on-chip PLL is off. For more detail with your specific design, use the Power Calculator tool. Power specified with master SPI configuration mode. Other modes may be up to 25% higher.
- Frequency = 0 MHz.
- $T_J = 25^\circ C$ , power supplies at nominal voltage.
- Does not include pull-up.
- $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

### Programming NVCM Supply Current – LP Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^5$	Units
$I_{CC}$	Core Power Supply	iCE40LP384	60	$\mu A$
		iCE40LP640	120	$\mu A$
		iCE40LP1K	120	$\mu A$
		iCE40LP4K	350	$\mu A$
		iCE40LP8K	350	$\mu A$
$I_{CCPLL}^{6,7}$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	2.5	mA
$I_{CCIO}^8, I_{CC\_SPI}$	Bank Power Supply <sup>5</sup>	All devices	3.5	mA

- Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
- Typical user pattern.
- SPI programming is at 8 MHz.
- $T_J = 25^\circ C$ , power supplies at nominal voltage.
- Per bank.  $V_{CCIO} = 2.5 V$ . Does not include pull-up.
- No PLL available on the iCE40-LP384 and iCE40-LP640 device.
- $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
- $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.

### Programming NVCM Supply Current – HX Devices<sup>1, 2, 3, 4</sup>

Symbol	Parameter	Device	Typ. $V_{CC}^5$	Units
$I_{CC}$	Core Power Supply	iCE40HX1K	278	$\mu A$
		iCE40HX4K	1174	$\mu A$
		iCE40HX8K	1174	$\mu A$
$I_{CCPLL}^6$	PLL Power Supply	All devices	0.5	$\mu A$
$I_{PP\_2V5}$	NVCM Power Supply	All devices	2.5	mA
$I_{CCIO}^7, I_{CC\_SPI}$	Bank Power Supply <sup>5</sup>	All devices	3.5	mA

1. Assumes all inputs are held at  $V_{CCIO}$  or GND and all outputs are tri-stated.
2. Typical user pattern.
3. SPI programming is at 8 MHz.
4.  $T_J = 25^\circ C$ , power supplies at nominal voltage.
5. Per bank.  $V_{CCIO} = 2.5 V$ . Does not include pull-up.
6.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
7.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications.

### Peak Startup Supply Current – LP Devices

Symbol	Parameter	Device	Max	Units
$I_{CCPEAK}$	Core Power Supply	iCE40LP384	7.7	mA
		iCELP640	6.4	mA
		iCE40LP1K	6.4	mA
		iCE40LP4K	15.7	mA
		iCE40LP8K	15.7	mA
$I_{CCPLLPEAK}^{1, 2, 4}$	PLL Power Supply	iCE40LP1K	1.5	mA
		iCELP640	1.5	mA
		iCE40LP4K	8.0	mA
		iCE40LP8K	8.0	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40LP384	3.0	mA
		iCELP640	7.7	mA
		iCE40LP1K	7.7	mA
		iCE40LP4K	4.2	mA
		iCE40LP8K	4.2	mA
$I_{PP\_FASTPEAK}^3$	NVCM Programming Supply	iCE40LP384	5.7	mA
		iCELP640	8.1	mA
		iCE40LP1K	8.1	mA
$I_{CCIOPEAK}^5, I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40LP384	8.4	mA
		iCELP640	3.3	mA
		iCE40LP1K	3.3	mA
		iCE40LP4K	8.2	mA
		iCE40LP8K	8.2	mA

1. No PLL available on the iCE40LP384 and iCE40LP640 device.
2.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.
3.  $V_{PP\_FAST}$ , used only for fast production programming, must be left floating or unconnected in applications, except CM36 and CM49 packages MUST have the  $V_{PP\_FAST}$  ball connected to  $V_{CCIO\_0}$  ball externally.
4. While no PLL is available in the iCE40-LP640 the  $I_{CCPLLPEAK}$  is additive to  $I_{CCPEAK}$ .
5. iCE40LP384 requires  $V_{CC}$  to be greater than 0.7 V when  $V_{CCIO}$  and  $V_{CC\_SPI}$  are above GND.

### Peak Startup Supply Current – HX Devices

Symbol	Parameter	Device	Max	Units
$I_{CCPEAK}$	Core Power Supply	iCE40HX1K	6.9	mA
		iCE40HX4K	22.3	mA
		iCE40HX8K	22.3	mA
$I_{CCPLLPEAK}^1$	PLL Power Supply	iCE40HX1K	1.8	mA
		iCE40HX4K	6.4	mA
		iCE40HX8K	6.4	mA
$I_{PP\_2V5PEAK}$	NVCM Power Supply	iCE40HX1K	2.8	mA
		iCE40HX4K	4.1	mA
		iCE40HX8K	4.1	mA
$I_{CCIOPEAK}, I_{CC\_SPIPEAK}$	Bank Power Supply	iCE40HX1K	6.8	mA
		iCE40HX4K	6.8	mA
		iCE40HX8K	6.8	mA

1.  $V_{CCPLL}$  is tied to  $V_{CC}$  internally in packages without PLLs pins.

### sysIO Recommended Operating Conditions

Standard	$V_{CCIO}$ (V)		
	Min.	Typ.	Max.
LVC MOS 3.3	3.14	3.3	3.46
LVC MOS 2.5	2.37	2.5	2.62
LVC MOS 1.8	1.71	1.8	1.89
LVDS25E <sup>1,2</sup>	2.37	2.5	2.62
subLV DSE <sup>1,2</sup>	1.71	1.8	1.89

1. Inputs on-chip. Outputs are implemented with the addition of external resistors.

2. Does not apply to Configuration Bank  $V_{CC\_SPI}$ .

### sysIO Single-Ended DC Electrical Characteristics

Input/ Output Standard	$V_{IL}$		$V_{IH}^1$		$V_{OL}$ Max. (V)	$V_{OH}$ Min. (V)	$I_{OL}$ Max. (mA)	$I_{OH}$ Max. (mA)
	Min. (V)	Max. (V)	Min. (V)	Max. (V)				
LVC MOS 3.3	-0.3	0.8	2.0	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	8, 16 <sup>2</sup> , 24 <sup>2</sup>	-8, -16 <sup>2</sup> , -24 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 2.5	-0.3	0.7	1.7	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	6, 12 <sup>2</sup> , 18 <sup>2</sup>	-6, -12 <sup>2</sup> , -18 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1
LVC MOS 1.8	-0.3	$0.35V_{CCIO}$	$0.65V_{CCIO}$	$V_{CCIO} + 0.2$ V	0.4	$V_{CCIO} - 0.4$	4, 8 <sup>2</sup> , 12 <sup>2</sup>	-4, -8 <sup>2</sup> , -12 <sup>2</sup>
					0.2	$V_{CCIO} - 0.2$	0.1	-0.1

1. Some products are clamped to a diode when  $V_{IN}$  is larger than  $V_{CCIO}$ .

2. Only for High Drive LED outputs.

## sysIO Differential Electrical Characteristics

The LVDS25E/subLVDSSE differential output buffers are available on all banks but the LVDS/subLVDS input buffers are only available on Bank 3 of iCE40 devices.

### LVDS25

#### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}, V_{INM}$	Input Voltage	$V_{CCIO}^1 = 2.5$	0	—	2.5	V
$V_{THD}$	Differential Input Threshold		250	350	450	mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO}^1 = 2.5$	$(V_{CCIO}/2) - 0.3$	$V_{CCIO}/2$	$(V_{CCIO}/2) + 0.3$	V
$I_{IN}$	Input Current	Power on	—	—	$\pm 10$	$\mu A$

1. Typical.

### subLVDS

#### Over Recommended Operating Conditions

Parameter Symbol	Parameter Description	Test Conditions	Min.	Typ.	Max.	Units
$V_{INP}, V_{INM}$	Input Voltage	$V_{CCIO}^1 = 1.8$	0	—	1.8	V
$V_{THD}$	Differential Input Threshold		100	150	200	mV
$V_{CM}$	Input Common Mode Voltage	$V_{CCIO}^1 = 1.8$	$(V_{CCIO}/2) - 0.25$	$V_{CCIO}/2$	$(V_{CCIO}/2) + 0.25$	V
$I_{IN}$	Input Current	Power on	—	—	$\pm 10$	$\mu A$

1. Typical.

## LVDS25E Emulation

iCE40 devices can support LVDS outputs via emulation on all banks. The output is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all devices. The scheme shown in Figure 3-1 is one possible solution for LVDS25E standard implementation. Resistor values in Figure 3-1 are industry standard values for 1% resistors.

Figure 3-1. LVDS25E Using External Resistors

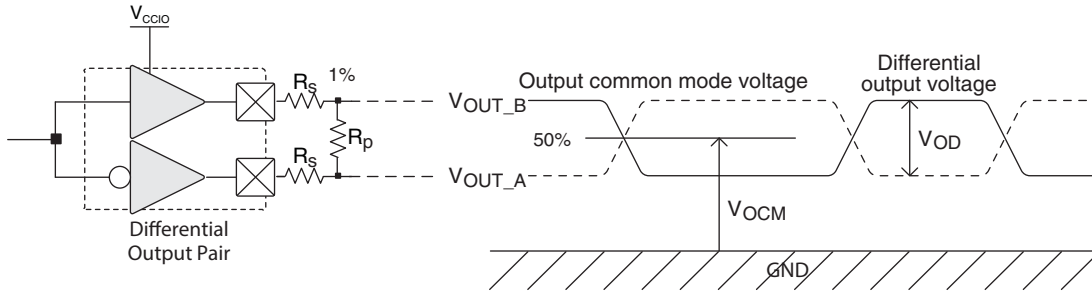


Table 3-1. LVDS25E DC Conditions

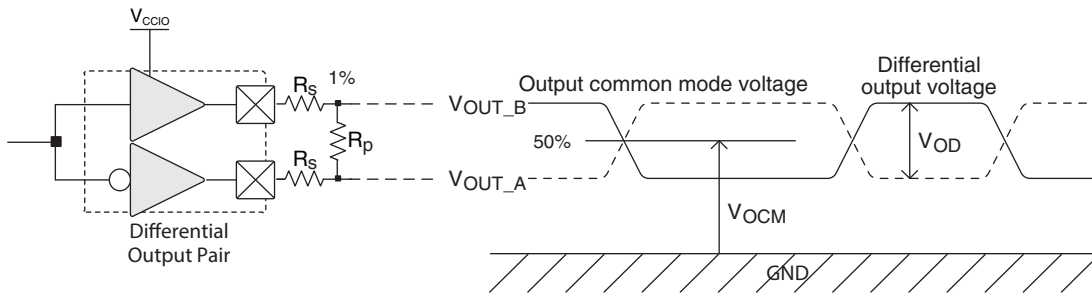
### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	150	Ohms
$R_P$	Driver parallel resistor	140	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.30	V
$V_{CM}$	Output common mode voltage	1.25	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	6.03	mA

## SubLVDS Emulation

The iCE40 family supports the differential subLVDS standard. The output standard is emulated using complementary LVCMOS outputs in conjunction with resistors across the driver outputs on all banks of the devices. The subLVDS input standard is supported by the LVDS25 differential input buffer. The scheme shown in Figure 3-2 is one possible solution for subLVDS output standard implementation. Use LVDS25E mode with suggested resistors for subLVDS operation. Resistor values in Figure 3-2 are industry standard values for 1% resistors.

**Figure 3-2. subLVDS**



**Table 3-2. subLVDS DC Conditions**

### Over Recommended Operating Conditions

Parameter	Description	Typ.	Units
$Z_{OUT}$	Output impedance	20	Ohms
$R_S$	Driver series resistor	270	Ohms
$R_P$	Driver parallel resistor	120	Ohms
$R_T$	Receiver termination	100	Ohms
$V_{OH}$	Output high voltage	1.43	V
$V_{OL}$	Output low voltage	1.07	V
$V_{OD}$	Output differential voltage	0.35	V
$V_{CM}$	Output common mode voltage	0.9	V
$Z_{BACK}$	Back impedance	100.5	Ohms
$I_{DC}$	DC output current	2.8	mA

## Typical Building Block Function Performance – LP Devices<sup>1, 2</sup>

### Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
<b>Basic Functions</b>		
16-bit decoder	11.0	ns
4:1 MUX	12.0	ns
16:1 MUX	13.0	ns

### Register-to-Register Performance

Function	Timing	Units
<b>Basic Functions</b>		
16:1 MUX	190	MHz
16-bit adder	160	MHz
16-bit counter	175	MHz
64-bit counter	65	MHz
<b>Embedded Memory Functions</b>		
256x16 Pseudo-Dual Port RAM	240	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a  $V_{CC}$  of 1.14 V at Junction Temp 85 °C.

## Typical Building Block Function Performance – HX Devices<sup>1, 2</sup>

### Pin-to-Pin Performance (LVCMOS25)

Function	Timing	Units
<b>Basic Functions</b>		
16-bit decoder	10.0	ns
4:1 MUX	9.0	ns
16:1 MUX	9.5	ns

### Register-to-Register Performance

Function	Timing	Units
<b>Basic Functions</b>		
16:1 MUX	305	MHz
16-bit adder	220	MHz
16-bit counter	255	MHz
64-bit counter	105	MHz
<b>Embedded Memory Functions</b>		
256x16 Pseudo-Dual Port RAM	403	MHz

1. The above timing numbers are generated using the iCECube2 design tool. Exact performance may vary with device and tool version. The tool uses internal parameters that have been characterized but are not tested on every device.
2. Using a  $V_{CC}$  of 1.14 V at Junction Temp 85 °C.



## Derating Logic Timing

Logic timing provided in the following sections of the data sheet and the Lattice design tools are worst case numbers in the operating range. Actual delays may be much faster. Lattice design tools can provide logic timing numbers at a particular temperature and voltage.

## Maximum sysIO Buffer Performance<sup>2</sup>

I/O Standard	Max. Speed	Units
<b>Inputs</b>		
LVDS25 <sup>1</sup>	400	MHz
subLVDS18 <sup>1</sup>	400	MHz
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	250	MHz
<b>Outputs</b>		
LVDS25E	250	MHz
subLVDS18E	155	MHz
LVC MOS33	250	MHz
LVC MOS25	250	MHz
LVC MOS18	155	MHz

1. Supported in Bank 3 only.
2. Measured with a toggling pattern

## iCE40 Family Timing Adders

Over Recommended Commercial Operating Conditions - LP Devices<sup>1, 2, 3, 4, 5</sup>

Buffer Type	Description	Timing	Units
<b>Input Adjusters</b>			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	-0.18	ns
subLVDS	subLVDS, $V_{CCIO} = 1.8\text{ V}$	0.82	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.18	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	0.19	ns
<b>Output Adjusters</b>			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
subLVDS E	subLVDS, Emulated, $V_{CCIO} = 1.8\text{ V}$	1.32	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	-0.12	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	1.32	ns

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.

**Over Recommended Commercial Operating Conditions - HX Devices<sup>1, 2, 3, 4, 5</sup>**

Buffer Type	Description	Timing	Units
<b>Input Adjusters</b>			
LVDS25	LVDS, $V_{CCIO} = 2.5\text{ V}$	0.13	ns
subLVDS	subLVDS, $V_{CCIO} = 1.8\text{ V}$	1.03	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.16	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	0.23	ns
<b>Output Adjusters</b>			
LVDS25E	LVDS, Emulated, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
subLVDS E	subLVDS, Emulated, $V_{CCIO} = 1.8\text{ V}$	1.76	ns
LVC MOS33	LVC MOS, $V_{CCIO} = 3.3\text{ V}$	0.17	ns
LVC MOS25	LVC MOS, $V_{CCIO} = 2.5\text{ V}$	0.00	ns
LVC MOS18	LVC MOS, $V_{CCIO} = 1.8\text{ V}$	1.76	ns

1. Timing adders are relative to LVC MOS25 and characterized but not tested on every device.
2. LVC MOS timing measured with the load specified in Switching Test Condition table.
3. All other standards tested according to the appropriate specifications.
4. Commercial timing numbers are shown.
5. Not all I/O standards are supported for all banks. See the Architecture section of this data sheet for details.