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# iCE40 UltraPlus™ Family

## Preliminary **Data Sheet**

DS1056 Version 1.3

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# Acronyms in This Document

A list of acronyms used in this document.

| Acronym | Definition |
|---|---|
| DFF | D-style Flip-Flop |
| DSP | Digital Signal Processor |
| EBR | Embedded Block RAM |
| HFOSC | High Frequency Oscillator |
| $I^2C$ | Inter-Integrated Circuit |
| LFOSC | Low Frequency Oscillator |
| LUT | Look Up Table |
| LVCMOS | Low-Voltage Complementary Metal Oxide Semiconductor |
| NVCM | Non Volatile Configuration Memory |
| PCLK | Primary Clock |
| PFU | Programmable Functional Unit |
| PIC | Programmable I/O Cells |
| PLB | Programmable Logic Blocks |
| PLL | Phase Locked Loops |
| SoC | System on a Chip |
| SPI | Serial Peripheral Interface |
| SPR | Single Port RAM |
| WLCSP | Wafer Level Chip Scale Packaging |

# 1. General Description

iCE40 UltraPlus family from Lattice Semiconductor is an ultra-low power FPGA and sensor manager designed for ultra-low power mobile applications, such as smartphones, tablets and hand-held devices. iCE40 UltraPlus is compatible with Lattice's iCE40 Ultra family devices, containing all the functions iCE40 Ultra family has except the high current IR LED driver. In addition, the iCE40 UltraPlus features an additional 1 Mb SRAM, additional DSP blocks, with additional LUTs, all which can be used to support an always-on Voice Recognition function in the mobile devices, without the need to keep the higher power consuming voice codec on all the time.

The iCE40 UltraPlus family includes integrated SPI and $I^2C$ blocks to interface with virtually all mobile sensors and application processors. In addition, the iCE40 UltraPlus family also features two I/O pins that can support the interface to I3C devices. There are two on-chip oscillators, 10 kHz and 48 MHz, the LFOSC (10 kHz) is ideal for low power function in always-on applications, while HFOSC (48 MHz) can be used for awaken activities.

The iCE40 UltraPlus family also features DSP functional block to off-load Application Processor to pre-process information sent from the mobile device, such as voice data. The RGB PWM IP, with the three 24 mA constant current RGB outputs on the iCE40 UltraPlus provides all the necessary logic to directly drive the service LED, without the need of external MOSFET or buffer.

The iCE40 UltraPlus family of devices are targeting for mobile applications to perform all the functions in iCE40 Ultra devices, such as Service LED, GPIO Expander, SDIO Level Shift, and other custom functions. In addition, the iCE40 UltraPlus family devices are also targeting for Voice Recognition application.

The iCE40 UltraPlus family features two device densities, 2800 to 5280 Look Up Tables (LUTs) of logic with programmable I/Os that can be used as either SPI/$I^2C$ interface ports or general purpose I/O's. Two of the iCE40 UltraPlus I/Os can be used to interface to higher performance I3C. It also has up to 120 kb of Block RAMs, plus 1024 kb of Single Port SRAMs to work with user logic.

## 1.1. Features

- Flexible Logic Architecture
  - Two devices with 2800 to 5280 LUTs
  - Offered in WLCS and QFN packages
- Ultra-low Power Devices
  - Advanced 40 nm low power process
  - As low as 100 µA standby current typical
- Embedded Memory
  - Up to 1024 kb Single Port SRAM
  - Up to 120 kb sysMEM™ Embedded Block RAM
- Two Hardened $I^2C$ Interfaces
  - Two I/O pins to support I3C interface
- Two Hardened SPI Interfaces
- Two On-Chip Oscillators
  - Low Frequency Oscillator – 10 kHz
  - High Frequency Oscillator – 48 MHz
- 24 mA Current Drive RGB LED Outputs
  - Three drive outputs in each device
  - User selectable sink current up to 24 mA
- On-chip DSP
  - Signed and unsigned 8-bit or 16-bit functions
  - Functions include Multiplier, Accumulator, and Multiply-Accumulate (MAC)
- Flexible On-Chip Clocking
  - Eight low skew global signal resource, six can be directly driven from external pins
  - One PLL with dynamic interface per device
- Flexible Device Configuration
  - SRAM is configured through:
    - Standard SPI Interface
    - Internal Nonvolatile Configuration Memory (NVCM)
- Ultra-Small Form Factor
  - As small as 2.15 mm × 2.55 mm
- Applications
  - Always-On Voice Recognition Application
  - Smartphones
  - Tablets and Consumer Handheld Devices
  - Handheld Commercial and Industrial Devices
  - Multi Sensor Management Applications
  - Sensor Pre-processing and Sensor Fusion
  - Always-On Sensor Applications
  - USB 3.1 Type C Cable Detect / Power Delivery Applications

# 2. Product Family

Table 2.1 lists device information and packages of the iCE40 UltraPlus family.

**Table 2.1. iCE40 UltraPlus Family Selection Guide**

| Part Number | iCE40UP3K | iCE40UP5K |
|---|---|---|
| **Logic Cells (LUT + Flip-Flop)** | **2800** | **5280** |
| EBR Memory Blocks | 20 | 30 |
| EBR Memory Bits (Kbits) | 80 | 120 |
| SPRAM Memory Blocks | 4 | 4 |
| SPRAM Memory Bits (Kbits) | 1024 | 1024 |
| NVCM | Yes | Yes |
| PLL | 1 | 1 |
| DSP Blocks (MULT16 with 32-bit Accumulator | 4 | 8 |
| Hardened $I^2C$, SPI | 2, 2 | 2, 2 |
| HF Oscillator (48 MHz) | 1 | 1 |
| LF Oscillator (10 KHz) | 1 | 1 |
| 24 mA LED Sink | 3 | 3 |
| PWM IP Block | Yes | Yes |
| **Packages, ball pitch, dimension** | **Total User I/O Count** | |
| 30-ball WLCSP, 0.4 mm, 2.15 mm x 2.55 mm | 21 | 21 |
| 48-ball QFN, 0.5 mm, 7.0 mm x 7.0 mm | - | 39 |

## 2.1. Overview

The iCE40 UltraPlus family of ultra-low power FPGAs has three devices with densities ranging from 2800 to 5280 Look-Up Tables (LUTs) fabricated in a 40 nm Low Power CMOS process. In addition to LUT-based, low-cost programmable logic, these devices also feature Embedded Block RAM (EBR), Single Port RAM (SPRAM), on-chip Oscillators (LFOSC, HFOSC), two hardened $I^2C$ Controllers, two hardened SPI Controllers, PWM IP, three 24 mA RGB LED open-drain drivers, I3C interface pins, and DSP blocks. These features allow the devices to be used in low-cost, high-volume consumer and mobile applications.

The iCE40 UltraPlus FPGAs are available in very small form factor packages, as small as 2.15 mm x 2.55 mm. The small form factor allows the device to easily fit into a lot of mobile applications, where space can be limited. Table 2.1 lists the LUT densities, package and I/O pin count.

The iCE40 UltraPlus devices offer I/O features such as pull-up resistors. Pull-up features are controllable on a “per pin” basis. In addition, the iCE40 UltraPlus devices offer two I/Os with dynamic control on the pull-up resistors to support I3C interface.

The RGB PWM IP in the iCE40 UltraPlus devices provides controls for driving the 24 mA LED Sink driver, including color controls, LED ON/OFF time, and breathe rate.

The iCE40 UltraPlus devices also provide flexible, reliable and secure configuration from on-chip NVCM. These devices can also configure themselves from external SPI Flash, or be configured by an external master such as a CPU.

Lattice provides a variety of design tools that allow complex designs to be efficiently implemented using the iCE40 UltraPlus family of devices. Popular logic synthesis tools provide synthesis library support for iCE40 UltraPlus. Lattice design tools use the synthesis tool output along with the user-specified preferences and constraints to place and route the design in the iCE40 UltraPlus device. These tools extract the timing from the routing and back-annotate it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules, including a number of reference designs, licensed free of charge, optimized for the iCE40 UltraPlus FPGA family. Lattice also can provide fully verified bitstream for some of the widely used target functions in mobile device applications, such as ultra-low power sensor management, gesture recognition, IR remote, barcode emulator functions. Users can use these functions as offered by

Lattice, or they can use the design to create their own unique required functions. For more information regarding Lattice's reference designs or fully-verified bitstreams, contact your local Lattice representative.

# 3. Architecture

## 3.1. Architecture Overview

The iCE40 UltraPlus family architecture contains an array of Programmable Logic Blocks (PLB), two Oscillator Generators, two user configurable $I^2C$ controllers, two user configurable SPI controllers, blocks of sysMEM™ Embedded Block RAM (EBR) and Single Port RAM (SPRAM) surrounded by Programmable I/O (PIO). Figure 3.1 shows the block diagram of the iCE40UP5K device.

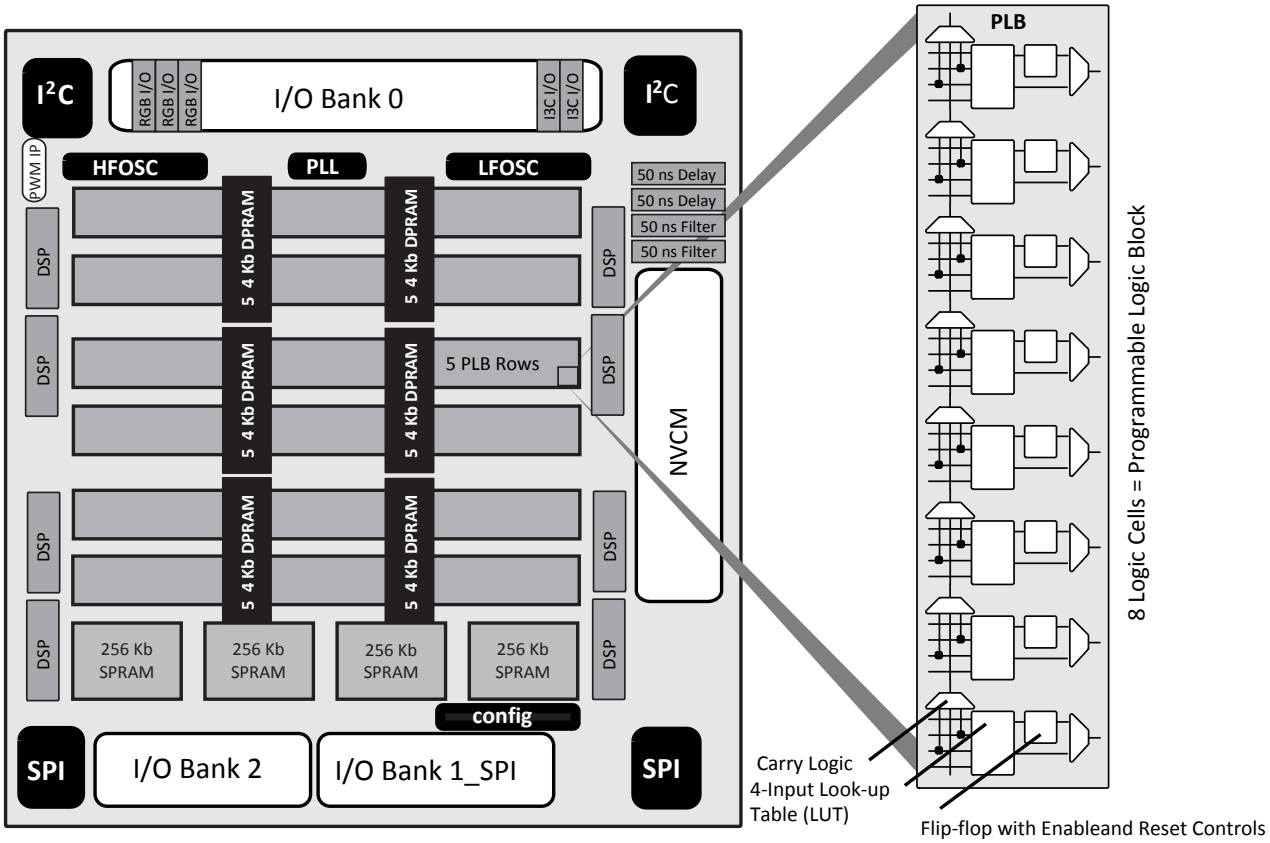


**Figure 3.1. iCE40UP5K Device, Top View**

The Programmable Logic Blocks (PLB) and sysMEM EBR blocks, are arranged in a two-dimensional grid with rows and columns. Each column has either PLB or EBR blocks. The PIO cells are located at the top and bottom of the device, arranged in banks. The PLB contains the building blocks for logic, arithmetic, and register functions. The PIOs utilize a flexible I/O buffer referred to as a sysIO buffer that supports operation with a variety of interface standards. The blocks are connected with many vertical and horizontal routing channel resources. The place and route software tool automatically allocates these routing resources.

In the iCE40 UltraPlus family, there are three sysIO banks, one on top and two at the bottom. User can connect some $V_{CCIO}$s together, if all the I/Os are using the same voltage standard. See the Power-up Supply Sequence section. The sysMEM EBRs are large 4 kb, dedicated fast memory blocks. These blocks can be configured as RAM, ROM or FIFO with user logic using PLBs.

In addition to the EBR, the iCE40 UltraPlus devices also feature four 256 kb SPRAM blocks that can be cascaded to create up to 1 Mb block. It is useful for temporary storage of large quantities of information.

Every device in the family has two user SPI ports, one of these (right side) SPI ports also supports programming and configuration of the device. The iCE40 UltraPlus also includes two user $I^2C$ ports, two oscillators, and high current RGB LED sink.

### 3.1.1. PLB Blocks

The core of the iCE40 UltraPlus device consists of Programmable Logic Blocks (PLB) which can be programmed to perform logic and arithmetic functions. Each PLB consists of eight interconnected Logic Cells (LC) as shown in Figure 3.2. Each LC contains one LUT and one register.

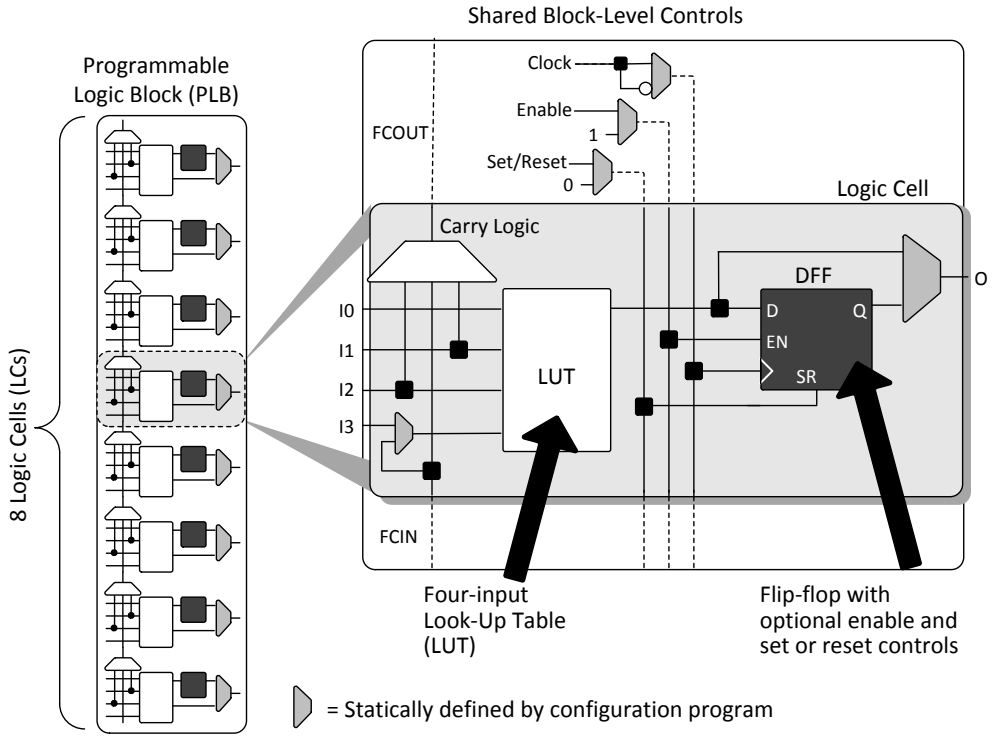


**Figure 3.2. PLB Block Diagram**

**Logic Cells**

Each Logic Cell includes three primary logic elements shown in Figure 3.2.

- A four-input Look-Up Table (LUT) builds any combinational logic function, of any complexity, requiring up to four inputs. Similarly, the LUT element behaves as a 16x1 Read-Only Memory (ROM). Combine and cascade multiple LUTs to create wider logic functions.
- A 'D'-style Flip-Flop (DFF), with an optional clock-enable and reset control input, builds sequential logic functions. Each DFF also connects to a global reset signal that is automatically asserted immediately following device configuration.
- Carry Logic boosts the logic efficiency and performance of arithmetic functions, including adders, subtracters, comparators, binary counters and some wide, cascaded logic functions.

Table 3.1 lists the logic cell signals.

**Table 3.1. Logic Cell Signal Descriptions**

| Function | Type | Signal Name | Description |
|---|---|---|---|
| Input | Data signal | I0, I1, I2, I3 | Inputs to LUT |
| Input | Control signal | Enable | Clock enable shared by all LCs in the PLB |
| Input | Control signal | Set/Reset* | Asynchronous or synchronous local set/reset shared by |
| Input | Control signal | Clock | Clock one of the eight Global Buffers, or from the |

| | | | |
|---|---|---|---|
| Input | Inter-PLB signal | FCIN | Fast carry in |
| Output | Data signals | O | LUT or registered output |
| Output | Inter-PFU signal | FCOUT | Fast carry out |

***Note**: If Set/Reset is not used, then the flip-flop is never set/reset, except when cleared immediately after configuration.

### 3.1.2. Routing

There are many resources provided in the iCE40 UltraPlus devices to route signals individually with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The inter-PLB connections are made with three different types of routing resources: Adjacent (spans two PLBs), x4 (spans five PLBs) and x12 (spans thirteen PLBs). The Adjacent, x4 and x12 connections provide fast and efficient connections in the diagonal, horizontal and vertical directions.

The design tool takes the output of the synthesis tool and places and routes the design.

### 3.1.3. Clock/Control Distribution Network

Each iCE40 UltraPlus device has six global inputs, two pins on the top bank and four pins on the bottom bank

These global inputs can be used as high fanout nets, clock, reset or enable signals. The dedicated global pins are identified as Gxx and each drives one of the eight global buffers. The global buffers are identified as GBUF[7:0]. These six inputs may be used as general purpose I/O if they are not used to drive the clock nets.

Table 3.2 lists the connections between a specific global buffer and the inputs on a PLB. All global buffers optionally connect to the PLB CLK input. Any four of the eight global buffers can drive logic inputs to a PLB. Even-numbered global buffers optionally drive the Set/Reset input to a PLB. Similarly, odd-numbered buffers optionally drive the PLB clock-enable input. GBUF[7:6, 3:0] can connect directly to G[7:6, 3:0] pins respectively. GBUF4 and GBUF5 can connect to the two on-chip Oscillator Generators (GBUF4 connects to LFOSC, GBUF5 connects to HFOSC).

**Table 3.2. Global Buffer (GBUF) Connections to Programmable Logic Blocks**

| Global Buffer | LUT Inputs | Clock | Reset | Clock Enable |
|---|---|---|---|---|
| GBUF0 | Yes, any 4 of 8 GBUF Inputs | ✓ | ✓ | — |
| GBUF1 | | ✓ | — | ✓ |
| GBUF2 | | ✓ | ✓ | — |
| GBUF3 | | ✓ | — | ✓ |
| GBUF4 | | ✓ | ✓ | — |
| GBUF5 | | ✓ | — | ✓ |
| GBUF6 | | ✓ | ✓ | — |
| GBUF7 | | ✓ | — | ✓ |

The maximum frequency for the global buffers are listed in Table 4.21.

#### Global Hi-Z Control

The global high-impedance control signal, GHIZ, connects to all I/O pins on the iCE40 UltraPlus device. This GHIZ signal is automatically asserted throughout the configuration process, forcing all user I/O pins into their high-impedance state.

#### Global Reset Control

The global reset control signal connects to all PLB and PIO flip-flops on the iCE40 UltraPlus device. The global reset signal is automatically asserted throughout the configuration process, forcing all flip-flops to their defined wake-up state. For PLB flip-flops, the wake-up state is always reset, regardless of the PLB flip-flop primitive used in the application.

### 3.1.4. sysCLOCK Phase Locked Loops (PLLs)

The sysCLOCK PLLs provide the ability to synthesize clock frequencies. The iCE40 UltraPlus devices have one sysCLOCK PLL. REFERENCECLK is the reference frequency input to the PLL and its source can come from an external I/O pin, the internal Oscillator Generators from internal routing. EXTFEEDBACK is the feedback signal to the PLL which can come from internal routing or an external I/O pin. The feedback divider is used to multiply the reference frequency and thus synthesize a higher frequency clock output.

The PLLOUT output has an output divider, thus allowing the PLL to generate different frequencies for each output. The output divider can have a value from 1 to 64 (in increments of 2X). The PLLOUT outputs can all be used to drive the iCE40 UltraPlus global clock network directly or general purpose routing resources can be used.

The LOCK signal is asserted when the PLL determines it has achieved lock and de-asserted if a loss of lock is detected. A block diagram of the PLL is shown in Figure 3.3.

The timing of the device registers can be optimized by programming a phase shift into the PLLOUT output clock which will advance or delay the output clock with reference to the REFERENCECLK clock. This phase shift can be either programmed during configuration or can be adjusted dynamically. In dynamic mode, the PLL may lose lock after a phase adjustment on the output used as the feedback source and not relock until the tLOCK parameter has been satisfied.

There is an additional feature in the iCE40 UltraPlus PLL. There are two FPGA controlled inputs, SCLK and SDI, that allows the user logic to serially shift in data thru SDI, clocked by SCLK clock. The data shifted in would change the configuration settings of the PLL. This feature allows the PLL to be time multiplexed for different functions, with different clock rates. After the data is shifted in, user would simply pulse the RESET input of the PLL block, and the PLL will re-lock with the new settings. For more details, refer to TN1251, iCE40 sysCLOCK PLL Design and Usage Guide.

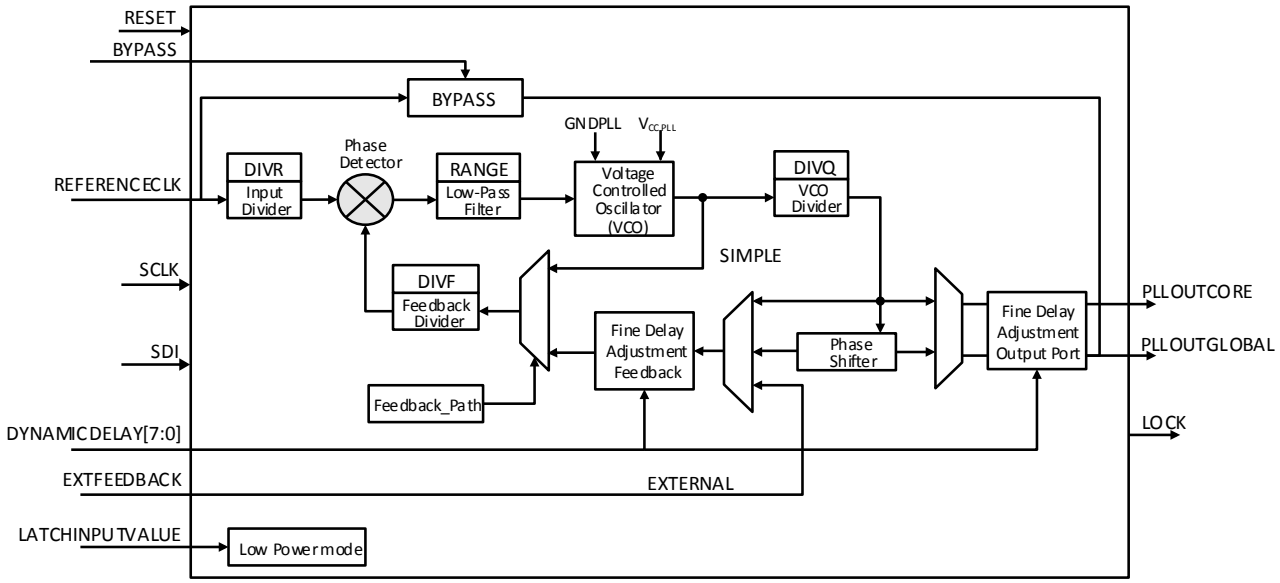


**Figure 3.3. PLL Diagram**

Table 3.3 provides signal descriptions of the PLL block.

**Table 3.3. PLL Signal Descriptions**

| Signal Name | Direction | Description |
|---|---|---|
| REFERENCECLK | Input | Input reference clock |
| BYPASS | Input | The BYPASS control selects which clock signal connects to the PLLOUT output.<br>0 – PLL generated signal<br>1 – REFERENCECLK |
| EXTFEEDBACK | Input | External feedback input to PLL. Enabled when the FEEDBACK_PATH attribute is set to EXTERNAL. |
| DYNAMICDELAY[7:0] | Input | Fine delay adjustment control inputs. Enabled when DELAY_ADJUSTMENT_MODE is set to DYNAMIC. |
| LATCHINPUTVALUE | Input | When enabled, puts the PLL into low-power mode; PLL output is held static at the last input clock value. Set ENABLE ICEGATE_PORTA and PORTB to '1' to enable. |
| PLLOUTGLOBAL | Output | Output from the Phase-Locked Loop (PLL). Drives a global clock network on the FPGA. The port has optimal connections to global clock buffers GBUF4 and GBUF5. |
| PLLOUTCORE | Output | Output clock generated by the PLL, drives regular FPGA routing. The frequency generated on this output is the same as the frequency of the clock signal generated on the PLLOUTLGOBAL port. |
| LOCK | Output | When High, indicates that the PLL output is phase aligned or locked to the input reference clock. |
| RESET | Input | Active low reset. |
| SCLK | Input | Input, Serial Clock used for re-programming PLL settings. |
| SDI | Input | Input, Serial Data used for re-programming PLL settings. |

### 3.1.5. sysMEM Embedded Block RAM Memory

Larger iCE40 UltraPlus device includes multiple high-speed synchronous sysMEM Embedded Block RAMs (EBRs), each 4 kbit in size. This memory can be used for a wide variety of purposes including data buffering and FIFO.

#### sysMEM Memory Block

The sysMEM block can implement single port, pseudo dual port, or FIFO memories with programmable logic resources. Each block can be used in a variety of depths and widths as listed in Table 3.4.

**Table 3.4. sysMEM Block Configurations**

| Block RAM Configuration | Block RAM Configuration and Size | WADDR Port Size (Bits) | WDATA Port Size (Bits) | RADDR Port Size (Bits) | RDATA Port Size (Bits) | MASK Port Size (Bits) |
|---|---|---|---|---|---|---|
| SB_RAM256x16<br>SB_RAM256x16NR<br>SB_RAM256x16NW<br>SB_RAM256x16NRNW | 256x16 (4 k) | 8 [7:0] | 16 [15:0] | 8 [7:0] | 16 [15:0] | 16 [15:0] |
| SB_RAM512x8<br>SB_RAM512x8NR<br>SB_RAM512x8NW<br>SB_RAM512x8NRNW | 512x8 (4 k) | 9 [8:0] | 8 [7:0] | 9 [8:0] | 8 [7:0] | No Mask Port |
| SB_RAM1024x4<br>SB_RAM1024x4NR<br>SB_RAM1024x4NW<br>SB_RAM1024x4NRNW | 1024x4 (4 k) | 10 [9:0] | 4 [3:0] | 10 [9:0] | 4 [3:0] | No Mask Port |
| SB_RAM2048x2<br>SB_RAM2048x2NR<br>SB_RAM2048x2NW<br>SB_RAM2048x2NRNW | 2048x2 (4 k) | 11 [10:0] | 2 [1:0] | 11 [10:0] | 2 [1:0] | No Mask Port |

**Note**: For iCE40 UltraPlus, the primitive name without "Nxx" uses rising-edge Read and Write clocks. "NR" uses rising-edge Write clock and falling-edge Read clock. "NW" uses falling-edge Write clock and rising-edge Read clock. "NRNW" uses failing-edge clocks on both Read and Write.

### RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration.

By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

### Memory Cascading

Larger and deeper blocks of RAM can be created using multiple EBR sysMEM Blocks.

### RAM4k Block

Figure 3.4 shows the 256x16 memory configurations and their input/output names. In all the sysMEM RAM modes, the input data and addresses for the ports are registered at the input of the memory array.

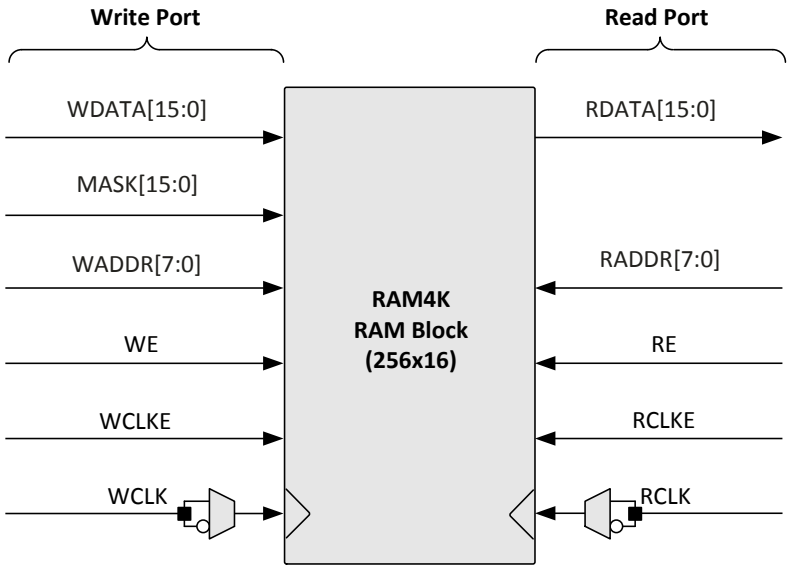


**Figure 3.4. sysMEM Memory Primitives**

Table 3.5 lists the EBR signals.

**Table 3.5. EBR Signal Descriptions**

| Signal Name | Direction | Description |
|---|---|---|
| WDATA[15:0] | Input | Write Data input. |
| MASK[15:0] | Input | Masks write operations for individual data bit-lines.<br>0 – Write bit<br>1 – Do not write bit |
| WADDR[7:0] | Input | Write Address input. Selects one of 256 possible RAM locations. |
| WE | Input | Write Enable input. |
| WCLKE | Input | Write Clock Enable input. |
| WCLK | Input | Write Clock input. Default rising-edge, but with falling-edge option. |
| RDATA[15:0] | Output | Read Data output. |
| RADDR[7:0] | Input | Read Address input. Selects one of 256 possible RAM locations. |
| RE | Input | Read Enable input. |
| RCLKE | Input | Read Clock Enable input. |

| | | |
|---|---|---|
| RCLK | Input | Read Clock input. Default rising-edge, but with falling-edge option. |

For further information on the sysMEM EBR block, refer to TN1250, Memory Usage Guide for iCE40 Devices.

### 3.1.6. sysMEM Single Port RAM Memory (SPRAM)

The SPRAM block is implemented to be accessed only as single port. Each block of SPRAM is designed to be 16K x 16 (256 kbits) in size. See Figure 3.5.

#### SPRAM Data Width

The SPRAM is designed with fixed 16-bit data width. However, the block contains nibble mask control on the write input that allows the user logic to operate the SPRAM as x4 or x8 with this control on the write side, and user logic to select which nible/byte in the read side.

#### SPRAM Initialization and ROM Operation

There is no pre-load into the SPRAM during device configuration, therefore, the SPRAM is not initialized after configuration.

#### SPRAM Cascading

Deeper SPRAM can be created using multiple SPRAM blocks, up to four blocks (64K x 16)

#### SPRAM Power Modes

There are three power modes in the SPRAM that the users can select during normal operation. This reduces the SPRAM block power when it Is not needed, allow lower power consumption in an always-on application. These modes are:

- **Standby Mode**: SPRAM stops all activity, and SPRAM freezes in its current state. Memory contents are retained, memory outputs are retained, and all register contents are retained.
- **Sleep Mode**: SPRAM block is shut down on all peripheral circuit, except the memory core. Memory contents are retained, memory outputs and register contents are clear and become unknown.
- **Power Off Mode**: Power source to the SPRAM is disconnected. This is the lowest power state. Memory contents are lost. Memory outputs are unknown.

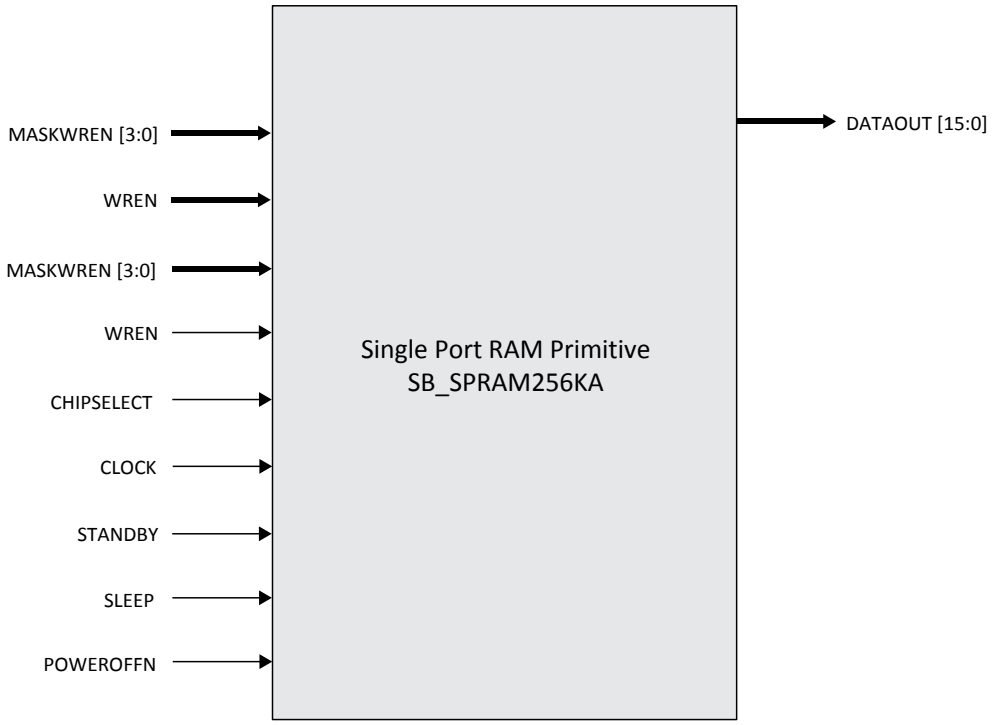


**Figure 3.5. SPRAM Primitive**

**Table 3.6. SPRAM Signal Descriptions**

| Signal Name | Direction | Description |
|---|---|---|
| ADDRESS[13:0] | Input | Address input |
| DATAIN[15:0] | Input | Write Data input |
| MASKWREN[3:0] | Input | Nibble WE control |
| WREN | Input | Write Enable |
| CHIPSELECT | Input | Enable SPRAM |
| CLOCK | Input | Clock input |
| STANDY | Input | Standby Mode |
| SLEEP | Input | Sleep Mode |
| POWEROFF | Input | Switch off power source to SPRAM |
| DATAOUT[15:0] | Output | Output Data |

For further information on sysMEM SPRAM block, refer to TN1314, iCE40 SPRAM Usage Guide.

### 3.1.7. sysDSP

The iCE40 UltraPlus family provides an efficient sysDSP architecture that is very suitable for low-cost Digital Signal Processing (DSP) functions for mobile applications. Typical functions used in these applications are Multiply, Accumulate, and Multiply-Accumulate. The block can also be used for simple Add and Subtract functions.

#### iCE40 UltraPlus sysDSP Architecture Features

The iCE40 UltraPlus sysDSP supports many functions that include the following:

- Single 16-bit x 16-bit Multiplier, or two independent 8-bit x 8-bit Multipliers
- Optional independent pipeline control on Input Register, Output Register, and Intermediate Reg faster clock performance
- Single 32-bit Accumulator, or two independent 16-bit Accumulators
- Single 32-bit, or two independent 16-bit Adder/Subtracter functions, registered or asynchronous
- Cascadable to create wider Accumulator blocks

Figure 3.6 shows the block diagram of the sysDSP block. The block consists of the Multiplier section with a bypassable Output register, Input Register, and Intermediate register between Multiplier and AC timing to achieve the highest performance.

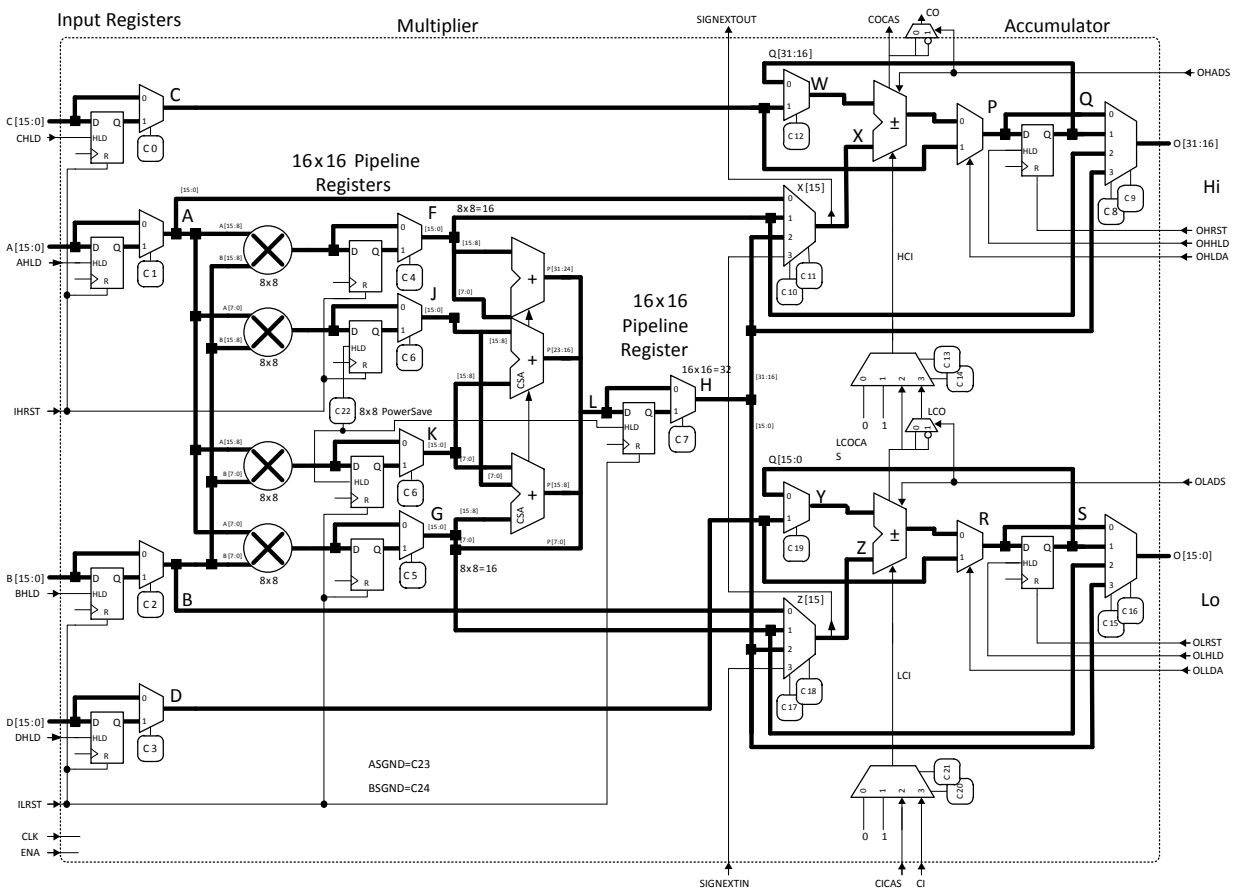


**Figure 3.6. sysDSP Functional Block Diagram (16-bit x 16-bit Multiply-Accumulate)**

**Table 3.7. Output Block Port Description**

| Signal | Primitive Port Name | Width | Input/ Output | Function | Default |
|---|---|---|---|---|---|
| CLK | CLK | 1 | Input | Clock Input. Applies to all clocked elements in the sysDSP block | — |
| ENA | CE | 1 | Input | Clock Enable Input. Applies to all clocked elements in the sysDSP block.<br>0 – Not enabled<br>1 – Enabled | 0 – Enabled |
| A[15:0] | A[15:0] | 16 | Input | Input to the A Register. Feeds the Multiplier or is a direct input to the Adder Accumulator | 16'b0 |
| B[15:0] | B[15:0] | 16 | Input | Input to the B Register. Feeds the Multiplier or is a direct input to the Adder Accumulator | 16'b0 |
| C[15:0] | C[15:0] | 16 | Input | Input to the C Register. It is a direct input to the Adder Accumulator | 16'b0 |
| D[15:0] | D[15:0] | 16 | Input | Input to the D Register. It is a direct input to the Adder Accumulator | 16'b0 |
| AHLD | AHOLD | 1 | Input | A Register Hold.<br>0 – Update<br>1 – Hold | 0 – Update |

**Table 3.7. Output Block Port Description** *(Continued)*

| Signal | Primitive Port Name | Width | Input/ Output | Function | Default |
|---|---|---|---|---|---|
| BHLD | BHOLD | 1 | Input | B Register Hold.<br>0 – Update<br>1 – Hold | 0 – Update |
| CHLD | CHOLD | 1 | Input | C Register Hold.<br>0 – Update<br>1 – Hold | 0 – Update |
| DHLD | DHOLD | 1 | Input | D Register Hold.<br>0 – Update<br>1 – Hold | 0 – Update |
| IHRST | IRSTTOP | 1 | Input | Reset input to A and C input registers, and the pipeline registers in the upper half of the Multiplier Section.<br>0 – No reset<br>1 – Reset | 0 – No reset |
| ILRST | IRSTBOT | 1 | Input | Reset input to B and D input registers, and the pipeline registers in the lower half of the Multiplier Section. It also resets the Multiplier result pipeline register.<br>0 – No reset<br>1 – Reset | 0 – No reset |
| O[31:0] | O[31:0] | 32 | Output | Output of the sysDSP block. This output can be:<br>• O[31:0] – 32-bit result of 16x16 Multiplier or MAC<br>• O[31:16] – 16-bit result of 8x8 upper half Multiplier or MAC<br>• O[15:0] – 16-bit result of 8x8 lower half Multiplier or MAC | — |
| OHHLD | OHOLDTOP | 1 | Input | High-order (upper half) Accumulator Register Hold.<br>0 – Update<br>1 – Hold | 0 – Update |
| OHRST | ORSTTOP | 1 | Input | Reset input to high-order (upper half) bits of the Accumulator Register.<br>0 – No reset<br>1 – Reset | 0 – No reset |
| OHLDA | OLOADTOP | 1 | Input | High-order (upper half) Accumulator Register Accumulate/Load control.<br>0 – Accumulate, register is loaded with Adder/Subtracter results<br>1 – Load, register is loaded with Input C or C Register | 0 – Accumulate |
| OHADS | ADDSUBTOP | 1 | Input | High-order (upper half) Accumulator Add or Subtract select.<br>0 – Add<br>1 – Subtract | 0 – Add |
| OLHLD | OHOLDBOT | 1 | Input | Low-order (lower half) Accumulator Register Hold.<br>0 – Update<br>1 – Hold | 0 – Update |
| OLRST | ORSTBOT | 1 | Input | Reset input to Low-order (lower half) bits of the Accumulator Register.<br>0 –No reset<br>1 – Reset | 0 – No reset |

**Table 3.7. Output Block Port Description** *(Continued)*

| Signal | Primitive Port Name | Width | Input/ Output | Function | Default |
|---|---|---|---|---|---|
| OLLDA | OLOADBOT | 1 | Input | Low-order (lower half) Accumulator Register Accumulate/Load control.<br>0 – Accumulate, register is loaded with Adder/Subtracter results<br>1 – Load, register is loaded with Input C or C Register | 0 – Accumulate |
| OLADS | ADDSUBBOT | 1 | Input | Low-order (lower half) Accumulator Add or Subtract select.<br>0 – Add<br>1 – Subtract | 0 – Add |
| CICAS | ACCUMCI | 1 | Input | Cascade Carry/Borrow input from previous sysDSP block | — |
| CI | CI | 1 | Input | Carry/Borrow input from lower logic tile | — |
| COCAS | ACCUMCO | 1 | Output | Cascade Carry/Borrow output to next sysDSP block | — |
| CO | CO | 1 | Output | Carry/Borrow output to higher logic tile | — |
| SIGNEXTIN | SIGNEXTIN | 1 | Input | Sign extension input from previous sysDSP block | — |
| SIGNEXTOUT | SIGNEXTOUT | 1 | Output | Sing extension output to next sysDSP block | — |

The iCE40 UltraPlus sysDSP can support the following functions:

- 8-bit x 8-bit Multiplier
- 16-bit x 16-bit Multiplier
- 16-bit Adder/Subtracter
- 32-bit Adder/Subtracter
- 16-bit Accumulator
- 32-bit Accumulator
- 8-bit x 8-bit Multiply-Accumulate
- 16-bit x 16-bit Multiply-Accumulate

Figure 3.7 on the next page shows the path for an 8-bit x 8-bit Multiplier using the upper half of sysDSP block.

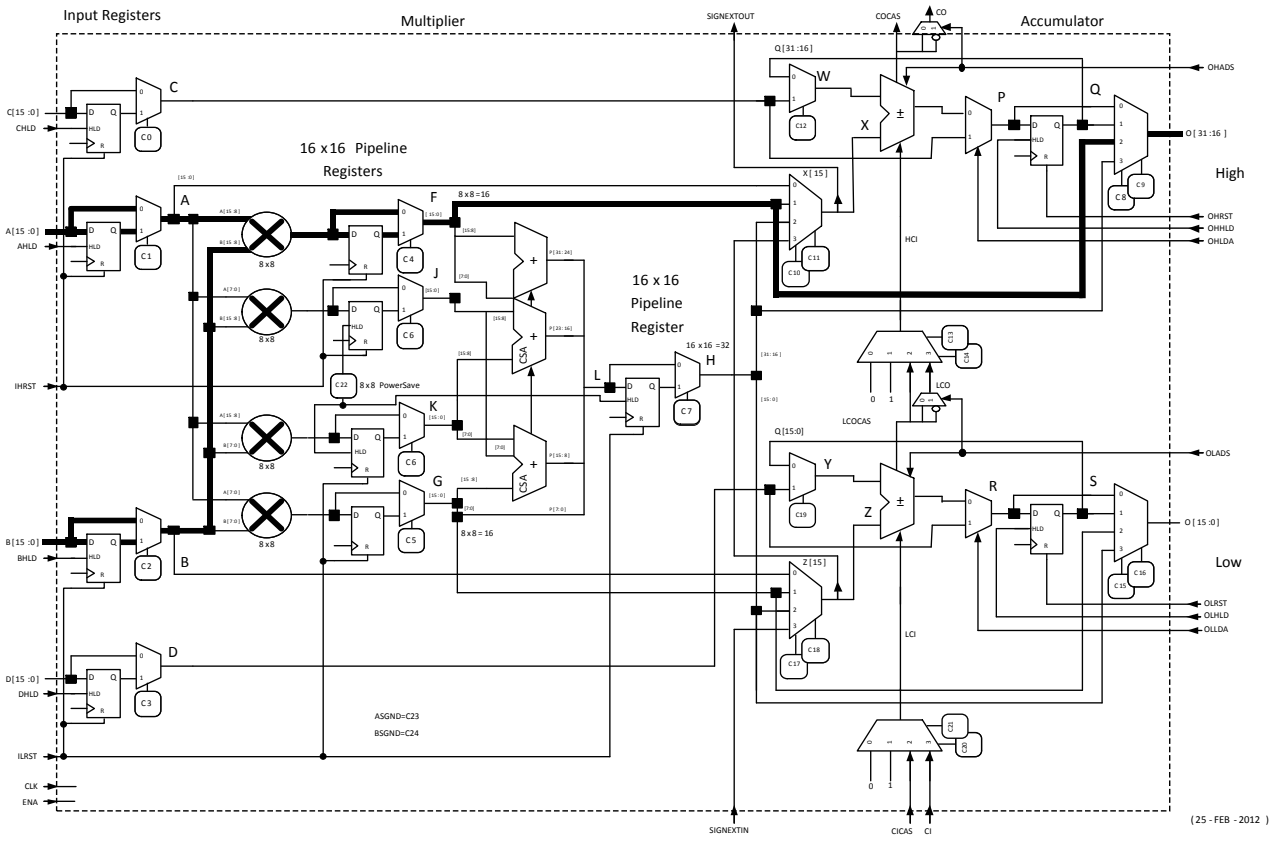


**Figure 3.7. sysDSP 8-bit x 8-bit Multiplier**

Figure 3.8 shows the path for an 16-bit x 16-bit Multiplier using the upper half of sysDSP block.

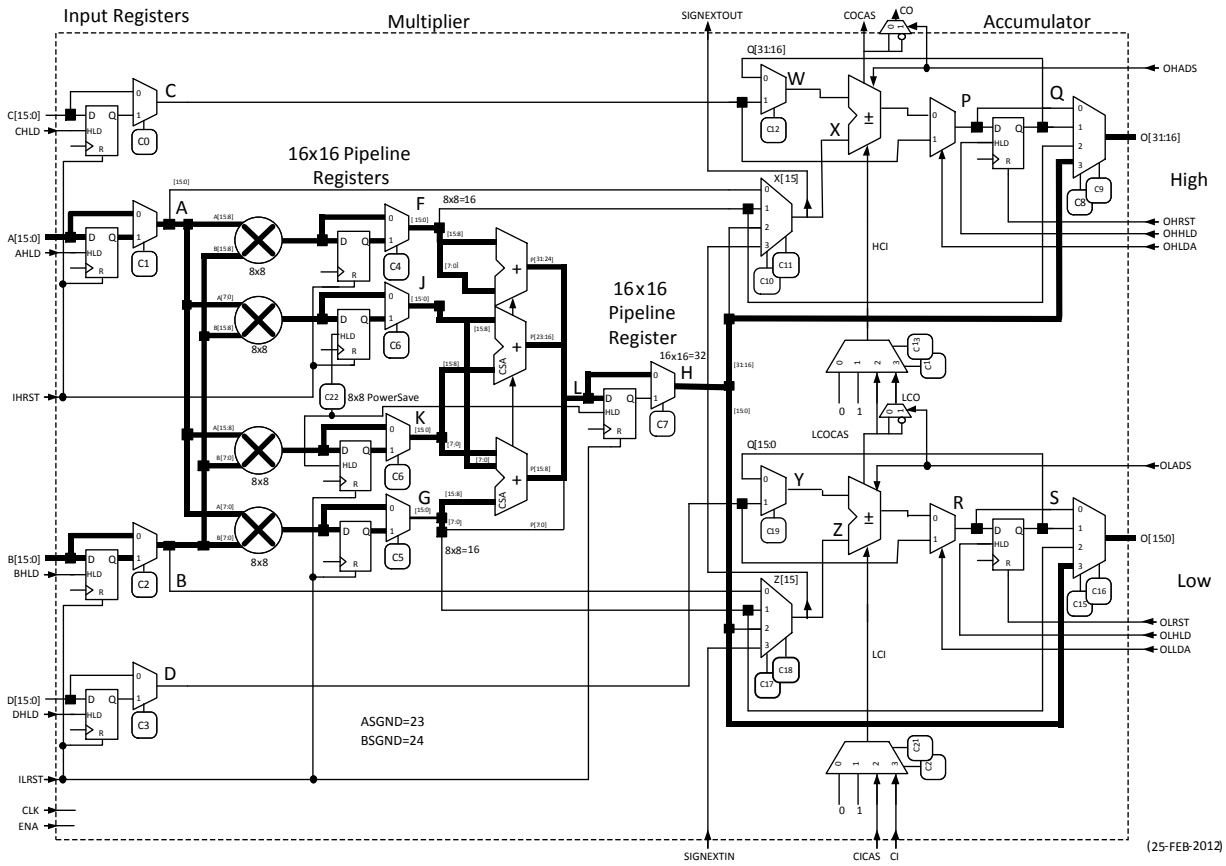


**Figure 3.8. DSP 16-bit x 16-bit Multiplier**

## 3.1.8. sysIO Buffer Banks

iCE40 UltraPlus devices have up to three I/O banks with independent $V_{CCIO}$ rails. The configuration SPI interface signals are powered by SPI_$V_{CCIO1}$. Please refer to the Pin Information Summary table.

### Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIOs are connected to their respective sysIO buffers and pads. The PIOs are placed on the top and bottom of the devices.

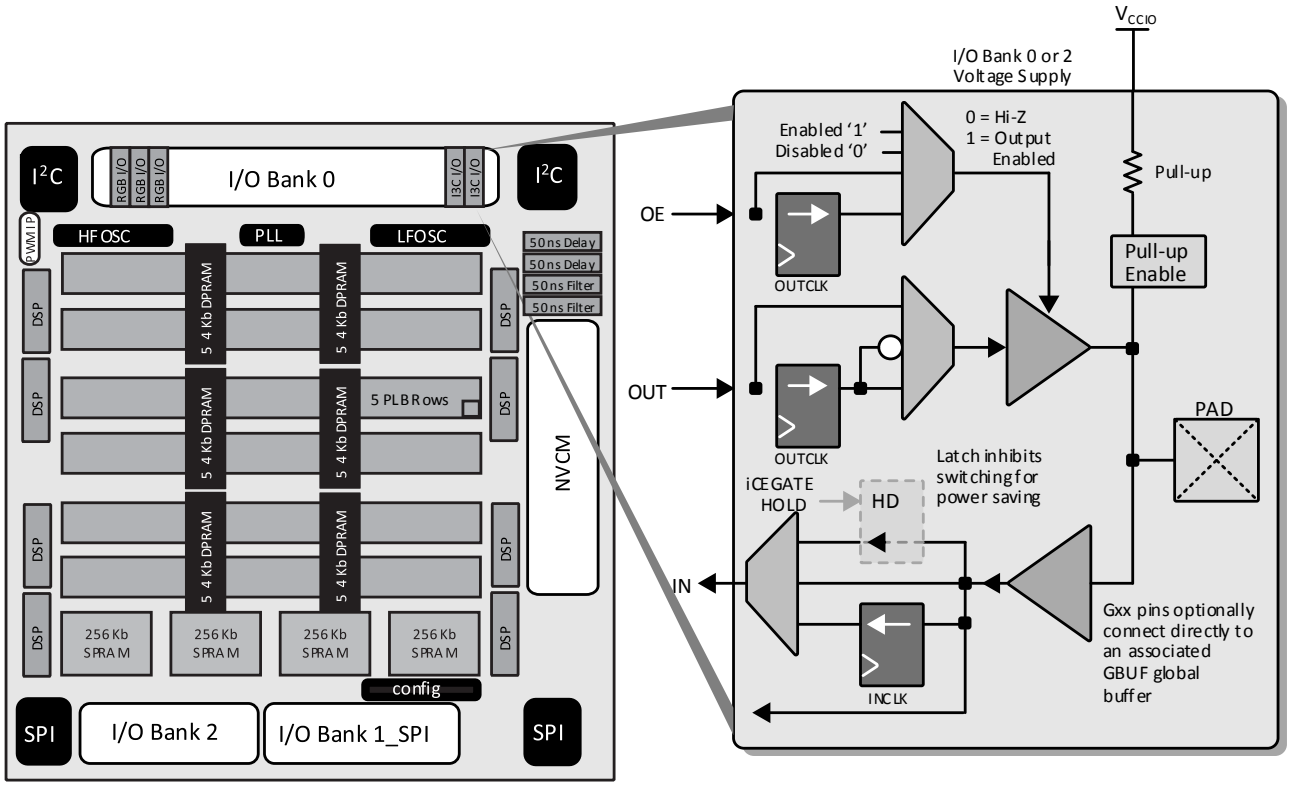


**Figure 3.9. I/O Bank and Programmable I/O Cell**

The PIO contains three blocks: an input register block, output register block iCEGate™ and tri-state register block. To save power, the optional iCEGate™ latch can selectively freeze the state of individual, non-registered inputs within an I/O bank. Note that the freeze signal is common to the bank. These blocks can operate in a variety of modes along with the necessary clock and selection logic.

### Input Register Block

The input register blocks for the PIOs on all edges contain registers that can be used to condition high-speed interface signals before they are passed to the device core.

### Output Register Block

The output register block can optionally register signals from the core of the device before they are passed to the sysIO buffers.

Figure 3.10 shows the input/output register block for the PIOs.

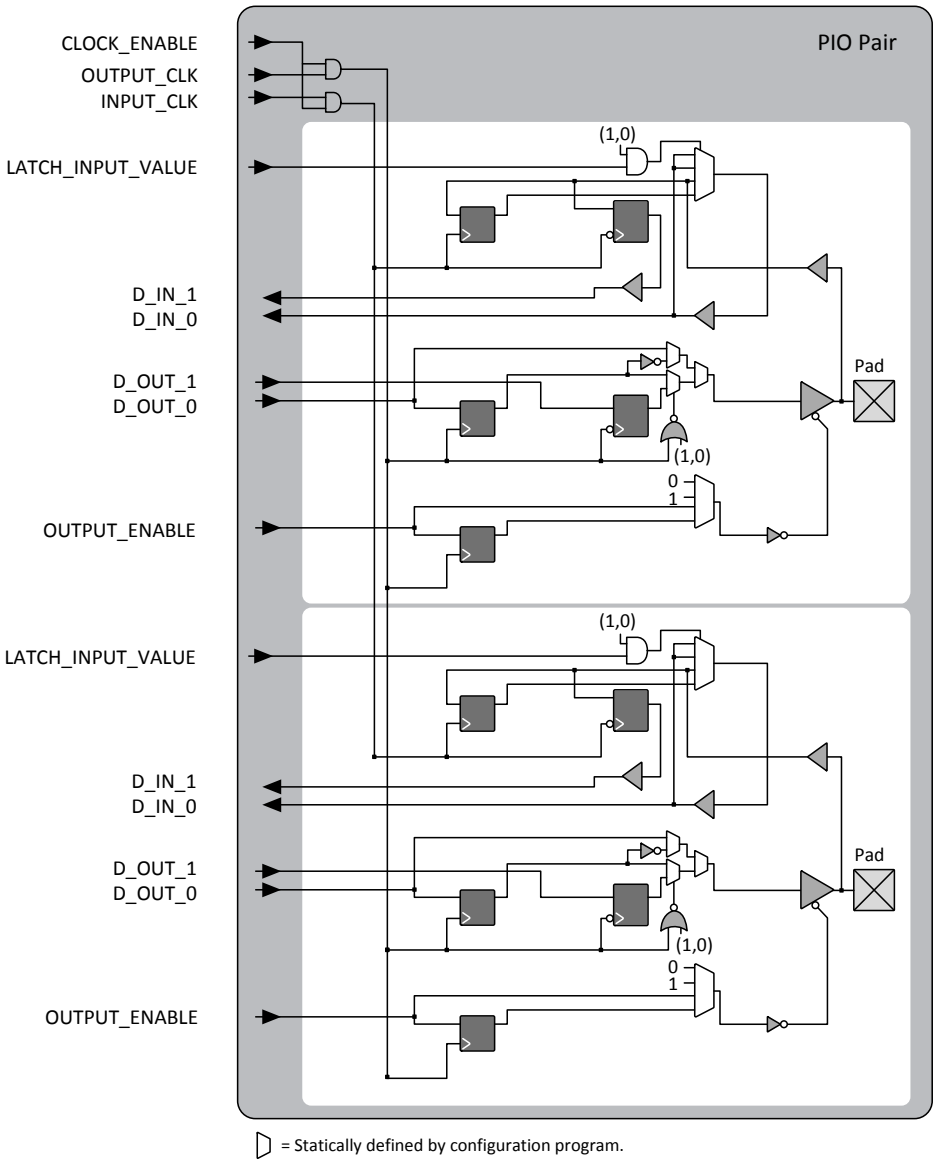


**Figure 3.10. iCE I/O Register Block Diagram**

**Table 3.8. PIO Signal List**

| Pin Name | I/O Type | Description |
|---|---|---|
| OUTPUT_CLK | Input | Output register clock |
| CLOCK_ENABLE | Input | Clock enable |
| INPUT_CLK | Input | Input register clock |
| OUTPUT_ENABLE | Input | Output enable |
| D_OUT_0/1 | Input | Data from the core |
| D_IN_0/1 | Output | Data to the core |
| LATCH_INPUT_VALUE | Input | Latches/holds the Input Value |

### 3.1.9. sysIO Buffer

Each I/O is associated with a flexible buffer referred to as a sysIO buffer. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysIO buffers allow users to implement a wide variety of standards that are found in today's systems with LVCMOS interfaces.

#### Typical I/O Behavior During Power-up

The internal power-on-reset (POR) signal is deactivated when $V_{CC}$, SPI_$V_{CCIO1}$ and $V_{PP\_2V5}$ reach the level defined in Table 4.4. After the POR signal is deactivated, the FPGA core logic becomes active. You must ensure that all $V_{CCIO}$ banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. The default configuration of the I/O pins in a device prior to configuration is tri-stated with a weak pull-up to $V_{CCIO}$. The I/O pins maintain the pre-configuration state until $V_{CC}$, SPI_$V_{CCIO1}$ and $V_{PP\_2V5}$ reach the defined levels. The I/Os take on the software user-configured settings only after POR signal is deactivated and the device performs a proper download/configuration. Unused I/Os are automatically blocked and the pull-up termination is disabled.

#### Supported Standards

The iCE40 UltraPlus sysIO buffer supports both single-ended input/output standards, and used as differential comparators. The buffer supports the LVCMOS 1.8 V, 2.5 V, and 3.3 V standards. The buffer has individually configurable options for bus maintenance (weak pull-up or none).

Table 3.9 and Table 3.10 show the I/O standards (together with their supply and reference voltages) supported by the iCE40 UltraPlus devices.

#### Differential Comparators

The iCE40 UltraPlus devices provide differential comparator on pairs of I/O pins. These comparators are useful in some mobile applications. See the Pin Information Summary section on page 44 to locate the corresponding paired I/Os with differential comparators.

**Table 3.9. Supported Input Standards**

| I/O Standard | $V_{CCIO}$ (Typical) | | |
|---|---|---|---|
| | 3.3 V | 2.5 V | 1.8 V |
| **Single-Ended Interfaces** | | | |
| LVCMOS33 | Yes | — | — |
| LVCMOS25 | — | Yes | — |
| LVCMOS18 | — | — | Yes |

**Table 3.10. Supported Output Standards**

| I/O Standard | $V_{CCIO}$ (Typical) |
|---|---|
| **Single-Ended Interfaces** | |
| LVCMOS33 | 3.3 V |
| LVCMOS25 | 2.5 V |
| LVCMOS18 | 1.8 V |

### 3.1.10. On-Chip Oscillator

The iCE40 UltraPlus devices feature two different frequency Oscillator. One is tailored for low-power operation that runs at low frequency (LFOSC). Both Oscillators are controlled with internally generated current.

The LFOSC runs at nominal frequency of 10 kHz. The high frequency oscillator (HFOSC) runs at a nominal frequency of 48 MHz, divisible to 24 MHz, 12 MHz, or 6 MHz by user option. The LFOSC can be used to perform all always-on functions, with the lowest power possible. The HFOSC can be enabled when the always-on functions detect a condition that would need to wake up the system to perform higher frequency functions.