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USB Type-C Demo Kit V2 Board User Guide

EB99 Version 1.0, June 2015

Introduction

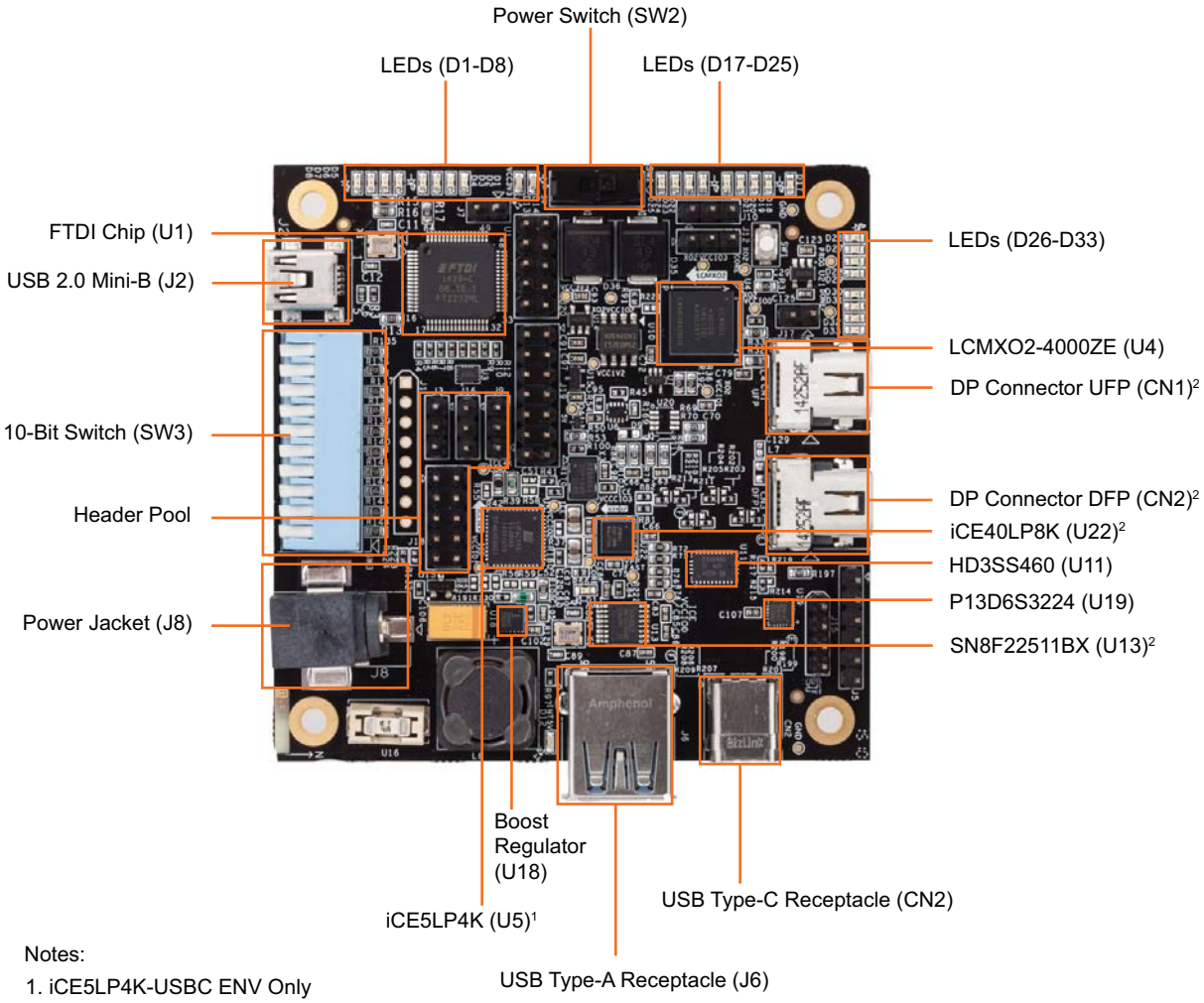
The USB Type-C Demo Kit V2 has been developed to support a variety of demos, encompassing different levels of the USB Type-C functionality which includes Power Delivery and negotiation, power and data role swap, control channel negotiation, super speed signaling, DP alternate mode support and a low speed signal aggregation function. There are two versions of this board, as identified by the Ordering Part Numbers (iCE40LP8K-USBC-EVN and iCE5LP4K-USBC-EVN). This document is applicable to either version, with the notes as applicable.

The main circuits on the development kit board:

- Programming Circuit
  - — Mini-USB Type B connector to FTDI
  - — FTDI to MachXO2™ Programming Mux
- MachXO2-4000ZE
  - — Programming Multiplexing
  - — Signal Generator and Receiver for aggregation
  - — General Purpose I/O
  - — LED Display Control
- iCE40LP-8K (iCE40LP8K-USBC-EVN only)
  - — Super-speed signaling control
  - — CD-PD physical layer and power delivery manager
  - — Billboard support
  - — DP alternate mode support and control
  - — Aggregator support
  - — AP interface
  - — Data logging
- iCE5LP-4K (iCE5LP4K-USBC-EVN only)
  - — Super-Speed signaling Control
  - — CD-PD physical layer and power delivery manager
  - — AP interface
  - — Data logging

Figure 1 is the top view of the USB Type-C Demo Kit V2 Board showing the key components present on the board.

Figure 1. Top View of USB Type-C Demo Kit V2 Board with Key Components



Notes:
1. iCE5LP4K-USBC ENV Only
2. iCE40LP8K-USBC ENV Only

Headers and Test Connectors

Figure 2 shows the top view of the demo board. The numbers of headers and test connectors which provide access to USB Type-C Demo Kit V2 Board circuits are indicated.

Figure 2. Top View of the USB Type-C Demo Kit V2 Board with Headers and Test Connectors

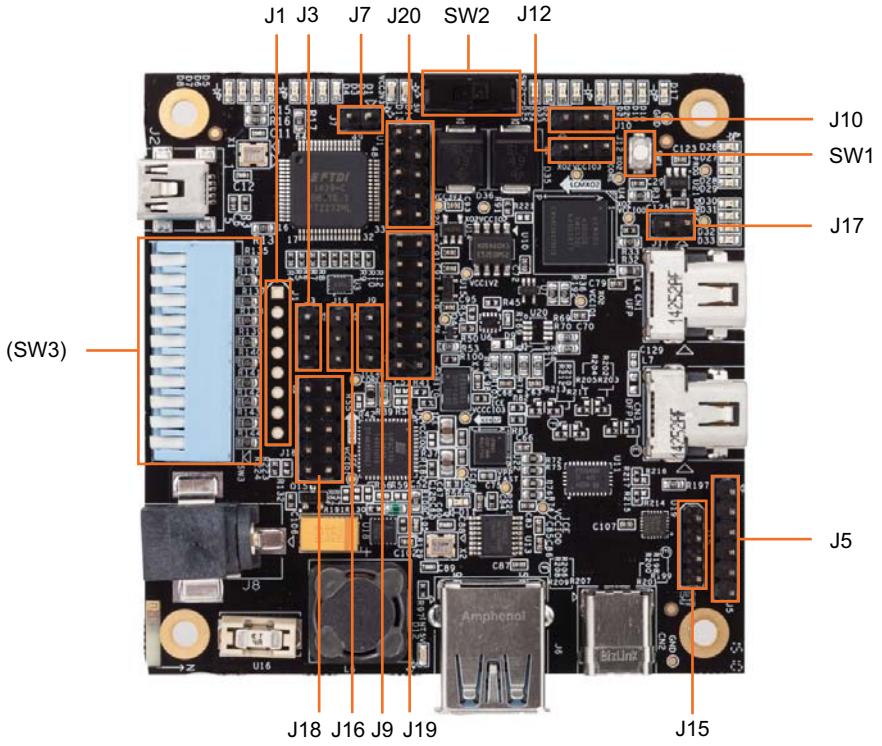


Table 1 provides the detailed definition of the headers and test connectors.

Table 1. Headers and Test Connectors

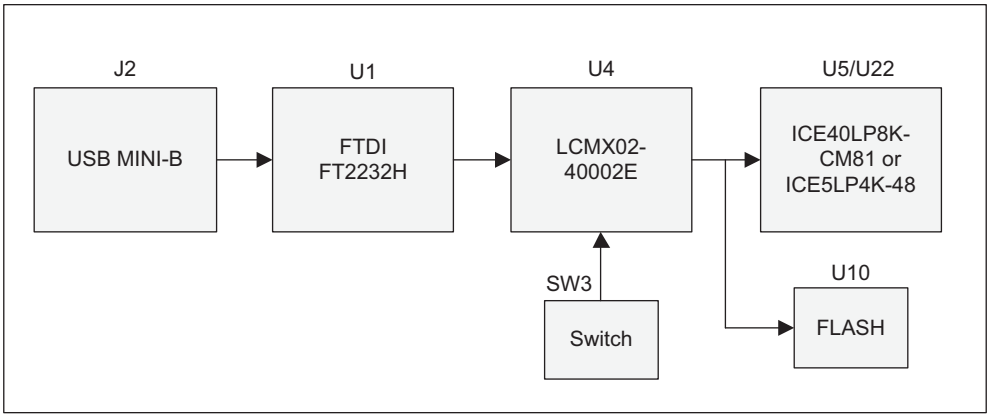
Part	Description	Setting Options	Default Setting
J1	External JTAG I/F		
J3	JTAG/SPI Selection	1-2 (SPI), 2-3 (JTAG)	JTAG
J16	JTAG/I2C Selection	1-2 (JTAG), 2-3 (I2C)	JTAG
SW1	MachXO2 Reset Switch		
J17	Jumper for DP Power	Open-Off, Short-On	Open
J5	BB Device Programmer I/F		
SW2	Board Power Switch	Left-On, Right-Off	Right
J7	VBUS Sink Connector	Open-Off, Short-On	Open
SW3	General Purpose Input Switch		
J9	USB Role Selection	1-2 (UFP), 2-3 (DFP)	Open
J10	MachXO2 I/O HIZ Enable	1-2 (Enable), 2-3 (Disable)	Open
J15	For Testing/Probing		
J12	MachXO2 I/O Direction Input	1-2 (Input), 2-3 (Output)	Open
J20	For Testing/Probing		
J18	External I2C I/F		
J19	External AGG Inputs		

Programming Circuit

The Mini-USB Type B connector is used for programming the board, using the standard Diamond Programmer software. Figure 3 shows the programming block of the USB Type-C Demo Kit V2.

The Mini-USB Type B connector interfaces with the FTDI FT2232H IC. The FTDI IC works with Diamond programmer to provide interfaces for JTAG (for programming MachXO2-4000ZE) and SPI (for programming both the iCE40™ LP and iCE40 Ultra™ devices and their SPI Flash Memories). The SPI programming works in conjunction with a mux design that must be programmed into the MachXO2-4000ZE. The mux design operation and required switch settings are described in detail in the next section. When the MachXO2 device contains the mux design and the proper switch settings are chosen, the Diamond Programmer interfaces directly with the iCE40 devices or SPI Flashes.

Figure 3. Programming Block



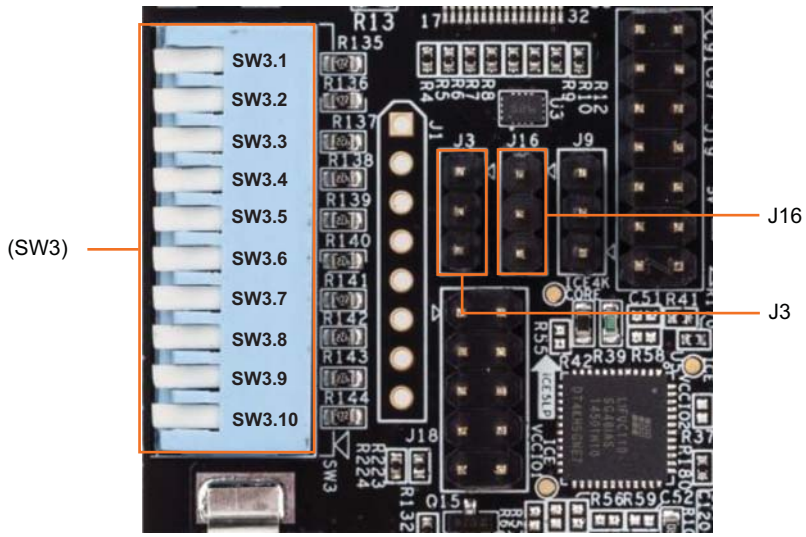
Programming Mux and Switch Settings

The board allows for programming the various devices contained on the USB Type-C Demo Kit V2:

- MachXO2 (LCMXO2-4000ZE-1MG132C) – U4
- iCE40 LP (iCE40LP8K-CM81) – U22
  - — Configuration or Programming
  - — iCE40 Ultra External SPI Flash – U10
    - — Micron Technology Inc. (N25Q032A13ESC40F)
  - — CDONE LED (Red) – D11
- iCE40 Ultra (iCE5LP4K-SG48) – U7
  - — Configuration or Programming
  - — iCE40 Ultra External SPI Flash - U6
    - — Micron Technology Inc (N25Q032A13ESC40F)
  - — CDONE LED (Green) – D9
- iCE40 Device CRESETB can be asserted by pushing SW1
  - — Routed through MachXO2 device

Figure 4 shows the DIP switch numbering and settings.

Figure 4. DIP Switch Numbering



Two positions of the DIP switch SW3 and the header J3 are used to control which devices and which mode the FTDI Bridge utilizes. Table 2 provides the detailed definitions of the DIP switch settings required to program each device.

Table 2. DIP Switch Settings to Program the Device

Device	Operation	Mode	Jumper Position		DIPSW (SW3) Position	
			J16	J3	SW3.10	SW3.9
MachXO2	Program/Configure	JTAG	1-2	3-2	Up	Down
iCE40 CRAM	Program/Configure	SPI	1-2	1-2	Down	Down
iCE40 Flash	Program/Configure	SPI	1-2	1-2	Down	Up
(All)	Boot	—	3-2	—	Up	Up

Note: The MachXO2 must be programmed with an image containing the SPI programming multiplexing and CRESET level-shifting driver (for example, the default image asdf.jed) prior to programming or configuring the iCE40 devices or their subtended SPI Flash devices.

Status Indicators

The board provides the number of LED status indicators, shows power, configuration, and an application status. Table 3 provides the detailed definition of the Status LED I/O Map.

Table 3. Status LED I/O Map

Device	I/O Balls	LED	Schematic NET	Bank	Color
LCMX02-4000ZE	B1	D1	AGG_LED1	3	Green
LCMX02-4000ZE	B2	D2	AGG_LED2	3	Green
LCMX02-4000ZE	C1	D3	AGG_LED3	3	Green
LCMX02-4000ZE	C2	D4	AGG_LED4	3	Green
LCMX02-4000ZE	C3	D5	AGG_LED5	3	Green
LCMX02-4000ZE	D1	D6	AGG_LED6	3	Green
LCMX02-4000ZE	E1	D7	AGG_LED7	3	Green
LCMX02-4000ZE	E2	D8	AGG_LED8	3	Green
LCMX02-4000ZE	J3	D17	STATUS_LED1	3	Blue
LCMX02-4000ZE	K1	D20	STATUS_LED2	3	Blue
LCMX02-4000ZE	K2	D22	STATUS_LED3	3	Green
LCMX02-4000ZE	K3	D23	STATUS_LED4	3	Green
LCMX02-4000ZE	L3	D26	STATUS_LED5	3	Red
LCMX02-4000ZE	M1	D27	STATUS_LED6	3	Red
LCMX02-4000ZE	M2	D30	STATUS_LED7	3	Yellow
LCMX02-4000ZE	N9	D31	STATUS_LED8	2	Yellow
LCMX02-4000ZE	N10	D33	STATUS_LED9	2	Yellow
LCMX02-4000ZE	P2	D18	STATUS_LED10	2	Blue
LCMX02-4000ZE	P4	D19	STATUS_LED11	2	Blue
LCMX02-4000ZE	P6	D21	STATUS_LED12	2	Green
LCMX02-4000ZE	P7	D23	STATUS_LED13	2	Green
LCMX02-4000ZE	P8	D25	STATUS_LED14	2	Green
LCMX02-4000ZE	P9	D28	STATUS_LED15	2	Blue
LCMX02-4000ZE	P11	D29	STATUS_LED16	2	Blue
LCMX02-4000ZE	P12	D32	STATUS_LED17	2	Blue
ICE5LP4K	7	D9	4KDONE	2	Red
ICE40LP8K	E6	D11	CDONE	2	Red

MachXO2-4000ZE Circuit Overview

LCMXO2-4000ZE-1MG132C

The MachXO2 device (LCMXO2-4000ZE-1MG132C) on the board performs a variety of functions:

- Programming Multiplexing
  - — Interface from PC/FTDI to iCE5LP, iCE40LP, and SPI Flash memories
- Signal Aggregator Demo Function
  - — Includes interface to iCE40LP8K
- General Purpose I/O from DIP switches and LEDs

The USB demo design includes bitstreams for the MachXO2.

Note: Refer to the documents accompanying each demo for details on the specific design function of the MachXO2.

Tables provide the detailed definition of the different functions:

- LED Indication (Table 3)
- Switches (Table 4)
  - — DIP Switches
  - — Push Button
  - — 3-pin Headers
- iCE40LP8K/iCE5LP4K Interface (Table 5)
- External Application Processor Interface (Table 6)

Table 4 provides the detailed definition of the I/O Map for the device MachXO2 general purpose functions.

Table 4. Switches / I/O Map for MachXO2

Device	I/O Ball	Schematic Net	Bank	Designator
LCMX02-4000ZE	B9/B12	CONFIG_SW1	0	SW3
LCMX02-4000ZE	B14	CONFIG_SW2	1	SW3
LCMX02-4000ZE	C13	CONFIG_SW3	1	SW3
LCMX02-4000ZE	C14	SW4	1	SW3
LCMX02-4000ZE	D12	SW5	1	SW3
LCMX02-4000ZE	E12	SW6	1	SW3
LCMX02-4000ZE	E13	SW7	1	SW3
LCMX02-4000ZE	E14	SW8	1	SW3
LCMX02-4000ZE	F12	SW9	1	SW3
LCMX02-4000ZE	F13	SW10	1	SW3
LCMX02-4000ZE	A2	XO2_RESET	0	SW1
POWER	—	5V	—	SW2

Table 5. Aggregator I/O Map for MachX02

MACHX02(U4)		ICE40LP8K(U22)		HD3SS460(U11) Pin Number	Schematic Net
I/O Ball	Bank	I/O Ball	Bank		
F1	3	B6	0	—	AGG_GPIO1
F2	3	A6	0	—	AGG_GPIO2
F3	3	B5	0	—	AGG_GPIO3
G3	3	A4	0	—	AGG_GPIO4
H1	3	B4	0	—	AGG_GPIO5
H2	3	D5	0	—	AGG_GPIO6
H3	3	E5	0	—	AGG_GPIO7
J1	3	A3	0	—	AGG_GPIO8
B8	0	A8	0	—	SDA1
C8	0	B8	0	—	SCL1
A9	0	B7	0	—	SDA2
A7	0	A7	0	—	SCL2
		A2	0	13	AUX_CHP
		A1	0	14	AUX_CHN

The MachXO2-4000ZE and an iCE40LP8k/iCE5LP4K provides connections to the header J18 (Embedded controller connector). Table 6 provides the detailed definition of the signals.

Table 6. AP Interface for MachXO2, iCE40LP/iCE5LP and J18

iCE40LP8K(U22)		iCE5LP4K(U5)		XO2(U4)		J18	Schematic Net Name
IO Ball	Bank	IO Ball	Bank	IO Ball	Bank		
G7	SPI	15	2	M7	2	1	SPI_SCK
G4	2	18	2	N4	2	3	EC_CS
G6	SPI	14	2	M9	2	5	SPI_MISO
H7	SPI	17	2	M8	2	8	SPI_MOSI

iCE40LP8K

The iCE40LP8K (U5/U22) is one of the devices on the board used to demonstrate the Lattice Type-C Power Delivery (PD) management and Cable Detect (CD) solution. In order to support the variety of demos, the iCE device provides multiple parallel and serial connections to the MachXO2 device on the board. Table 5 and Table 6 provide the detailed definition of the connections. Both the devices are connected to the J18 (Embedded Controller header).

The iCE configuration may be stored in external SPI Flash (Refer the section Programming Mux and Switch Settings for more information. The external SPI Flash (U10) is connected to the configuration SPI port of the iCE device. These signals, along with the CDONE and CRESET signals from the iCE are connected to the MachXO2-4000ZE device to facilitate connection from the PC (for programming) to both the iCE and SPI Flash.

The 25 MHz oscillator X2 is used to provide an external clock signal to the iCE40LP device. This clock signal is also passed to the iCE5LP device. Table 7 provides the detailed definition of the clock connections.

Table 7. Clock Connections for iCE40LP

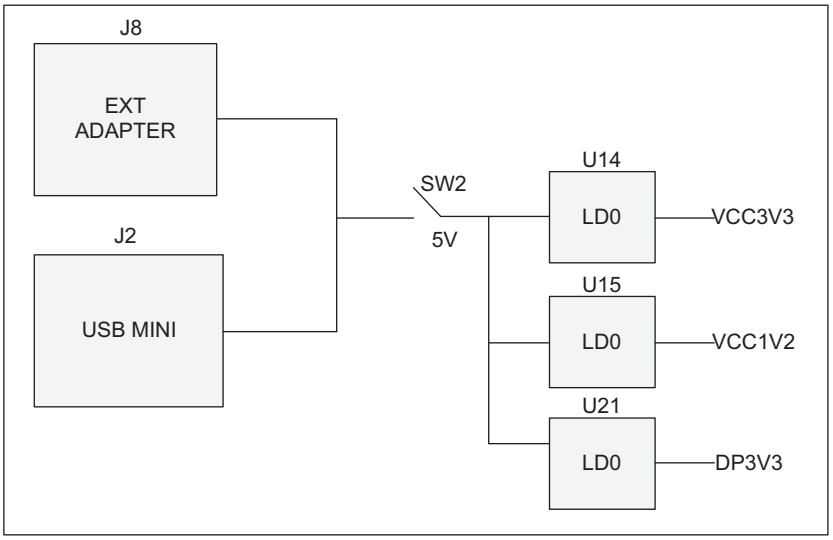
ICE40LP8K(U22)		ICE5LP4K(U5)		Schematic Net
IO Ball	Bank	IO Ball	Bank	Name
D8	1	20	2	CLK IN

Power Supply

Power supply to the development kit is by the MINI-USB Type-B connector or from an external adaptor. This connector provides 5 V source for the voltage regulators on the board which supply the power to MachXO2 and iCE devices on the board. Each IO and core voltage rail on the board is accessible by a test point on the board. The current flowing to each rail can also be measured using a 1Ω resistor placed in the path of each voltage rail.

Figure 5 shows the device power rails. There are three voltage regulators on the board used to supply the 3.3 V, 1.8 V, and 1.2 V rails. The input to these regulators is the 5 V rail on the board, which is supplied from either the MINI-USB Type-B connector or external power adaptor via switch SW2.

Figure 5. Device Power Rails



Several of the voltage rails also connect to indicator LEDs on the board to display the power status to the user. These LEDs are listed in Table 8.

Table 8. Voltage Rail Indicator LEDs

Voltage Rail	Indicator LED	Color
INT_5V	D12	Blue
VCC3V3	D14	Yellow
5V	D14	Yellow

The board voltage rails are summarized in Table 9, including the rail source voltage, test point #, and current sense resistor number.

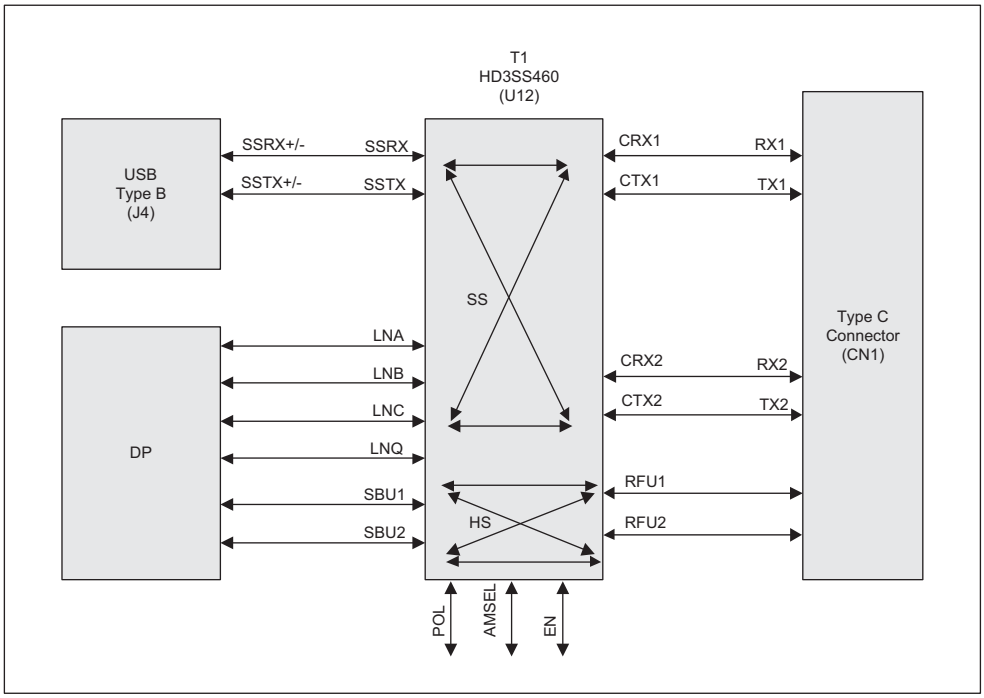
Table 9. Device Power Rail Summary and Test Points

Voltage Rail	Source Rail	Sense Resistor	Test Point #
VCC_SPI	VCC3V3	—	TP18
VCONN_5V	5V	R106	—
XO2_VCCIO0	VCC3V3	R107	TP6
XO2_VCCIO1	VCC3V3	R109	TP8
XO2_VCCIO2	VCC3V3	R111	TP10
XO2_VCCIO3	VCC3V3	R113	TP12
ICEVCCIO0	VCC3V3	R108	TP7
ICEVCCIO1	VCC3V3	R110	TP9
ICEVCCIO2	VCC3V3	R112	TP11
ICEVCCIO3	VCC3V3	R114	TP13
XO2_CORE	VCC3V3	R102	TP4
ICE4K_CORE	VCC3V3	R104	TP5
ICE8K_CORE	VCC3V3	R105	TP16
DP3V3	INT_5V	—	—
5V	USB5V/EXT_5V	—	TP17
VBUS	EXT_5V	—	—

USB Super-Speed Switch/Alternate Mode Function

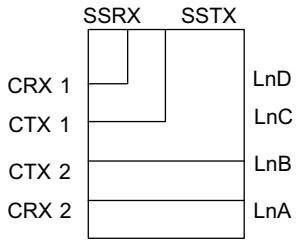
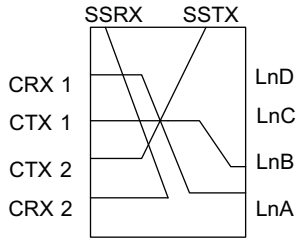
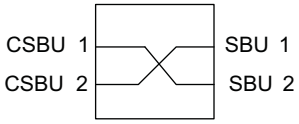
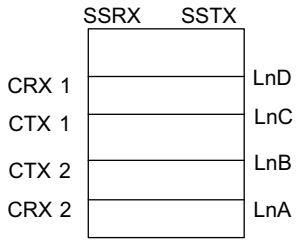
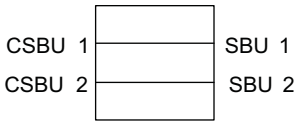
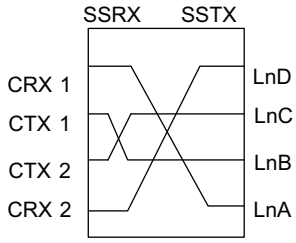
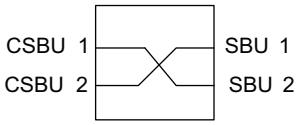
The development kit includes a super-speed switch IC (U11 - HD3SS460) along with a high-speed USB switch (U19 – PI3DBS3224). The super-speed switch IC is used to demonstrate the orientation-agnostic capability of the USB Type-C connector. The switches connect various USB sockets. Figure 6 shows the switch functions and the data flow diagram.

Figure 6. Super Speed Block



U11 is connected on one side to the standard-USB 9-pin connector (J6), the Mini DP connectors (CN1 and CN3) and the other side connected to the USB Type-C connector (CN1). J6 provides a bi-directional Super-Speed channel as well as a bi-directional High-Speed channel, with CN1, CN2 providing a unidirectional display source data. The U11 switch connection is managed by the iCE40 device on the board, using the SS_EN, SS_AMSEL, and SS_POL signal inputs to U11. For more information refer the documentation on the super-speed switch demo. Table 10 provides the detailed definition of the mode supported by the super speed switch.

Table 10. Modes Supported by Super Speed Switch

POL	AMSEL	EN	Configurations	High Speed Signal Flow	SBU Signal Flow
L	L	H	2CH USB SS + 2CH AM (Normal)		
H	L	H	2CH USBSS + 2CH AM (Flipped)		
L	H	H	4CH AM (Normal)		
H	H	H	4CH AM (Flipped)		

Note: This board (iCE40LP8K-USBC-EVN) supports Display Port as an Alternate Mode function. By default board population option is data sink. To modify it as data source, make the following changes on the board.
R199,R201,R203,R205,R207,R209,R211,R213,R215,R217-Do Not Populate
R198,R200,R202,R204,R206,R208,R210,R212,R214,R216-Populate

USB High Speed Function

High speed switch function done by the device (U19) which receives inputs from the standard-USB 3.0 type A connector J6 and the Billboard device (U13) data using USB2.0 protocol and switches either of one to the Type-C connector (CN2). The switching behavior of U13 is controlled by the iCE device using the HS_SAI and HS_EN signals. Figure 7 shows the High Speed Switch.

Figure 7. High Speed Switch

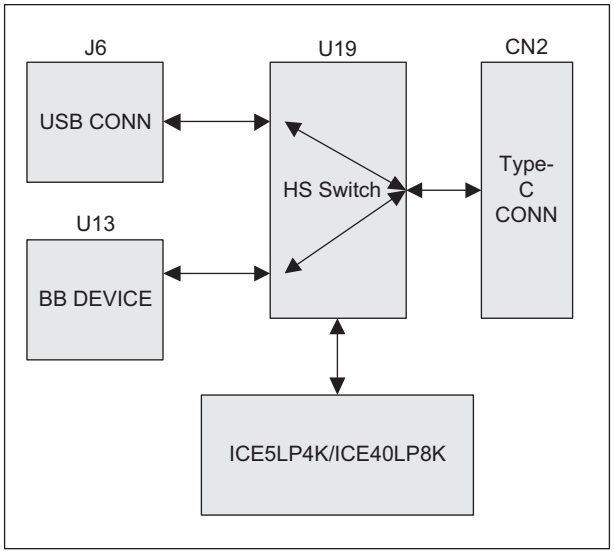


Table 11 provides the detailed definition of the MUX selection.

Table 11. MUX Selection

ENA/B	SAI	OUTA0
0	X	Hi-Z
1	1	INA
1	0	INB

Billboard Interface

Billboard interface is the feature supported by USB Type-C protocol and which functioned by U13 and based on the iCE control for the HS switch it will be terminated to the Type-C connector (CN2). Table 12 provides the detailed definition of the Billboard Interface I/O map and associated net names.

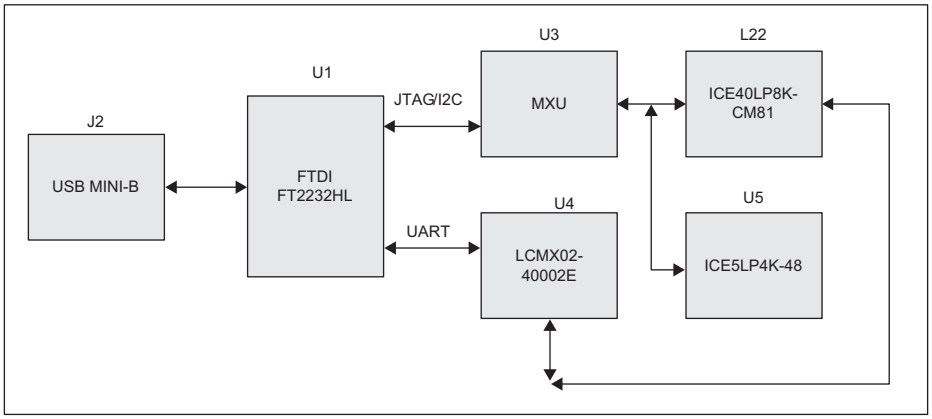
Table 12. Billboard Interface

ICE40LP8K(U22)		SNF225111BX(U13)	J5	PI3DBS3224(U19)	Schematic Net
I/O Ball	Bank	Pin Name	Pin Number	Pin Number	
C4	0	P5.0/SCK	—	—	BB_SCK
H5	2	P5.0/SDO	—	—	BB_SDO
G5	2	P5.1/SDI	—	—	BB_SDI
C5	0	P0.1/INT1	—	—	BB_INT
—	—	P1.0	2	—	BB_PGM
—	—	P1.1	3	—	BB_ALSB/PDB
—	—	P2.0	5	—	BB_CLK
—	—	P2.1	4	—	BB_OE
—	—	DN	—	4	BB_DN
—	—	DP	—	3	BB_DP

Data Logging Interface

Data logging interface can use a terminal screen such as HyperTerminal or Putty to display PD transactions of the USB Type-C Demo Kit V2. Figure 8 shows the data flow and the block diagram of the data logging interface.

Figure 8. Data Logging Interface



Ordering Information

Description	Ordering Part Number	China RoHS Environment-Friendly Use Period
iCE40LP8K USB Type-C Demo Kit V2	iCE40LP8K-USBC-EVN	
iCE40 Ultra USB Type-C Demo Kit V2	iCE5LP4K-USBC-EVN	

Technical Support Assistance

Submit a technical support case via www.latticesemi.com/techsupport.

Revision History

Date	Version	Change Summary
June 2015	1.0	Initial release.

Appendix A. Schematic Diagrams

Figure 9. Block Diagram

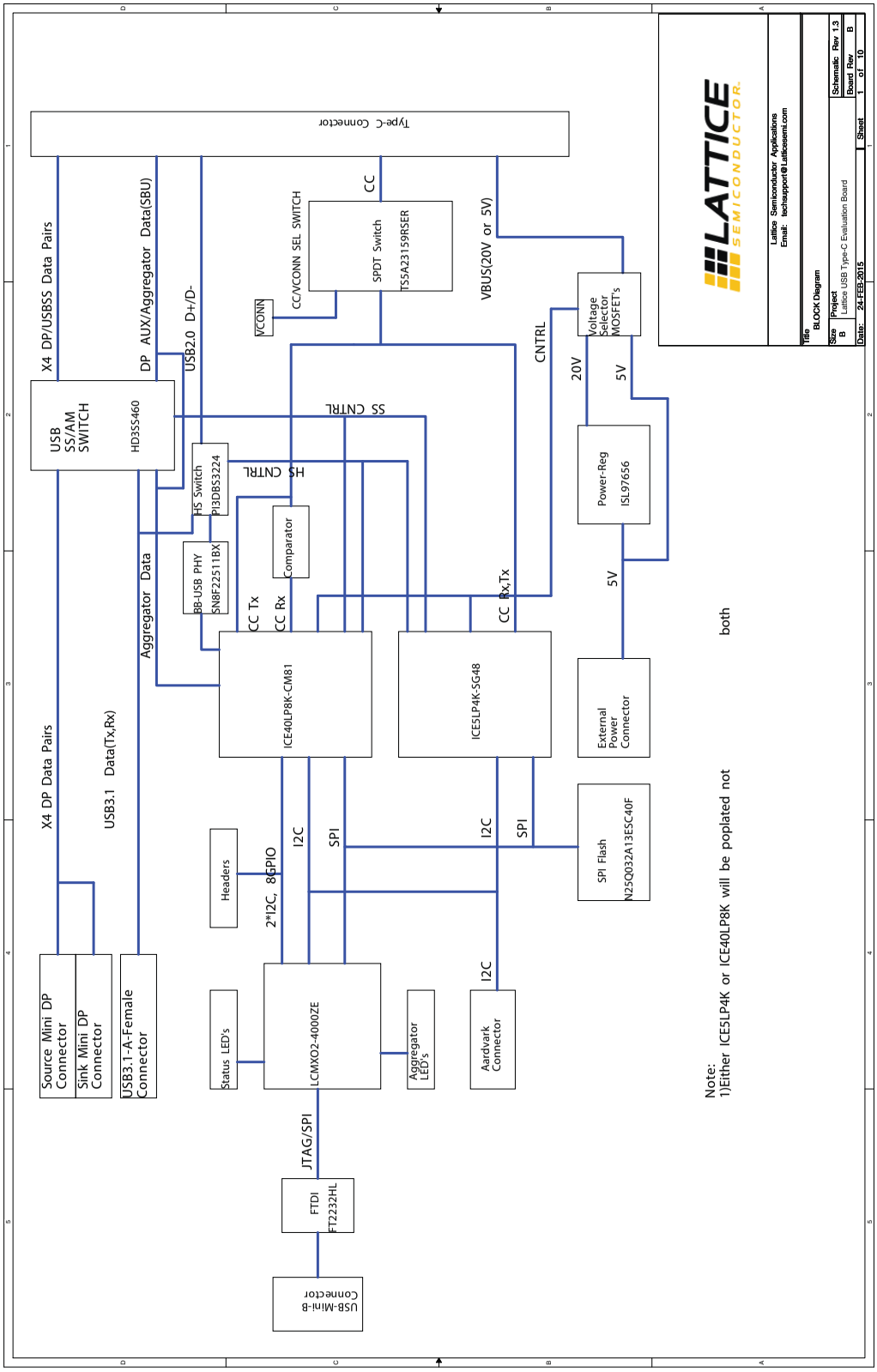


Figure 10. FTDI I/F

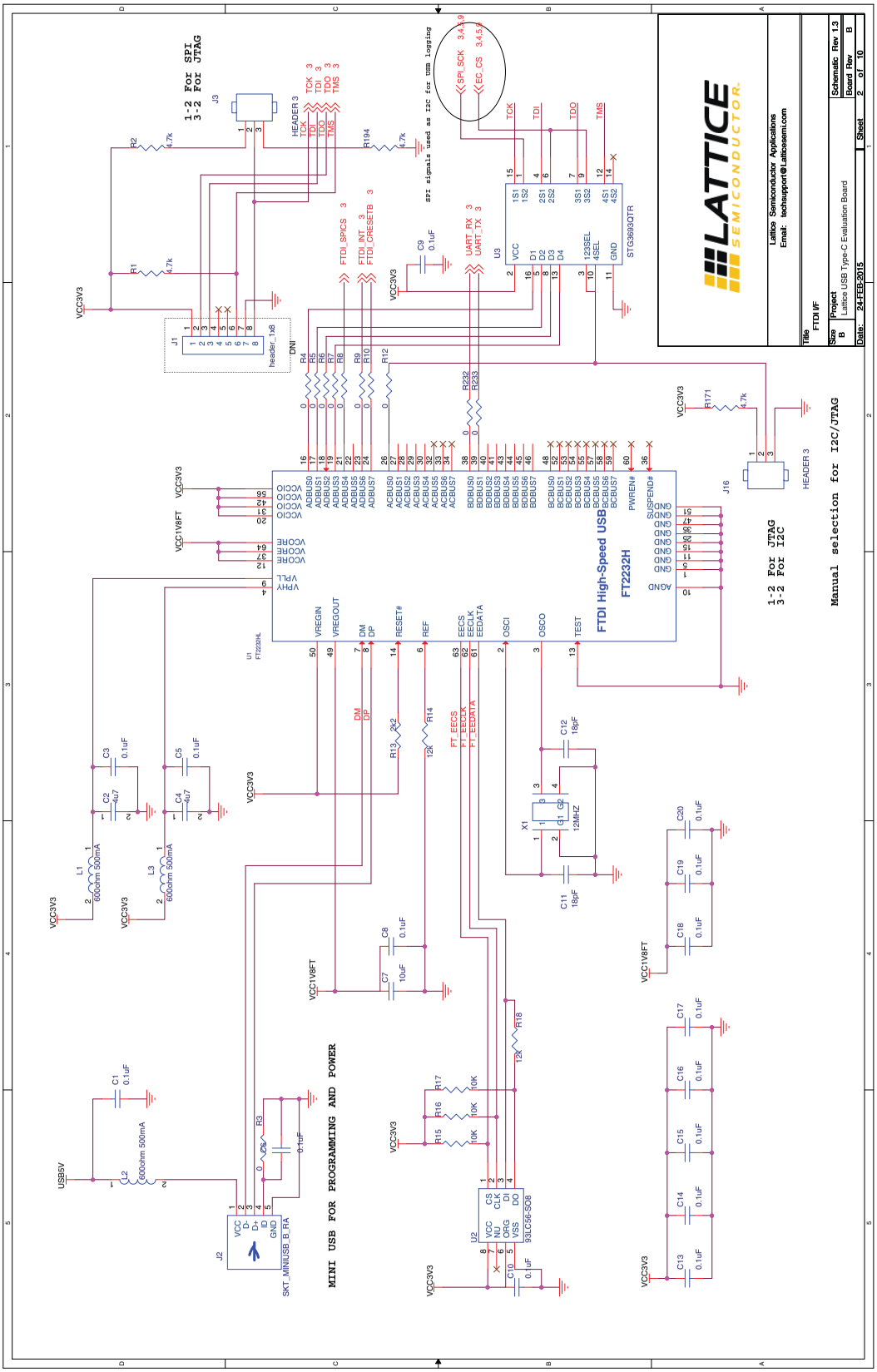


Figure 11. MachXO2 I/F

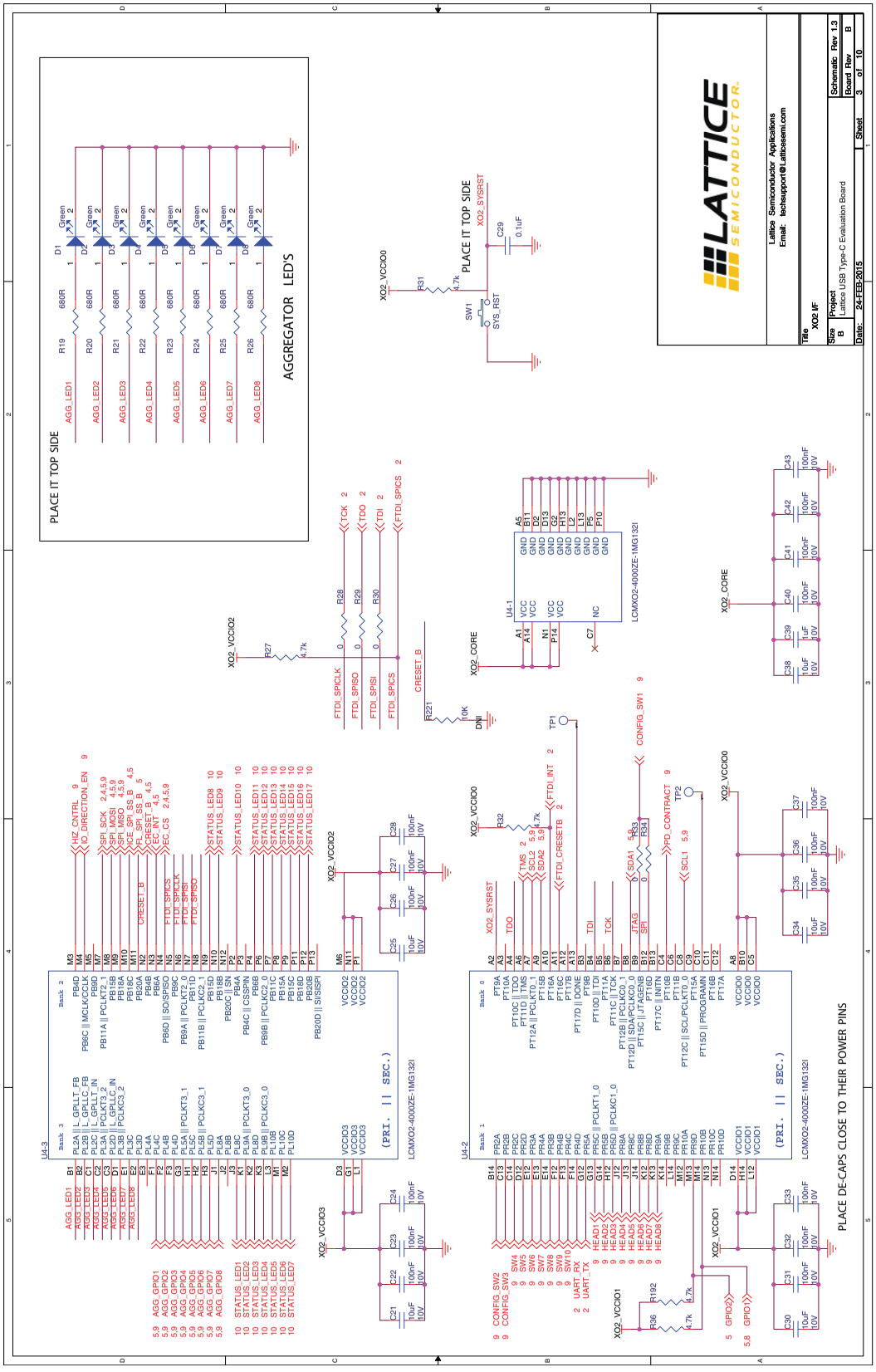


Figure 12. iCE5LP4K I/F

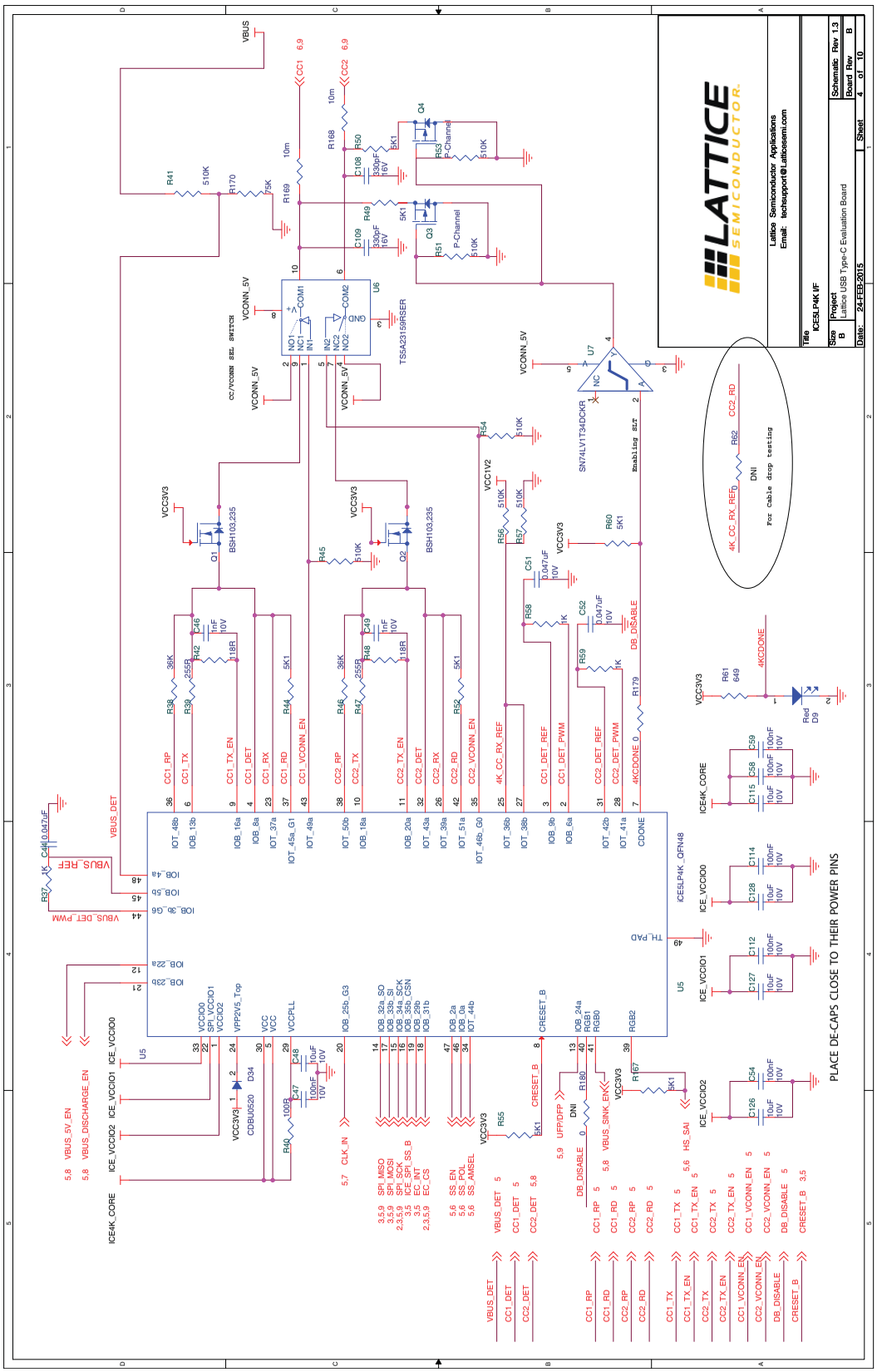


Figure 13. iCE5LP8K I/F

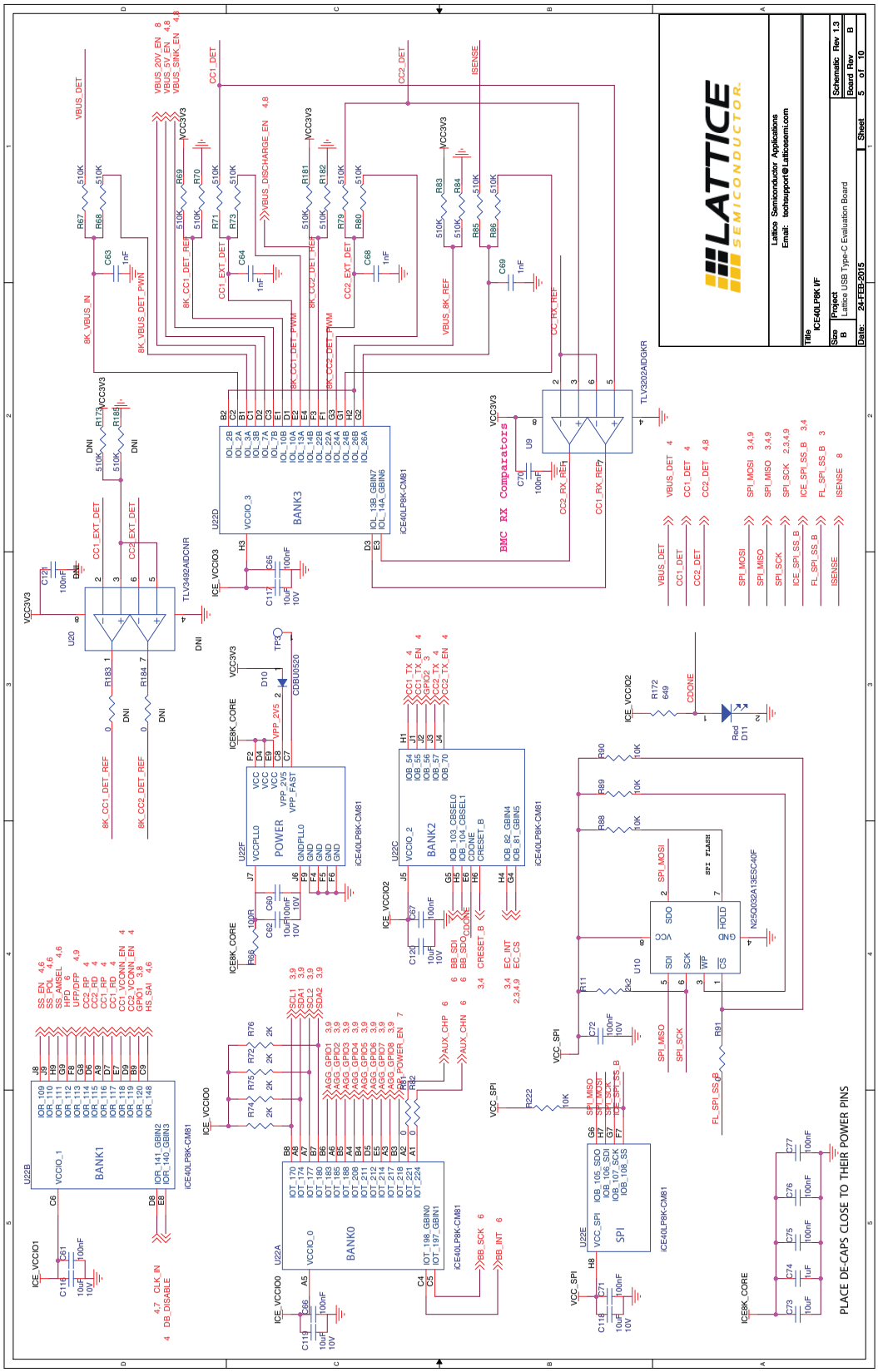


Figure 14. SS/DP/BB I/F

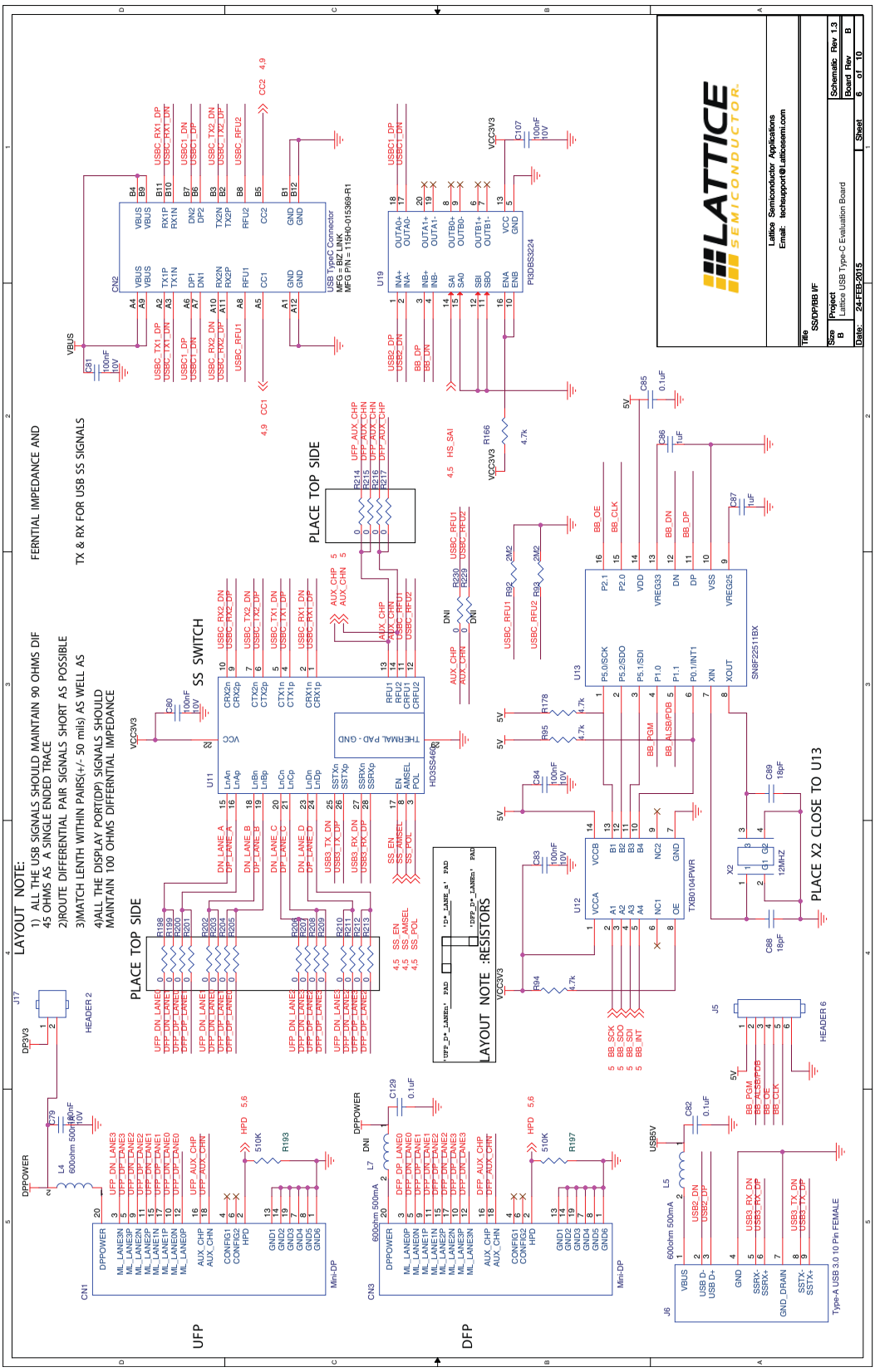


Figure 15. Power Regulator I/F

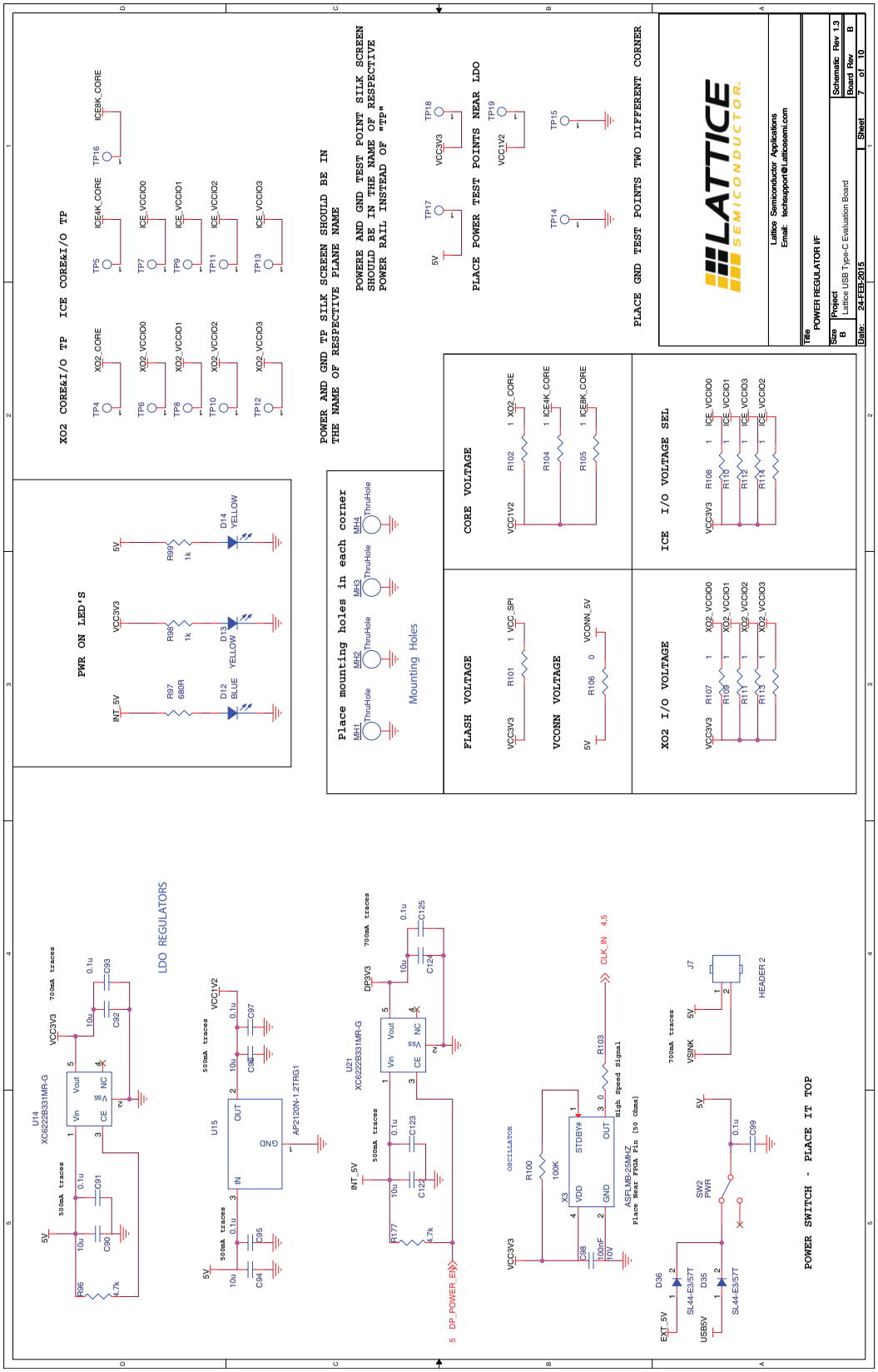


Figure 16. Power Source/Sink I/F

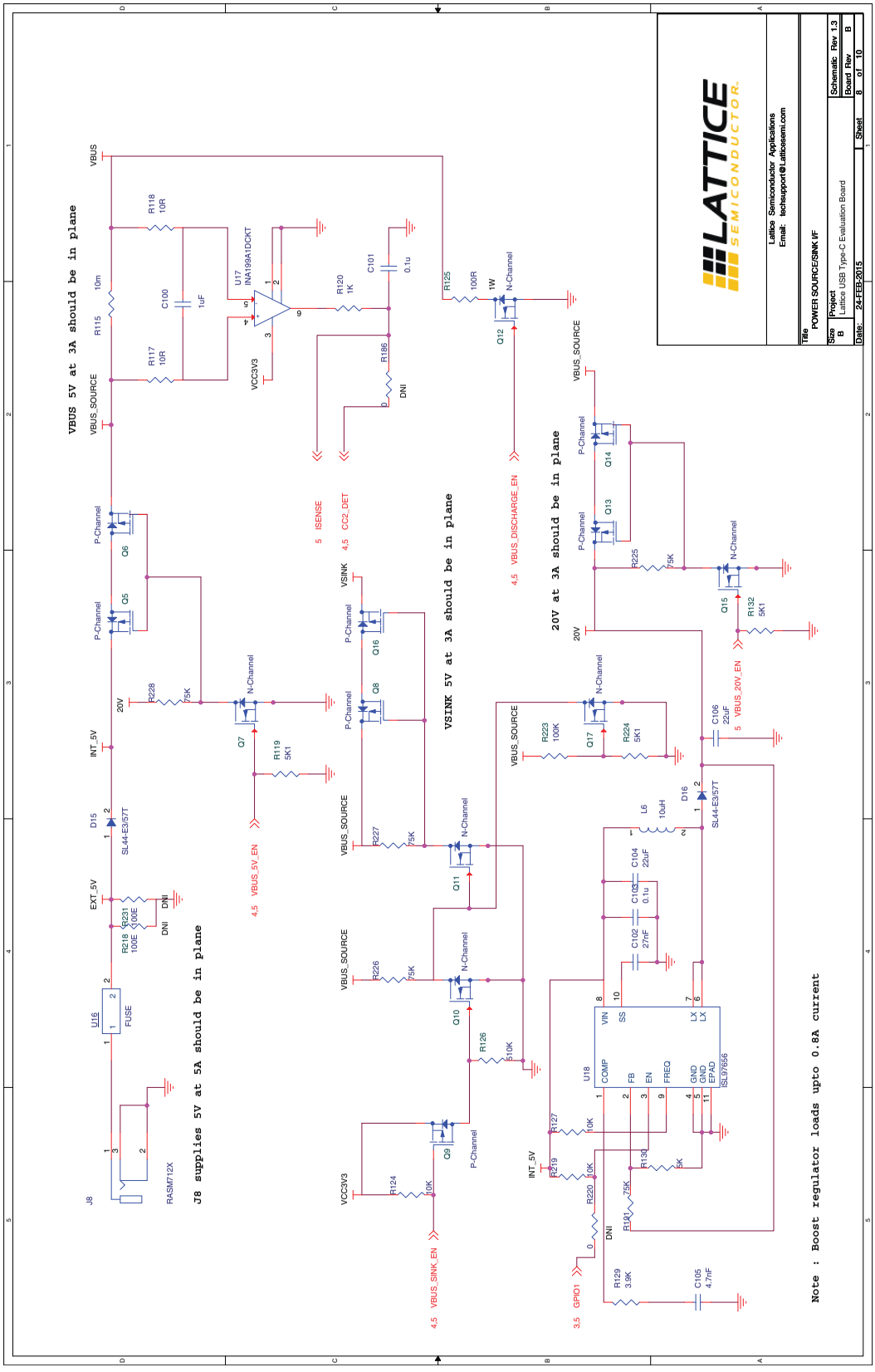


Figure 17. Headers and Switch I/F