Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

ICG-20330

High Performance 3-Axis OIS/EIS Optimized MEMS Gyro

GENERAL DESCRIPTION

The ICG-20330 is a 3-axis MotionTracking® device that includes a 3-axis gyroscope in a small 3x3x 0.75 mm (16-pin LGA) package.

- High performance specs
  - Gyroscope sensitivity error: ±1%
  - Gyroscope noise: 5 mdps/√Hz
- Includes 512-byte FIFO to reduce traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode
- EIS FSYNC support

ICG-20330 includes on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features an operating voltage range down to 1.71V. Communication ports include I^2C and high-speed SPI at 7 MHz.

ORDERING INFORMATION

PART	AXES	TEMP RANGE	PACKAGE
ICG-20330†	X,Y,Z	-40°C to +85°C	16-Pin LGA

†Denotes RoHS and Green-Compliant Package

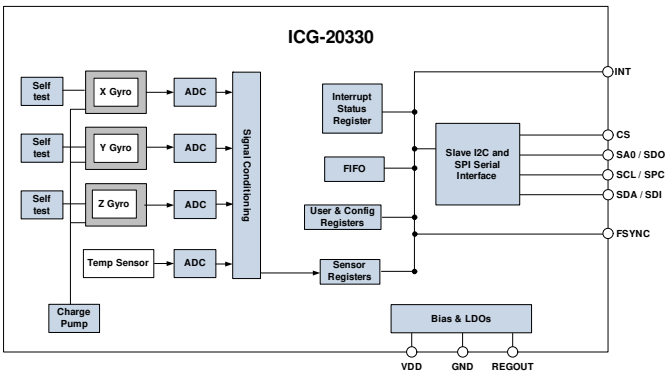
APPLICATIONS

- OIS (Optical Image Stabilization) in phone camera modules, DSLR, and DSC
- EIS (Electronic Image Stabilization) in DSC, and phone camera modules

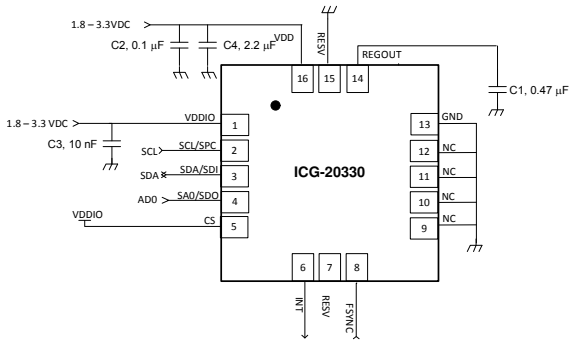
FEATURES

- 1% Gyro initial sensitivity eliminates OIS dynamic calibration
- Optimized OIS/EIS programmable gyro FSR of ±31.25dps, ±62.5dps, ±125ps and ±250dps
- High Resolution at up to 1048 LSB/(°/s)
- Low 5mdps/√Hz Noise
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- 512-byte FIFO buffer enables the applications processor to read the data in bursts
- On-Chip 16-bit ADCs and Programmable Filters
- Host interface: 7 MHz SPI or 400 kHz Fast Mode I^2C
- Digital-output temperature sensor
- VDD operating range of 1.71 V to 3.45 V
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

BLOCK DIAGRAM



TYPICAL OPERATING CIRCUIT



InvenSense Inc.
1745 Technology Drive, San Jose, CA 95110 U.S.A
+1(408) 988–7339
www.invensense.com

Document Number: DS-000127
Revision: 1.0
Release Date: 06/15/2016

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a preliminary product specification, providing a description, specifications, and design related information on the ICG-20330 MotionTracking device for imaging applications, such as Optical Image Stabilization, OIS, or Electronic Image Stabilization, EIS. The device is housed in a small 3x3x0.75 mm 16-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICG-20330 is a 3-axis MotionTracking device that has a 3-axis gyroscope in a small 3x3x0.75 mm (16-pin LGA) package. It also features a 512-byte FIFO for EIS applications to lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data for a given video frame. The unique support for FSYNC (frame sync), facilitates synchronization of Video Frame Sync from Image sensors and Motion data from gyro collected during a given frame via an interrupt to the host.

The gyroscope has a programmable full-scale range of ±31.25, ±62.5, ±125 and ±250 degrees/sec, optimized for Image Stabilization applications.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I^2C and SPI serial interfaces, a VDD operating range of 1.71 V to 3.6 V, and a separate digital IO supply, VDDIO from 1.71 V to 3.6 V.

Communication with all registers of the device is performed using either I^2C at 400 kHz or SPI at 7 MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 3x3x0.75 mm (16-pin LGA), to provide a very small yet high-performance, low-cost package. The device provides high robustness by supporting 10,000*g* shock reliability.

1.3 APPLICATIONS

- *OIS,* Optical Image Stabilization in phone camera modules, DSLR, and DSC
- *EIS,* Electronic Image Stabilization in DSC, and phone camera modules

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICG-20330 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ±31.25, ±62.5, ±125 and ±250 °/sec and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ADDITIONAL FEATURES

The ICG-20330 includes the following additional features:

- 512-byte FIFO buffer enable the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope and temp sensor
- 10,000 *g* shock tolerant
- 400-kHz Fast Mode I^2C for communicating with all registers
- 7-MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL= 0		±31.25		°/s	3
	FS_SEL= 1		±62.5		°/s	3
	FS_SEL= 2		±125		°/s	3
	FS_SEL= 3		±250		°/s	3
ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL= 0		1048		LSB/(°/s)	3
	FS_SEL=1		524		LSB/(°/s)	3
	FS_SEL= 2		262		LSB/(°/s)	3
	FS_SEL= 3		131		LSB/(°/s)	3
Sensitivity Scale Factor Tolerance	25°C		±1		%	1
Sensitivity Scale Factor Variation Over Temperature	-20°C to +75°C		±3		%	1
Nonlinearity	Best fit straight line; 25°C		±0.1		%	1
Cross-Axis Sensitivity			±2		%	1
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±5		°/s	2
ZRO Variation Over Temperature	-20°C to +75°C		±5		°/s	1
GYROSCOPE NOISE PERFORMANCE (FS_SEL=0)						
Total RMS Noise	DLPFCFG = 2 (92 Hz)		0.06		°/s-rms	2
Total Peak-to-Peak Noise	DLPFCFG = 2 (92 Hz)		0.30		°/s-p-p	2
Rate Noise Spectral Density	At 10 Hz		0.005		°/s/√Hz	2
GYROSCOPE MECHANICAL Mechanical Frequency Sensor Mechanical Bandwidth		 25 1.6	27	29	 KHz KHz	 2 1
LOW PASS FILTER RESPONSE	Programmable Range	92		250	Hz	3
GYROSCOPE START-UP TIME			80		ms	1
OUTPUT DATA RATE	Programmable, Normal (Filtered) mode	1000		8000	Hz	1

Table 1. Gyroscope Specifications

Notes:

1. Derived from validation or characterization of parts on PCB, not guaranteed in production.
2. Tested in production.
3. Guaranteed by design.
4. Calculated from Total RMS Noise.

3.2 ELECTRICAL SPECIFICATIONS

3.2.2 D.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	1
VDDIO		1.71	1.8	3.45	V	1
SUPPLY CURRENTS & BOOT TIME						
Active Current	3-Axis Gyroscope		2.9		mA	1
Full-Chip Sleep Mode			10		µA	1
Boot Time	VDD on to first register write		50		ms	1
TEMPERATURE RANGE						
Operating Temperature Range		-40		+85	°C	1

Table 2. D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Based on simulation.

3.2.2 A.C. Electrical Characteristics

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

Parameter	Conditions	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		100	ms	1
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
Room Temperature Offset	25°C		0		°C	1
Sensitivity	Untrimmed		326.8		LSB/°C	1
Power-On RESET						
Supply Ramp Time (T_{RAMP})	Valid power-on RESET	0.01		100	ms	1
Start-up time for register read/write	From power-up		11	100	ms	1
I²C ADDRESS	SA0 = 0 SA0 = 1		1101000 1101001			
DIGITAL INPUTS (FSYNC, SA0, SPC, SDI, CS)						
V_{IH}, High Level Input Voltage		0.7*VDDIO			V	1
V_{IL}, Low Level Input Voltage				0.3*VDDIO	V	
C_I, Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V_{OH}, High Level Output Voltage	R_{LOAD} = 1MΩ;	0.9*VDDIO			V	1
V_{OL1}, LOW-Level Output Voltage	R_{LOAD} = 1MΩ;			0.1*VDDIO	V	
$V_{OL.INT}$, INT Low-Level Output Voltage	OPEN = 1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN = 1		100		nA	
t_{INT}, INT Pulse Width	LATCH_INT_EN = 0		50		µs	
I²C I/O (SCL, SDA)						
V_{IL}, LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V_{IH}, HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V_{hys}, Hysteresis			0.1*VDDIO		V	
V_{OL}, LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I_{OL}, LOW-Level Output Current	V_{OL} = 0.4V V_{OL} = 0.6 V		3 6		mA mA	
Output Leakage Current			100		nA	
t_{of}, Output Fall Time from V_{IHmax} to V_{ILmax}	C_b bus capacitance in pf	20+0.1C_b		300	ns	
INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B = 1,2,3 SMPLRT_DIV = 0		32		kHz	2
	FCHOICE_B = 0; DLPFCFG = 0 or 7 SMPLRT_DIV = 0		8		kHz	2
	FCHOICE_B = 0; DLPFCFG = 1,2,3,4,5,6; SMPLRT_DIV = 0		1		kHz	2

Parameter	Conditions	MIN	TYP	MAX	UNITS	NOTES
Clock Frequency Initial Tolerance	CLK_SEL = 0, 6 or gyro inactive; 25°C	-5		+5	%	1
	CLK_SEL = 1,2,3,4,5 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL = 0,6 or gyro inactive	-10		+10	%	1
	CLK_SEL = 1,2,3,4,5 and gyro active		±1		%	1

Table 3. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.

3.2.3 Other Electrical Specifications

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization		100 ±10%		kHz	1
	High Speed Characterization		1	7	MHz	1, 2
SPI Modes			Modes 0 and 3			
I^2C Operating Frequency	All registers, Fast-mode			400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 4. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 7-MHz operation.

3.3 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

Parameters	Conditions	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING	**I²C FAST-MODE**					
f_{SCL}, SCL Clock Frequency				400	kHz	1
$t_{HD.STA}$, (Repeated) START Condition Hold Time		0.6			µs	1
t_{LOW}, SCL Low Period		1.3			µs	1
t_{HIGH}, SCL High Period		0.6			µs	1
$t_{SU.STA}$, Repeated START Condition Setup Time		0.6			µs	1
$t_{HD.DAT}$, SDA Data Hold Time		0			µs	1
$t_{SU.DAT}$, SDA Data Setup Time		100			ns	1
t_r, SDA and SCL Rise Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
t_f, SDA and SCL Fall Time	C_b bus cap. from 10 to 400 pF	20+0.1C_b		300	ns	1
$t_{SU.STO}$, STOP Condition Setup Time		0.6			µs	1
t_{BUF}, Bus Free Time Between STOP and START Condition		1.3			µs	1
C_b, Capacitive Load for each Bus Line			< 400		pF	1
$t_{VD.DAT}$, Data Valid Time				0.9	µs	1
$t_{VD.ACK}$, Data Valid Acknowledge Time				0.9	µs	1

Table 5. I²C Timing Characteristics

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.

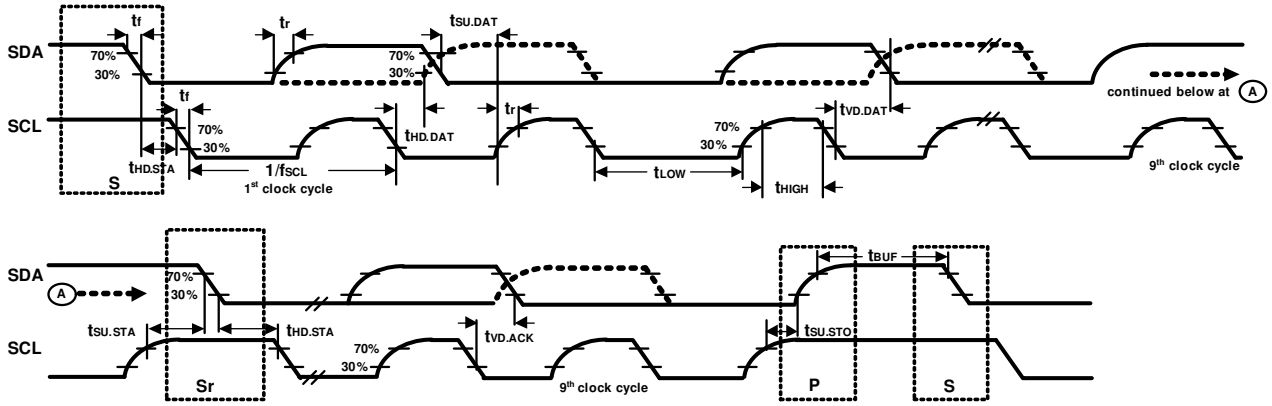


Figure 1. I²C Bus Timing Diagram

3.4 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section 0, VDD = 1.8 V, VDDIO = 1.8 V, T_A = 25°C, unless otherwise noted.

Parameters	Conditions	MIN	TYP	MAX	UNITS	NOTES
SPI TIMING						
f_{SCLK}, SCLK Clock Frequency				7	MHz	
t_{LOW}, SCLK Low Period		64			ns	
t_{HIGH}, SCLK High Period		64			ns	
$t_{SU.CS}$, CS Setup Time		8			ns	
$t_{HD.CS}$, CS Hold Time		500			ns	
$t_{SU.SDI}$, SDI Setup Time		5			ns	
$t_{HD.SDI}$, SDI Hold Time		7			ns	
$t_{VD.SDO}$, SDO Valid Time	C_{load} = 20pF			59	ns	
$t_{HD.SDO}$, SDO Hold Time	C_{load} = 20pF	6			ns	
$t_{DIS.SDO}$, SDO Output Disable Time				50	ns	

Table 6. SPI Timing Characteristics (7 MHz Operation)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets.

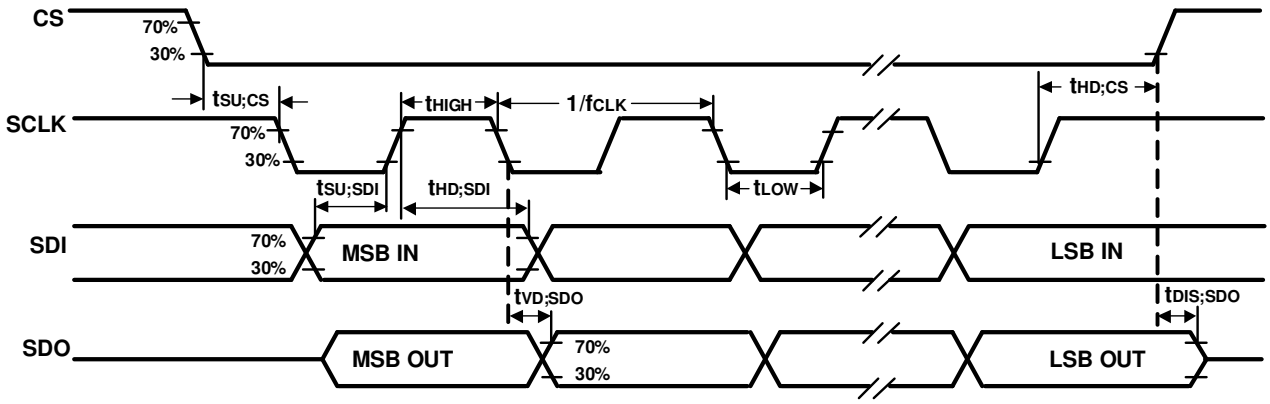


Figure 2. SPI Bus Timing Diagram

3.5 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

Parameter	Rating
Supply Voltage, VDD	-0.5 V to +4 V
Supply Voltage, VDDIO	-0.5 V to +4 V
REGOUT	-0.5 V to 2 V
Input Voltage Level (SA0, FSYNC, SCL, SDA)	-0.5 V to VDD + 0.5 V
Acceleration (Any Axis, unpowered)	10,000g for 0.2 ms
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 250 V (MM)
Latch-up	JEDEC Class II (2),125°C ±100 mA

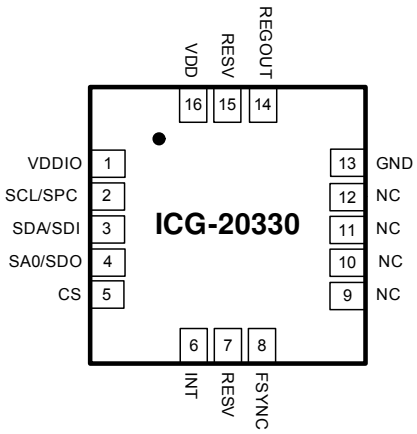
Table 7. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

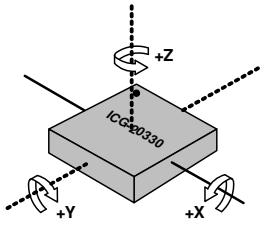
4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

Pin Number	Pin Name	Pin Description
1	VDDIO	Digital I/O supply voltage
2	SCL/SPC	I^2C serial clock (SCL); SPI serial clock (SPC)
3	SDA/SDI	I^2C serial data (SDA); SPI serial data input (SDI)
4	SA0/SDO	I^2C slave address LSB (SA0); SPI serial data output (SDO)
5	CS	Chip select (0 = SPI mode; 1 = I^2C mode)
6	INT	Interrupt digital output (totem pole or open-drain)
7	RESV	Reserved. Do not connect.
8	FSYNC	Synchronization digital input (optional). Connect to GND if unused.
9	NC	Connect to GND or do not connect
10	NC	Connect to GND or do not connect
11	NC	Connect to GND or do not connect
12	NC	Connect to GND or do not connect
13	GND	Connect to GND
14	REGOUT	Regulator filter capacitor connection
15	RESV	Reserved. Connect to GND
16	VDD	Power Supply

Table 8. Signal Descriptions



LGA Package (Top View)
16-pin, 3 mm x 3 mm x 0.75 mm
Typical Footprint and thickness



Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin-out Diagram for ICG-20330 3.0x3.0x0.75 mm LGA

4.2 TYPICAL OPERATING CIRCUIT

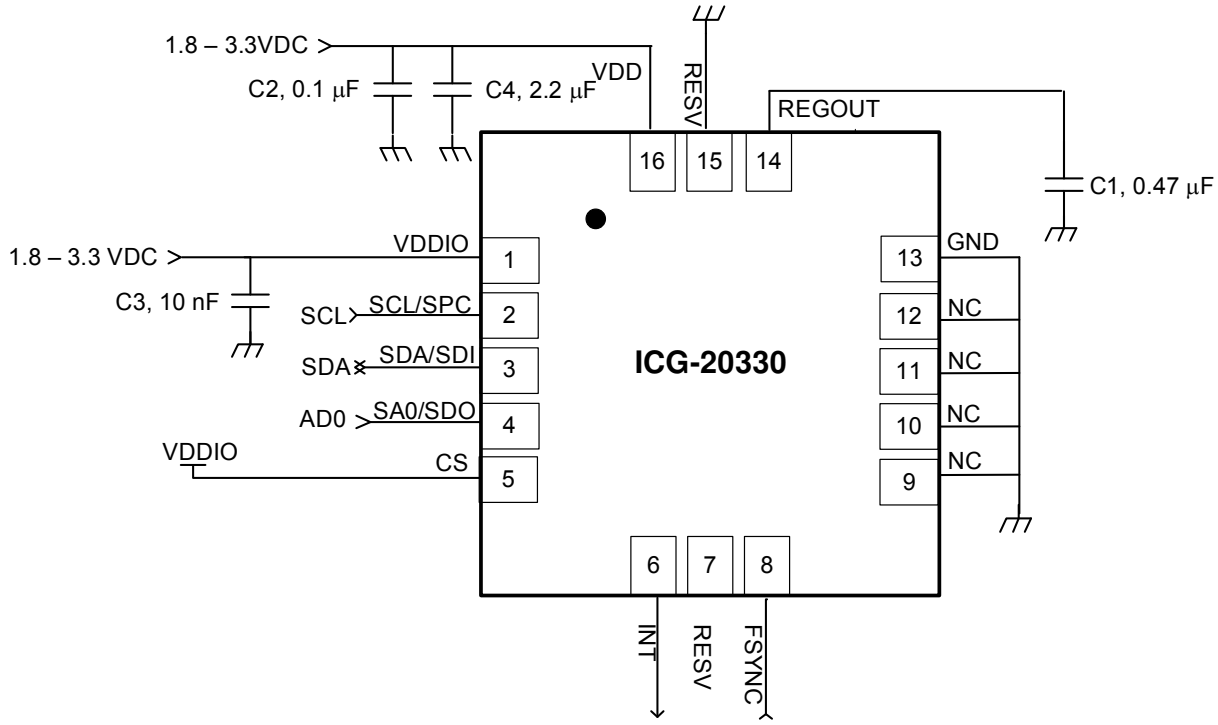


Figure 4. ICG-20330 LGA Application Schematic

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

Component	Label	Specification	Quantity
REGOUT Capacitor	C1	Ceramic, X7R, 0.47 µF ±10%, 2 V	1
VDD Bypass Capacitors	C2	Ceramic, X7R, 0.1 µF ±10%, 4 V	1
	C4	Ceramic, X7R, 2.2 µF ±10%, 4 V	1
VDDIO Bypass Capacitor	C3	Ceramic, X7R, 10 nF ±10%, 4 V	1

Table 9. Bill of Materials

4.4 BLOCK DIAGRAM

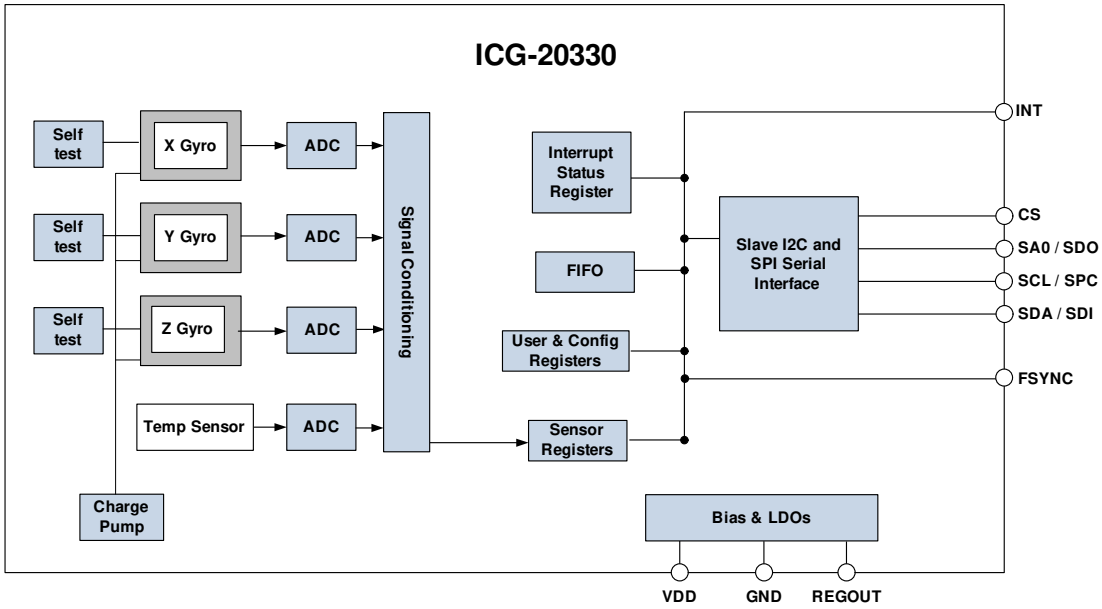


Figure 5. ICG-20330 Block Diagram

4.5 OVERVIEW

The ICG-20330 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Primary I^2C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICG-20330 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ±31.25, ±62.5, ±125 and ±250 degrees per second (dps). The ADC sample rate is programmable up to 8,000 samples per second with user-selectable low-pass filters that enable a wide range of cut-off frequencies.

4.7 I²C AND SPI SERIAL COMMUNICATIONS INTERFACES

The ICG-20330 communicates to a system processor using either a SPI or an I²C serial interface. The ICG-20330 always acts as a slave when communicating to the system processor. The LSB of the I²C slave address is set by pin 4 (SA0).

4.7.1 ICG-20330 Solution Using I²C Interface

In the figure below, the system processor is an I²C master to the ICG-20330.

Figure 6. ICG-20330 Solution Using I²C Interface

4.7.2 ICG-20330 Solution Using SPI Interface

In the figure below, the system processor is an SPI master to the ICG-20330. Pins 2, 3, 4, and 5 are used to support the SPC, SDI, SDO, and CS signals for SPI communications.

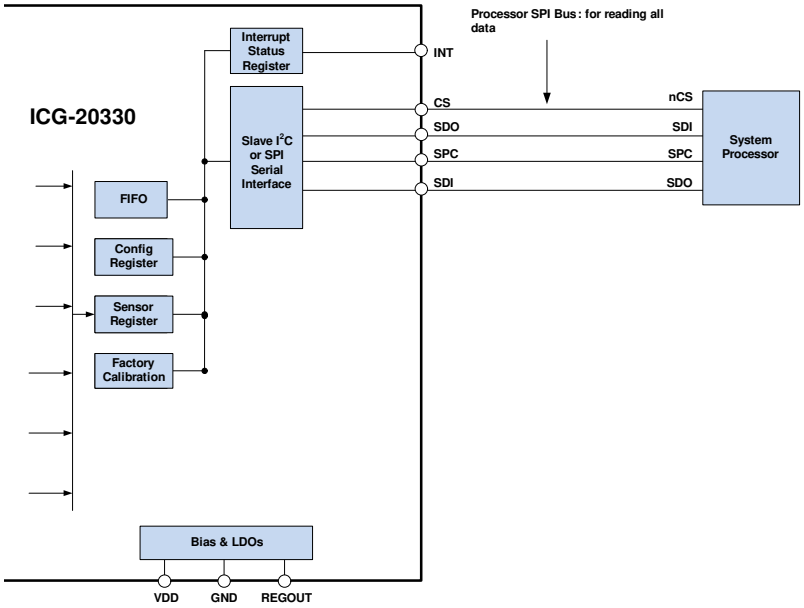


Figure 7. ICG-20330 Solution Using SPI Interface

4.8 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope self-test registers (registers 27 and 28).

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

Self-test response = Sensor output with self-test enabled – Sensor output with self-test disabled

The self-test response for each gyroscope axis is defined in the gyroscope specification table.

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test. It is recommended to use InvenSense MotionApps software for executing self-test.

For further information on Self-Test, please refer to the register map of ICG-20330.

4.9 CLOCKING

The ICG-20330 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

a) An internal relaxation oscillator
b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.10 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.11 FIFO

The ICG-20330 contains a 512-byte FIFO register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data and temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

For further information regarding the FIFO, please refer to the register map of ICG-20330.

4.12 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT pin configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.13 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICG-20330 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.14 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICG-20330. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.15 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.16 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICG-20330.

Mode	Name	Gyro
1	Sleep Mode	Off
2	Standby Mode	Drive On

Table 10. Standard Power Modes for ICG-20330

Notes:

1. Power consumption for individual modes can be found in section 0.

5 PROGRAMMABLE INTERRUPTS

The ICG-20330 has a programmable interrupt system which can generate an interrupt signal on the INT pin. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually.

Interrupt Name	Module
FIFO Overflow	FIFO
Data Ready	Sensor Registers

Table 11. Table of Interrupt Sources

For information regarding the interrupt enable/disable registers and flag registers, please refer to the register map of ICG-20330 in this document.

6 DIGITAL INTERFACE

6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICG-20330 can be accessed using either I²C at 400 kHz or SPI at 7 MHz. SPI operates in four-wire mode.

Pin Number	Pin Name	Pin Description
1	VDDIO	Digital I/O supply voltage.
4	SA0 / SDO	I²C Slave Address LSB (SA0); SPI serial data output (SDO)
2	SCL / SPC	I²C serial clock (SCL); SPI serial clock (SPC)
3	SDA / SDI	I²C serial data (SDA); SPI serial data input (SDI)

Table 12. Serial Interface

Note:

To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the "Start-Up Time for Register Read/Write" in Section 6.3.

For further information regarding the *I2C_IF_DIS* bit, please refer to the register map of ICG-20330.

6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICG-20330 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICG-20330 is b110100X which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin SA0. This allows two ICG-20330s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin SA0 is logic low) and the address of the other should be b1101001 (pin SA0 is logic high).

6.3 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

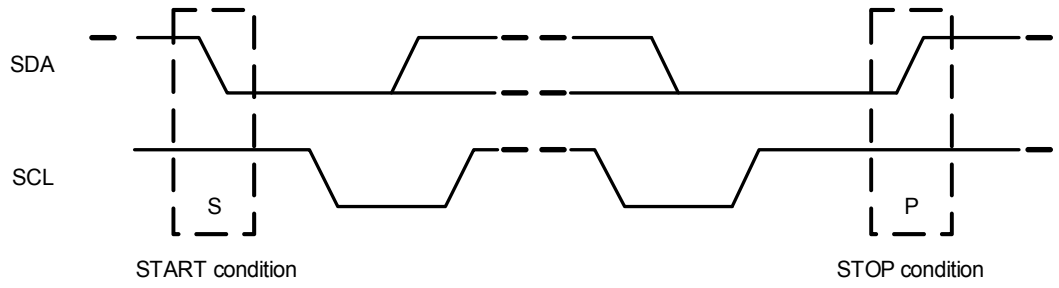


Figure 8. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8 bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

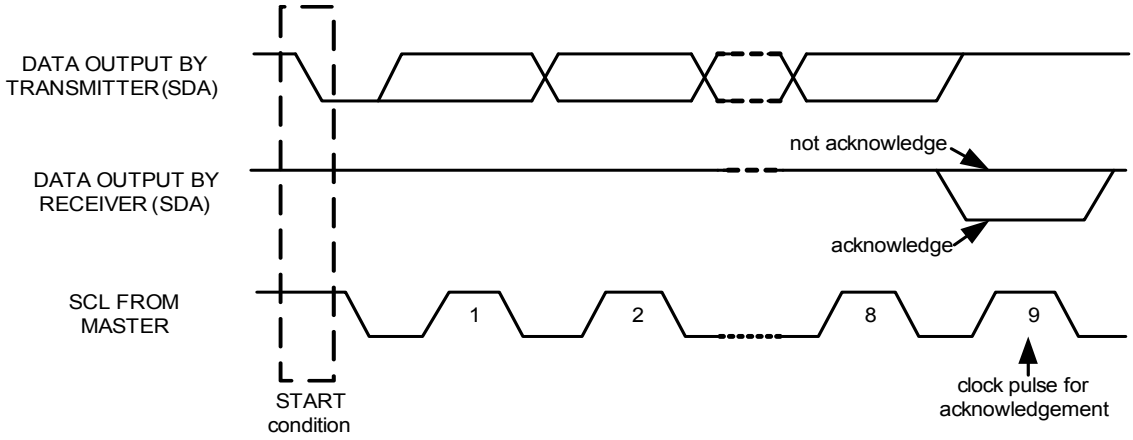


Figure 9. Acknowledge on the I²C Bus