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ICL5102 resonant controller IC 2nd generation with PFC for power supply and lighting drivers

Features

- 1.3MHz Maximum Soft Start Frequency
- 500kHz adjustable RUN Frequency
- Integrated PFC and HB controllers
- Supports universal input ($90V_{AC}$ to $305V_{AC}$) and wide output range
- Low count of external components supporting small form factors and a cost efficient design
- All parameters set by simple resistors only
- Junction temperature Range -40°C to +150°C
- Fast startup < 300ms, $I_{Startup}$ < 100µA
- Power Factor Correction > 99%, THD < 5%
- High efficiency up to 94%
- Active BURST Mode with Power Limitation / low Standby < 300mW / can be disabled
- 3 Phase self-adapting Soft Start
- Brownout Detection
- Boundary mode operation during nominal load and WCM[1)] mode during low load down to 0.1%
- Improved THD compensation
- Adjustable PFC current limitation
- Fully integrated 650V high-side driver
- Self-adaptive dead time 250ns – 750ns
- Detection of capacitive operation, overload, short circuit, output over voltage OVP & hot spot over temperature via NTC, Surge protection using in all cases Auto Restart

Potential Applications

- Offline AC-DC Power Supply, LCD TV, Adapter
- LED driver, e.g. commercial or residential lighting systems
- Integrated electronic control gear for LED luminaires

Product Validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22

1) WCM = Wait Cycle Mode = THD optimized DCM

Product Type	Package
ICL5102 51 – 100	PG-DSO-16

Description

The resonant controller ICL5102 is designed to control resonant converter topologies. The PFC stage operates in Boundary Mode and WCM mode, supporting low load conditions. Integrated high and low side drivers assure a low count of external components, enabling small form factor designs.

ICL5102 parameters are adjusted by simple resistors only, this being the ideal choice to ease the design-in process. A comprehensive set of protection features using auto restart ensures that the controller detects fault conditions, protecting both drivers and load. Figure 1 shows a typical application.

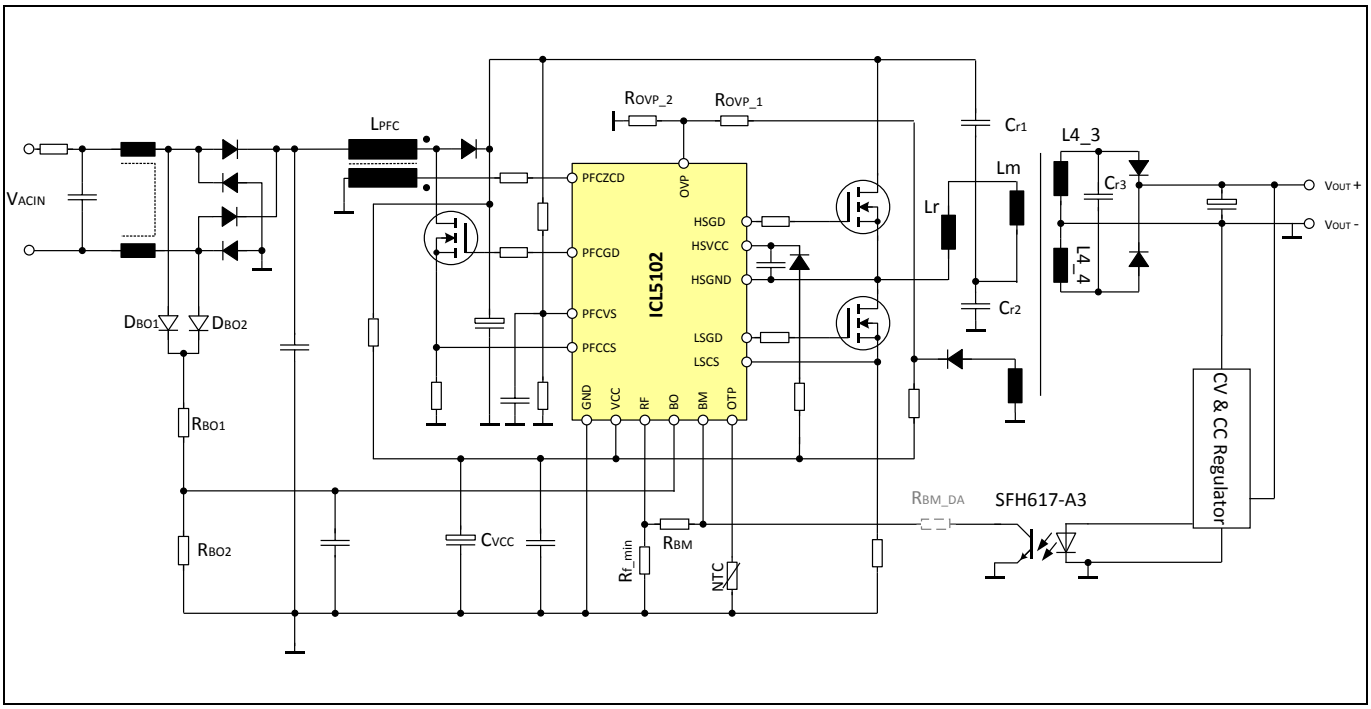

Figure 1 Generic LCC Application

Table of Contents

1 Pin Configuration and Description

The pin configuration is shown in Figure 2 PG-DSO-16 Package

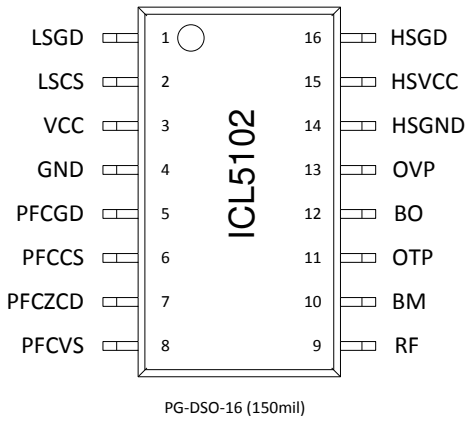

Figure 2 Pin Configuration

1.1 PIN Configuration for PG-DSO-16

Table 1

Symbol	Pin	Function
LSGD	1	Low-side gate drive
LSCS	2	Low-side current sense signal
VCC	3	Low-side chip supply voltage
GND	4	IC GND
PFCGD	5	PFC gate drive
PFCCS	6	PFC current sense signal
PFCZCD	7	PFC zero crossing detection / THD Optimzation
PFCVS	8	PFC voltage sensing
RF	9	RUN frequency setting
BM	10	Burst mode setting
OTP	11	Over Temperature protection
BO	12	Brown out detection
OVP	13	Overvoltage protection
HSGND	14	High-side GND
HSVCC	15	High-side supply voltage
HSGD	16	High-side gate drive

1.2 PIN Set-Up

The PIN set-up of ICL5102 for a typical PFC / LLC converter is shown in Figure 3.

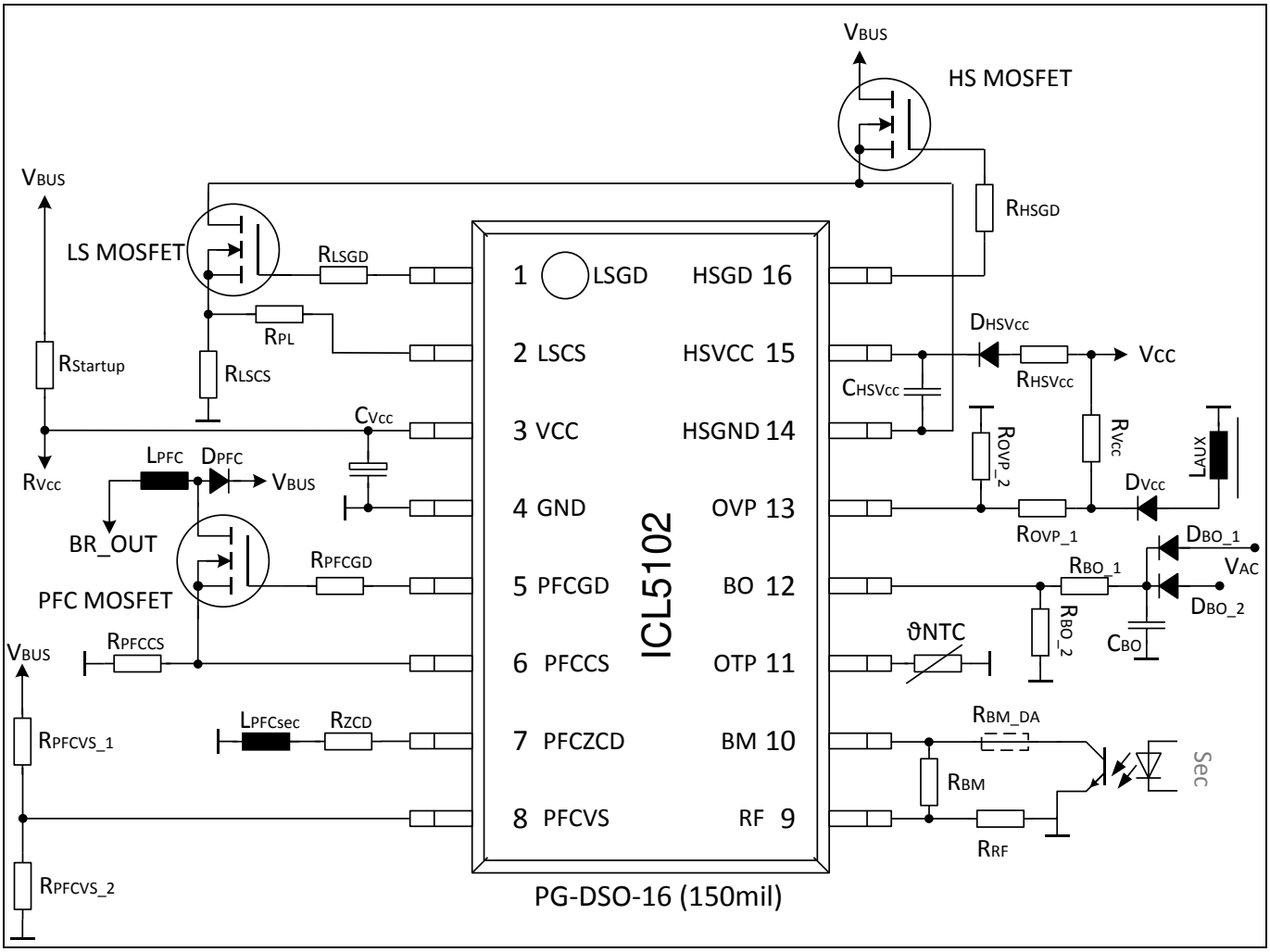

Figure 3 PIN Set-Up

1.3 PIN Functionality

Table 2 Pin Definitions and Function

Symbol	Pin	Function
LSGD	1	**Low-Side Gate Drive** The gate of the low-side MOSFET in a resonant inverter topology is controlled by this pin. The drivers of the ICL5102 are in voltage mode. There is an active low level during UVLO (under voltage lockout) and a limitation of the max high level at 11.0V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate voltage rises typically within 275ns from low level to high level. The rising time limits the driver current. The source current (here negative) and the maximum high level defining the MOSFET capacitance The fall time of the gate voltage is less than 50 ns in order to turn off quickly. This measure produces different switching speeds during turn-on and turn-off as it is usually achieved with a diode parallel to a resistor in the gate drive loop. It is recommended to use a resistor of typically 22Ω between the drive pin and gate in order to avoid oscillations.The maximum gate capacitance should not exceed Cg = 1.8nF. The dead time between the LSGD signal and HSGD signal is self-adapting between 250ns and 750ns. The pin is protected against negative voltage when switched to low.
LSCS	2	**Low-Side Current Sense Signal** This pin is connected via a serial resistor to the shunt, which is located between the source terminal of the low-side MOSFET of the inverter and ground. Internal clamping structures and filtering measures allow sensing of the source current for the low side inverter MOSFET without additional filter components. There is a first threshold of 0.8V sensed during each ½ cycle. If this threshold is reached, the over current control increases the frequency until the signal is below 0.8V. If this signal is present for longer than 50ms, the controller powers down and auto restarts the system. If the sensed current signal exceeds a second threshold of 1.6V for longer than 500ns, the IC stops the half bridge MOSFETs. There are further thresholds active at this pin to detect capacitive mode operation. A voltage level below -50mV in the second half of the LSGD ON indicates faulty operation (operation below resonance). The 1.6V threshold senses even short over currents during turn-on of the high-side MOSFET as typical for reverse recovery currents of a diode. If one of these comparator thresholds indicates incorrect operating conditions for longer than 620µs the IC turns off the gates and changes to fault mode due to detected capacitive mode operation. See chapter 2.6 The threshold of -50mV is also used to adjust the dead time between turn-off and turn-on of the resonant drivers in a range of 250ns to 750ns during all operating modes. See chapter 2.8 The capacitive load regulation will be active if the threshold of +50mV is reached within the first 7 % of the period. In order to prevent a capacitive switching operation, the controller increases the frequency until the area of capacitive switching is left. See chapter 2.6

VCC	3	**Low-Side Chip Supply Voltage** This pin provides the power supply of the ground-related section of the IC. There is a turn-on threshold at typ. 16.0V and an UVLO threshold at typ. 9.0V. The upper supply voltage limit is $V_{CCabsmax}$ = 18.5V. There is an internal VCC clamping at 16.3V (at I_{VCC} = 2mA typically). The maximum Zener current is internally limited to 5mA. The clamping is only active after startup; this ensures a safe start up. An external Zener diode is required for higher current levels. Current consumption during UVLO and during fault mode is less than typ. 80 µA. A ceramic capacitor close to the supply and GND pin is required in order to act as a low-impedance power source for gate drive and logic signal currents. For external Vcc supply make sure, that UVLO is possible. Due to the extended V_{CC} = 18.5V, for the initial Start Up, a 17V Zener diode can be used due to the very low start up current see chapter 2.1
GND	4	**IC GND** This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate drive and sense signals.
PFCGD	5	**PFC Gate Drive** The gate of the MOSFET in the PFC pre-converter designed in boost topology is controlled by this pin. There is an active low level during UVLO and a limitation of the max high level at 11.0V during normal operation. In order to turn on the MOSFET softly (with a reduced di_{DRAIN}/dt), the gate drive voltage rises within 245ns from low level to high level. The rising time limits the driver current. The source current (here negative) and the maximum high level defining the MOSFET capacitance The fall time of the gate voltage is less than 50ns in order to turn off quickly. The maximum gate capacitance should not exceed Cg = 4nFThe PFC section of the IC controls a boost converter as a PFC pre-converter in wait cycle mode (WCM) and critical conduction mode (CrCM). Typically, the control starts with an initial on-time depending on the line input voltage sensed by the BO PIN. Gate drive pulses with a fixed on-time of typically 6.0µs at V_{BO} = 2.0V, increasing up to 24µs and with an off-time of 47µs. As soon as sufficient zero current detector (ZCD) signals are available, the operation mode changes from fixed frequency operation to operation with variable frequency. The PFC works in critical conduction mode operation (CrCM) when rated and/or medium load conditions are present. That means triangular-shaped currents in the boost converter choke without gaps and variable operating frequency. During very low load the operation mode switches into the wait cycle mode (WCM) – that means triangular-shaped currents in the boost converter choke with gaps when reaching the zero current level and variable operating frequency in order to avoid steps in the consumed line current. The Brown Out voltage sets the on-time depending on the line input voltage. The pin is protected against negative voltage when switched to low.
PFCCS	6	**PFC Current Sense Signal** The voltage drop across a shunt resistor located between the source of the PFC MOSFET and GND is sensed with this pin. If the level exceeds a threshold of 1.0V for longer than 200ns, the PFC gate drive is turned off until the zero current detector (ZCD) enables a new cycle.

PFCZCD	7	**PFC Zero Crossing Detection** This pin senses the current through the boost inductor. If this current becomes zero during the off-time of the PFC MOSFET, the controller initiates a new cycle. A resistor connected between the ZCD winding and PIN 7 limits the sink and source current of the sense pin when the voltage of the ZCD winding exceeds the internal clamping levels (typically 4.6V and -1.4V @ 2mA) of the IC. If the sensed voltage level of the ZCD winding is not sufficient (e.g. during start-up), an internal start-up timer will initiate a new cycle every 52µs after the turn-off of the PFC gate drive. The clamping current out of this pin during the on-time of the PFC MOSFET gives a measure for the momentary input voltage. When the latter is low i.e. close to line zero crossing, the on-time of the PFC MOSFET is enlarged. This helps to minimize gaps in the line current close to zero crossing of the line voltage and improves the THD (Total Harmonic Distortion) of the line current. Optimization of the THD is possible by adjusting the resistor between this pin and the ZCD winding to adapt the THD correction to the boost inductance and PFC MOSFET. In order to calculate this resistor use a zero crossing current in a range of I_{ZCD} = 500µA – 1.2mA depending on design.
PFCVS	8	**PFC Voltage Sensing** The intermediate circuit voltage (bus voltage) at the smoothing capacitor is sensed by a resistive divider at this pin. The internal reference voltage for the rated bus voltage is 2.5V. There are further thresholds at < 12.5% of the rated bus voltage for detection of open control loop, < 75% for detection of under voltage during start up. An over voltage is detected during power up if V_{BUS} is > 105%, > 109% and > 115%. The over voltage threshold operates with a hysteresis of 100mV (4% of the rated bus voltage). It is recommended to use a small capacitor between this pin and GND as a spike suppression filter. In run mode, PFC over voltage higher than 109% of rated level stops the PFC gate drive within 5µs. As soon as the bus voltage is less than 105% of the rated level, the gate drives are enabled again. If the PFC over voltage 115% lasts for longer than 50ms, an inverter over voltage is detected and turns off the inverter gate drives, too.
RF	9	**Set minimum RUN Frequency** A resistor from this pin to ground sets the minimum operating frequency of the LLC / LCC inverter. This frequency limits the maximum output power. The combination of RRF and RBM sets the nominal frequency. This frequency must be lower than the expected run frequency during nominal load condition. The run frequency range is 20kHz to 500kHz. How to calculate the resistors see chapter 2.3.
BM	10	**Burst Mode** In order to achieve very low standby power consumption the ICL5102 has an integrated active burst mode. Active burst mode means, that the IC can leave the burst mode any time based on 4 different burst mode exit conditions. A resistor R_{BM} from pin 10 (BM) to RF (PIN 9) sets the max operating frequency when the IC should enter the burst mode depending on the load situation. Furthermore, it is possible disable burst mode by setting a resistor R_{BM_DA} from the opto coupler to BM PIN 10. How to calculate the resistor R_{RF} and R_{BM} see chapter 2.3 and 2.4. **During burst mode** the IC drives the BM pin as an output to generate the soft start ramp and soft on / soft off.

OTP	11	**Over Temperature Protection** The Over Temperature protection detects the temperature via an external NTC temperature sensor located on the PCB. If the voltage VOTP1 is < 703mV during start-up, the controller prevents a power up. If the voltage at pin 11 drops below VOTP2 < 625mV during RUN or Burst Mode, the IC powers down and auto restarts when VOTP > 703mV. Delay in both cases is 620 µs, the typical current at this pin is IOTP = 100µA. In case of using OTP, set a parallel capacitor from the NTC to GND of max. 1nF. If this function is not in use, a 20k resistance can be connected from PIN 11 to GND.
BO	12	**Brown Out Detection** AC line lnput voltage feedforward to set the initial pulse time for the PFC during the very first START UP and the max on-time – depending on the line input voltage. Furthermore, the brown out pin sets the fixed PFC gate pulse width during Burst Mode depending on line input voltage. The voltage at this pin must be above V_{BO} = 1.4V during monitoring to enable a brown in. If the voltage at this pin drops below V_{BO} = 1.2V for longer than 50ms during operation, a brown out is detected and the controller powers down and auto restarts the internal system. Use a double rectifier and high ohm resistors for the voltage divider.
OVP	13	**Over Voltage Protection** The ICL5102 has an integrated precise and fast reacting output overvoltage protection by sensing the secondary side output at the transformer supply AUX winding after the rectifier diode. This protection can be enabled or disabled. If the voltage at this pin exceeds V_{OVP} = 2.5V for longer than 5µs during the start-up phase, the controller prevents a power up. In case the voltage at pin 13 exceeds during RUN or Burst Mode the V_{OVP} = 2.5V threshold for longer than 5µs, the IC powers down and restarts automatically. To disable this function, set this pin to IC GND.
HSGND	14	**High-Side GND** This pin is connected to the source terminal of the high-side MOSFET, which is also the output of the half bridge. This pin represents the floating ground level of the high-side driver and the high-side supply.
HSVCC	15	**High-Side Supply Voltage** This pin provides the power supply of the high-side section of the IC. An external capacitor between pins 14 and 15 acts as bootstrap capacitor, which has to be recharged cycle by cycle via a high-voltage diode from the low-side supply voltage during the on-time of the low-side MOSFET. An UVLO threshold with hysteresis enables the high-side section at 10.4V and disables it at 8.6V.
HSGD	16	**High Side Gate Drive** The gate of the high-side MOSFET in a resonant inverter topology is controlled by this pin. There is an active low level during UVLO and a limitation of the max high level at 11.0V during normal operation. The switching characteristics are the same as described for LSGD (pin 1). The rising time limits the driver current. The source current (here negative) and the maximum high level defining the MOSFET capacitance The maximum gate capacitance should not exceed Cg = 1.8nF. The dead time between the LSGD signal and HSGD signal is self-adapting between 250ns and 750ns (typically).

2 Feature Description

2.1 Start Up

The sequence of the start-up: the ICL5102 starts with PFC first (see Figure 4). After the PFC BUS voltage is exceeding the V_{PFCVS} = 75% threshold, the half bridge starts working. The time from the IC start-up is depending how fast the PFC BUS voltage is reaching the 75 % level (see Figure 31).

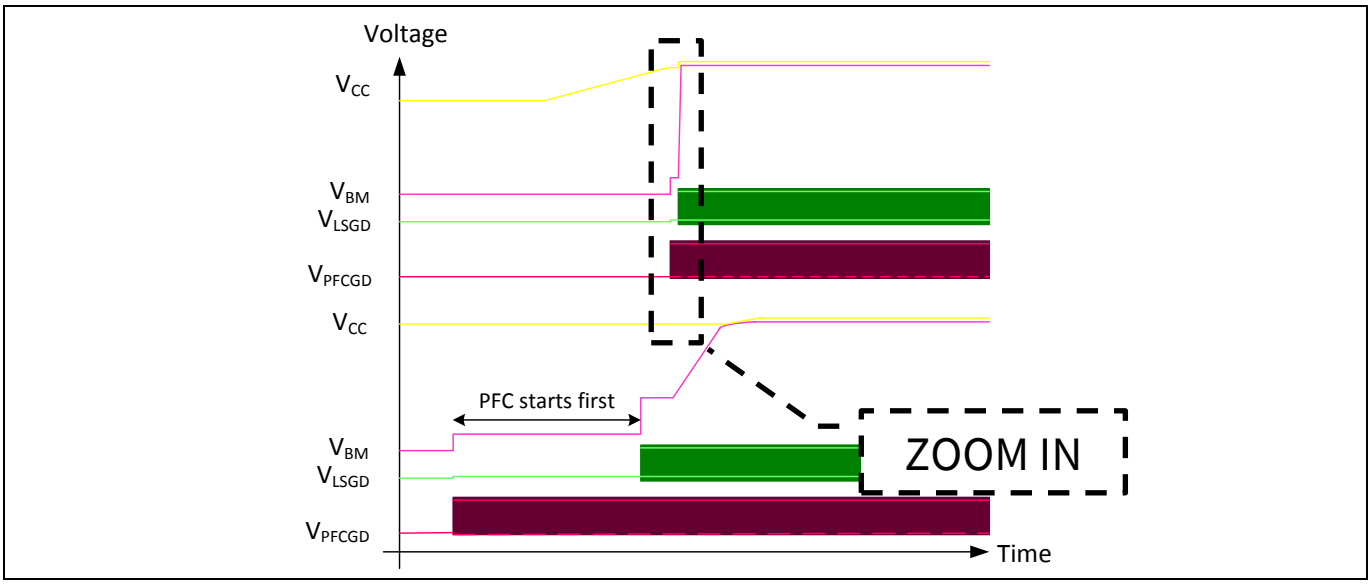

Figure 4 Start Up Sequence

2.2 Soft Start

The soft start consists of 3 subsequent states within a piecewise linear frequency ramp with a total minimum duration of t < 7ms. In case the LSCS peak voltage $V_{LSCSpeak}$ > 0.8V, the ICL5102 stops at the frequency of the frequency ramp and continues the frequency shift when $V_{LSCSpeak}$ < 0.8V.

The initial soft start frequency at line voltage first ON or at auto restart is:

$$f_{SoftStart} = 4*(f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 1: Initial Soft Start Frequency

During state 1 the frequency drops down within 624µs as in the followed equation:

$$f_{SS\_1} = 2.6*(f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 2: Soft Start Frequency in State 1

During state 2 the frequency ramps down to f_{MAX} within 2.5ms

$$f_{SS\_2} = f_{MAX}$$

Equation 3: Soft Start Frequency in State 2

During state 3 the frequency ramps down to f_{MIN} within 3.75ms

$$f_{SS\_3} = f_{MIN}$$

Equation 4: Soft Start Frequency in State 3

During state 1 and 2, the voltage at the BM pin is driven internally to V_{BM} = 0.75V. During state 3, the voltage at the BM pin ramps up from 0.75V up to 2.25V.
During soft start the voltage at the BM pin is driven by an internal ramp generator. This ramp generator can only sink current. Once the external opto-coupler takes away all current through the R_{BM} resistor from the ramp generator the soft start ends. The operational range for the maximum initial soft start frequency f_{InSS} is 1300kHz.

2.3 Frequency Setting

A Resonant Converter changes the frequency from a given minimum frequency fmin (full load, maximum power delivery) to a certain maximum frequency fmax that is reached at light load. The minimum frequency has to be chosen such that the converter doesn't enter capacitive switching under any load condition. The maximum frequency must not be too high in order to reduce switching losses and not compromise EMI.

In ICL5102 PIN RF delivers a constant voltage of V_{RF} = 2.5V. The current out of this pin defines the operating frequency, with a frequency to current ratio C_{FC} (typically 4.0 * 10^8 Hz/A). PIN BM is internally clamped to V_{BMmax} = 2.25V. The minimum and maximum frequencies f_{min} and f_{max} are set by the resistors R_{RF} and R_{BM} shown in the block diagram in Figure 6.

2.3.1 Maximum Frequency f_{MAX} of the ICL5102

The maximum RUN frequency f_{MAX} should not exceed the f_{RF5_MAX} as shown in chapter 5.5.3. The correlation between the user defined minimal frequency f_{MIN} and the absolute maximum working frequency f_{MAX} is given by:

2.3.1

$$f_{MAX} < 7 * f_{MIN}$$

Equation 5: Calculation of the maximum Frequency

2.3.2 Minimum Frequency f_{MIN} @ maximum Load

f_{MIN} is reached when the collector current of opto-coupler OC1 is 0µA and the whole current through R_{BM} flows into PIN BM. That means $V_{BM} = V_{BMmax}$ = 2.25V in this operating point.

$$f_{MIN} = C_{FC} * (I_{RF} + I_{RBM}) = C_{FC} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 2.25V}{R_{BM}})$$

Equation 6: Calculation of the minimum Frequency

2.3.3 Maximum Frequency f_{MAX} Before Entering Burst Mode

f_{MAX} is reached when the opto-coupler current is high enough to lower the voltage @ BM to 0.75V.

$$f_{MAX} = C_{FC} * (I_{RF} + I_{RBM}) = C_{FC} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 0.75V}{R_{BM}})$$

Equation 7: Calculation of the maximum Frequency

2.3.4 Calculation of R_{RF} and R_{BM}

In order to determine the values for R_{RF} and R_{BM} the frequencies fmin and fmax must be defined as mentioned above. Equations I and II can then be solved for R_{BM} and R_{RF}:

$$R_{BM} = C_{FC} * \frac{1.5V}{(f_{MAX} - f_{MIN})} = 4.0 * 10^8 \frac{Hz}{A} * \frac{1.5V}{(f_{MAX} - f_{MIN})}$$

$$R_{RF} = C_{FC} * \frac{15V}{(7 * f_{MIN} - f_{MAX})} = 4.0 * 10^8 \frac{Hz}{A} * \frac{15V}{(7 * f_{MIN} - f_{MAX})}$$

Equation 8: Calculation of R_{BM} and R_{RF}

2.3.5 Minimum typical Frequency versus Resistance

Figure 5 shows how to set the minimum RUN frequency via resistance from the RF pin to GND. Valid if no resistor to BM pin.

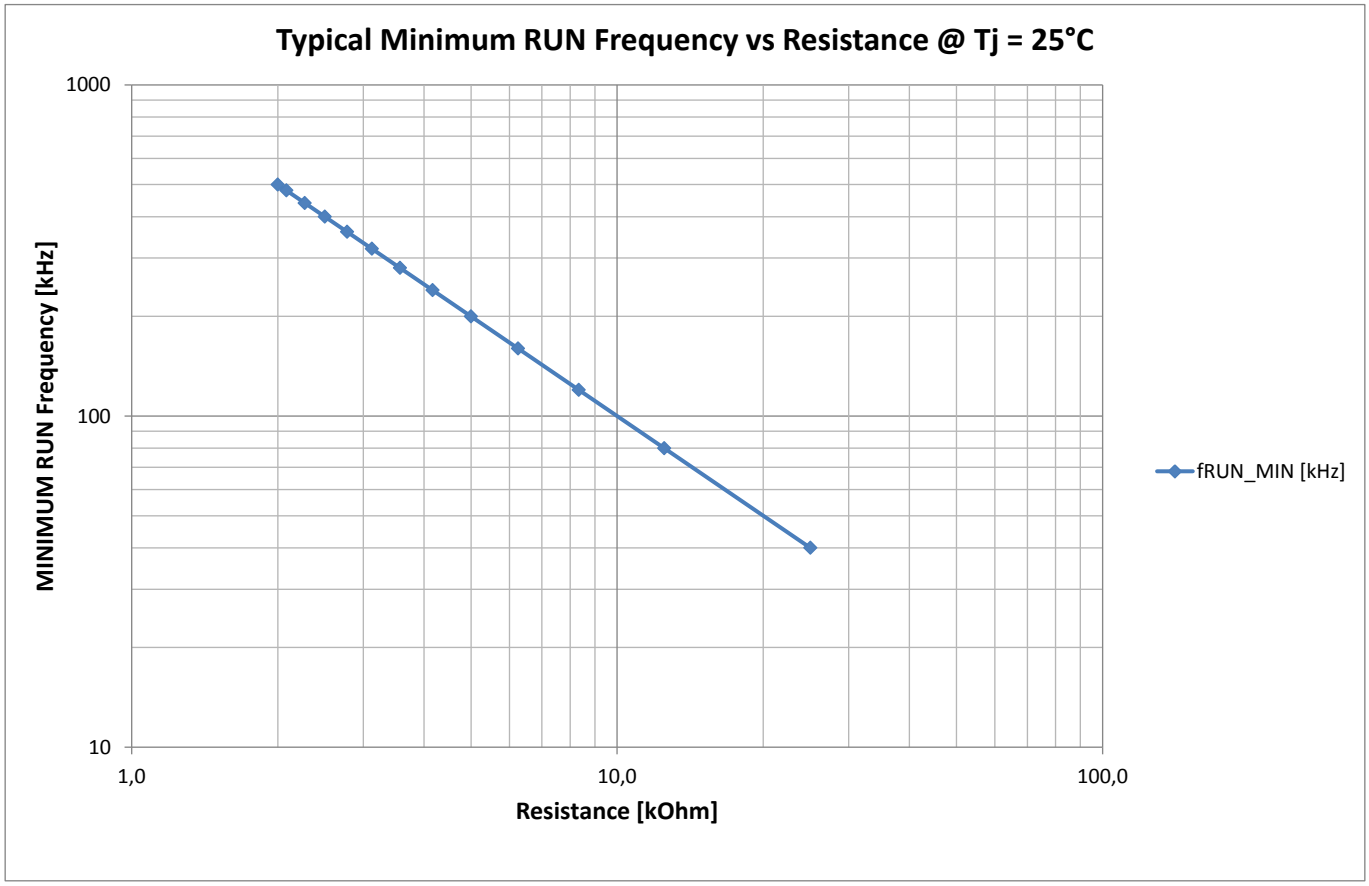

Figure 5 Typical Minimum RUN Frequency vs. Resistance @ Tj = 25°C

2.4 Burst Mode

2.4.1 Burst Mode Introduction

The ICL5102 burst mode is a one PIN concept made for lowest standby power during dimming, no load or µC to reach a STB < 300mW in an ultra-wide range design. The burst mode is self-adapting with an immediate response and covers each kind of load steps. The chip current consumption during Burst Mode is I_{VCC} ~ 1.5mA.

Dependent on the voltage at the BM PIN 10, the ICL5102 enters the Burst Mode, starts a burst pulse train, stops the pulse train or exits the burst mode operation in 4 different ways. The block diagram below shows the internal functionality of the burst mode operation. In order to regulate the power during the burst pulse train, a serial resistor R_{PL} from PIN 2 LSCS (see Figure 7) to the shunt resistor can be adjusted experimentally from 200Ω up to 1k depending on the application. Figure 6 shows the block diagram of the burst mode.

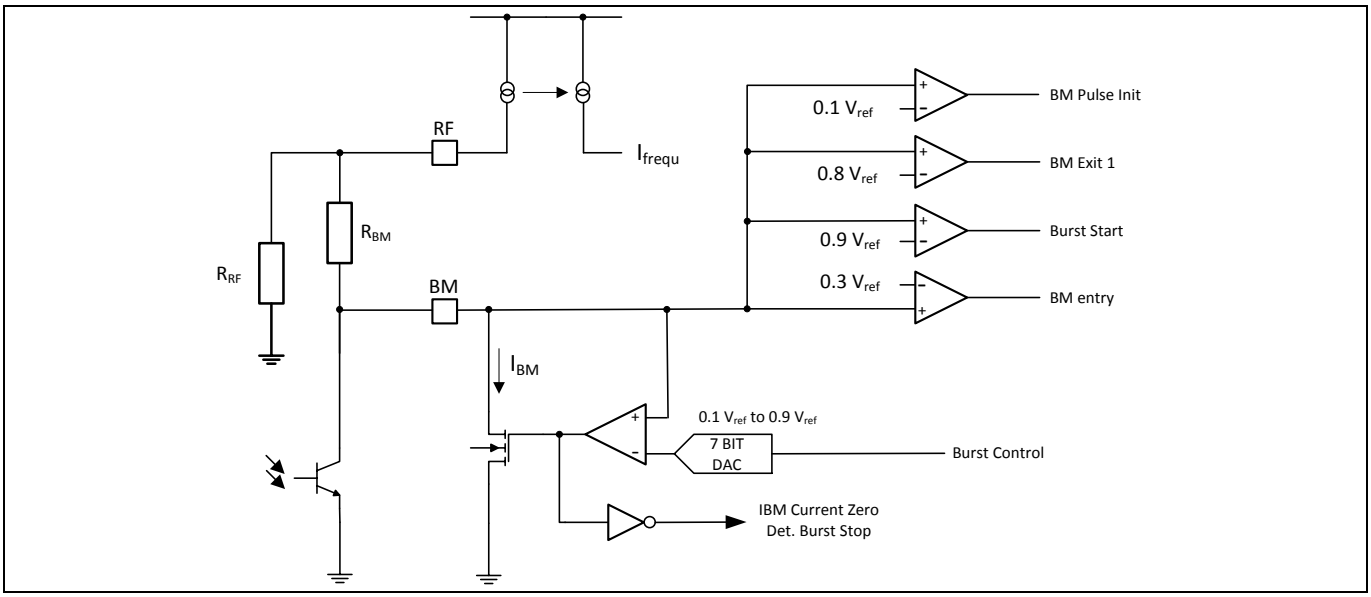

Figure 6 Burst Mode Block Diagram

Furthermore, a ceramic capacitor C_{Opt} at the opto-coupler should not exceed 2.2nF see Figure 7.

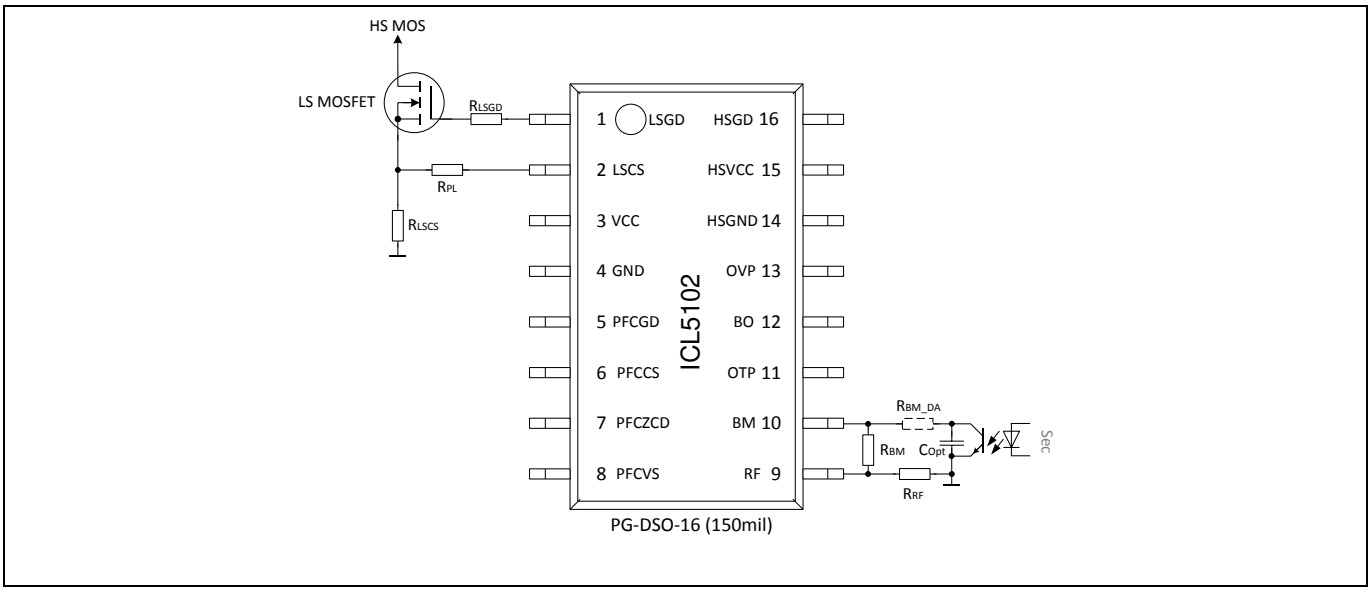

Figure 7 PIN Setup for Burst Mode Operation and Power Limitation during Burst Mode

2.4.2 Disable Burst Mode

If the voltage at the BM PIN 10 drops below V_{BM} = 0.75V for longer than 10ms, the burst mode will be entered. A serial resistor resistor R_{BM_DA} (see Figure 7 / calculated via Equation 9) between opto-coupler and BM PIN 10 prevents V_{BM} from going below 0.75V and the ICL5102 from entering burst mode – the burst mode function is disabled.

$$R_{BM\_DA} = \frac{3}{7} * R_{BM}$$

Equation 9: Calculation of R_{BM_DA}

2.4.3 Power Limitation during Burst Pulse

In order to help to prevent audible noise, the ICL5102 limits the power during burst pulse. Figure 8 shows the limitation of power during burst pulse. This can be easily adjusted by the resistor RPL connected to PIN 2 LSCS. This resistor also varies the burst mode pulse frequency.

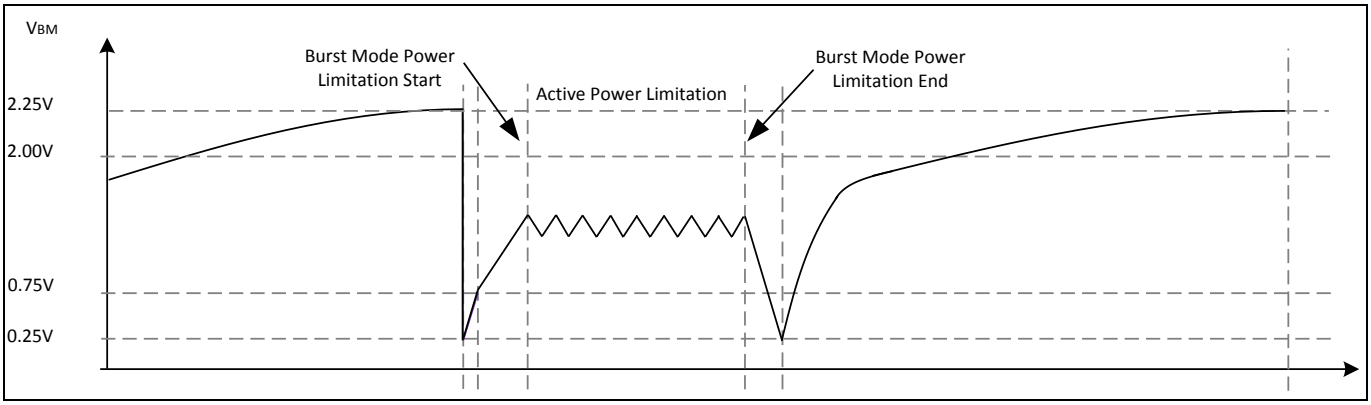

Figure 8 Active Power Limitation during Burst Pulse

2.4.4 Burst Mode Entry

In case of a low load condition, the ICL5102 increases the run frequency until reaching f_{MAX} see Equation 10, the burst mode voltage at the BM PIN 10 will drop below V_{BM} = 0.75V.

$$f_{MAX} = C_{FC} * (I_{RF} + I_{RBM}) = C_{FC} * (\frac{2.5V}{R_{RF}} + \frac{2.5V - 0.75V}{R_{BM}})$$

Equation 10: Calculation of the Maximum Frequency before entering the Burst Mode

If the voltage at the BM PIN 10 stays below V_{BM} = 0.75V for longer than t = 10ms, the ICL5102 enters the burst mode see Figure 9 (top). In this corridor, the IC increases further the frequency from f_{MAX} up to the soft off frequency $f_{SoftOFF}$ ($f_{SoftOFF} \geq f_{max}$) shown in Equation 11. This guarantees a smooth entry into the burst mode.

$$f_{SoftOFF} = \frac{4}{3} * (f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 11: Calculation of the Soft OFF Frequency

The ICL5102 starts with a burst sleep phase - all gate drives are off.

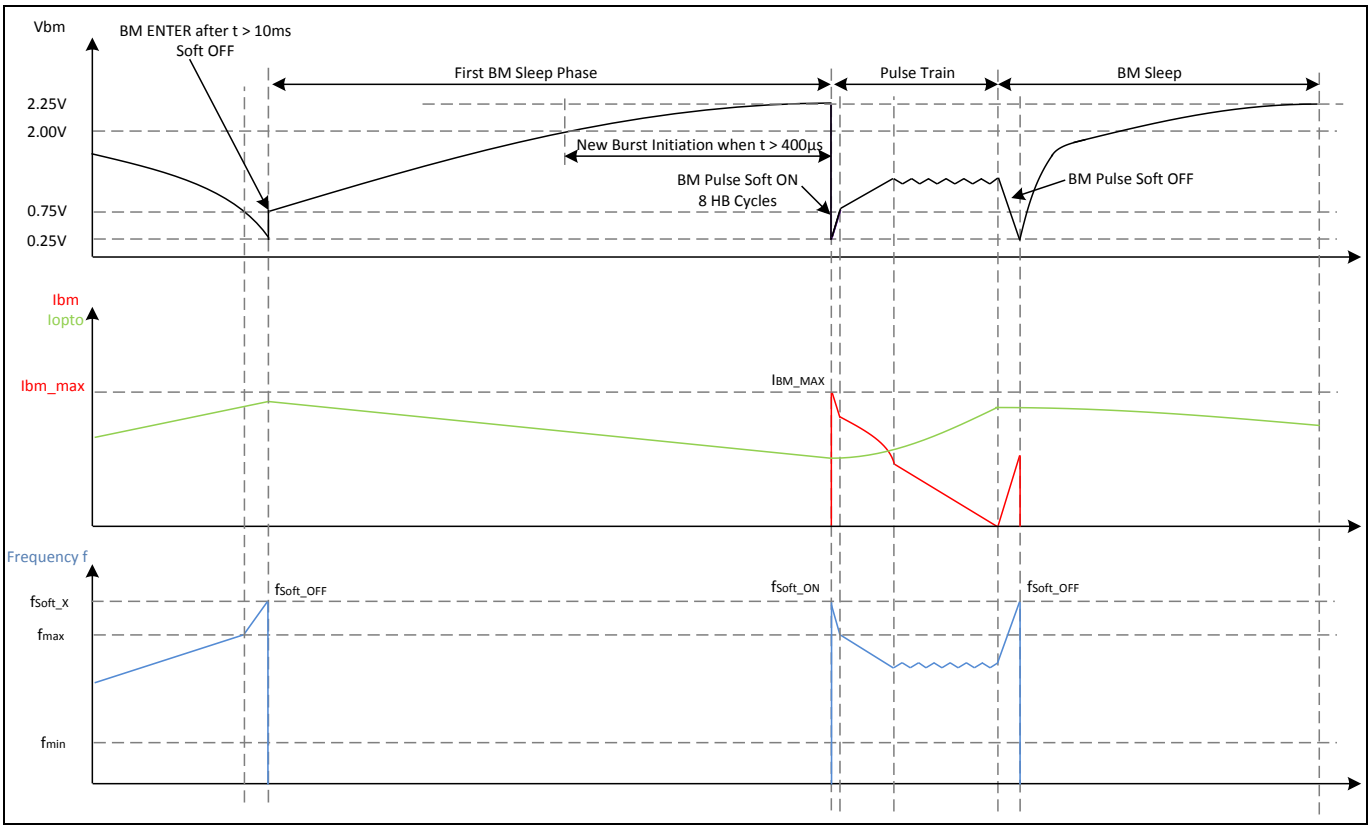

Figure 9 Burst Mode Entry

2.4.5 Burst ON (Pulse Train) – Voltage Mode Design

The burst pulse train starts with a higher frequency $f_{SoftON} > f_{max}$ in order to prevent noise or capacitive load operation. Determined by an internal counter, the frequency quickly ramps down to f_{max}. At the end of this ramp a second frequency ramp is reached and decreases the frequency to a stable value. The power will be controlled by the power limitation function of the burst mode. At the same time the current through the opto-coupler is monitored and when it reaches an internally defined value, a soft-off is initiated and the pulse train ends.

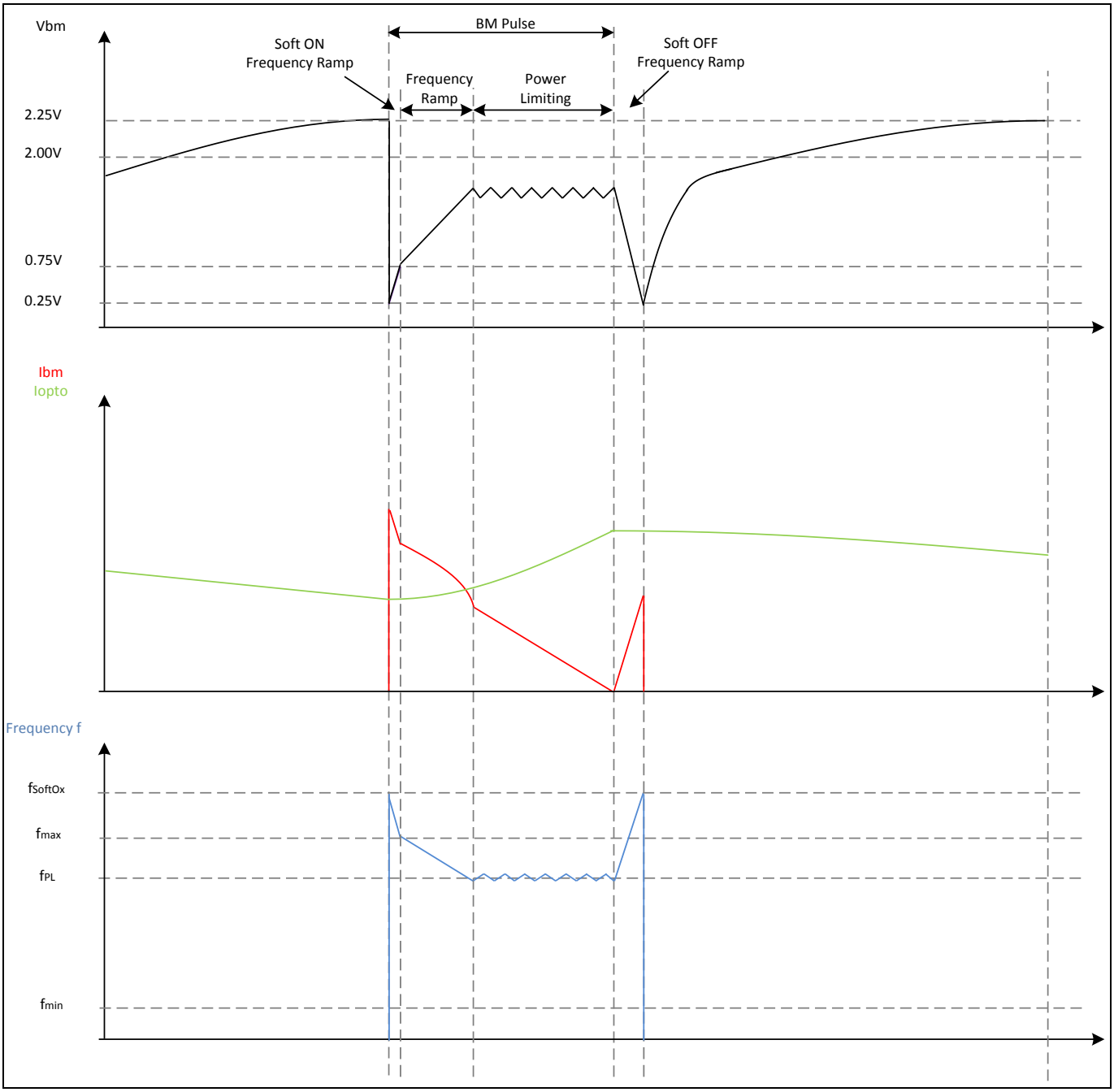

Figure 10 Pulse Train

2.4.6 Burst ON (Pulse Train) Phase I: SOFT ON (fixed)

Soft ON Start:

Soft ON will be activated when the voltage at the BM PIN drops to V_{BM} = 0.25V. During Soft ON Start, the frequency is internally set to:

$$f_{SoftON} = \frac{4}{3} * (f_{MAX} - f_{MIN}) + f_{MIN}$$

Equation 12: Calculation of the Soft ON Frequency

The internal burst mode current I_{BM} is at the highest level: I_{BM_MAX}.
Soft ON Phase:
During Soft ON phase, an internal Counter reduces the frequency from f_{SoftON} down to f_{MAX}. Also, the internal burst mode current decreases to a certain level.

Soft ON END
The end of soft on is initiated, when the voltage at the BM PIN reaches V_{BM} = 0.75V again.

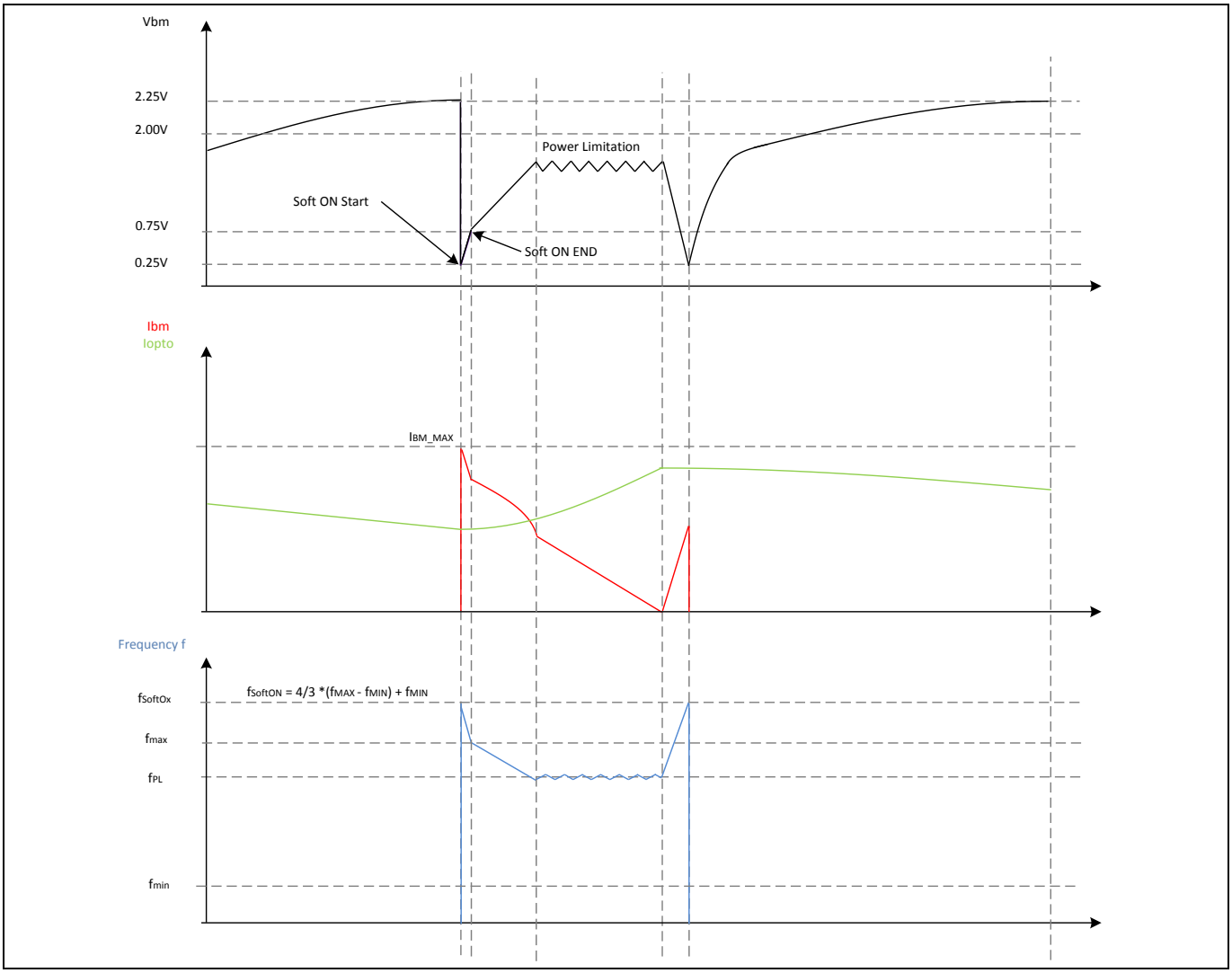

Figure 11 Pulse Train Soft ON

2.4.7 Burst ON (Pulse Train) Phase II: Frequency Ramp

The frequency reduces in order to reach the maximum power; the burst mode current I_{BM} decreases also from I_{BM_HIGH} to I_{BM}. Depending on an internal comparator result (see chapter 2.4.8), the frequency will decrease from f_{MAX} to f_{PL} and enters the next phase III (2.4.8).

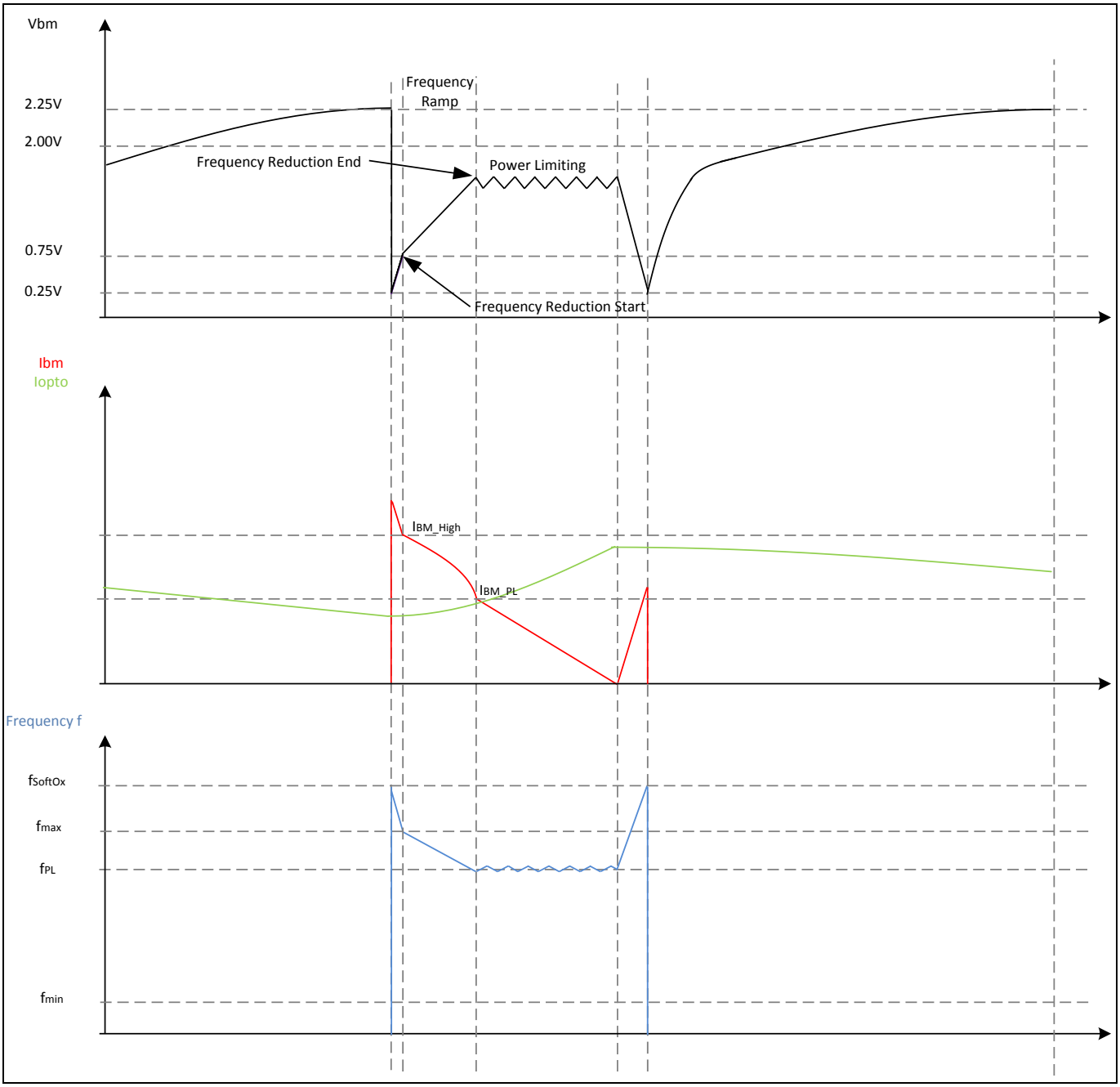

Figure 12 Pulse Train Frequency Ramp

2.4.8 Burst ON (Pulse Train) Phase III: Burst Pulse Power Limitation

After adjusting the frequency to the max power in phase II, the controller will hold a constant frequency with a regulation of the power shown in 2.4.7. The opto-coupler current increases, depending on the status of the output stage, and the burst mode sink current decreases from I_{BM_Low} to I_{BM} = 0µA. In the moment of I_{BM} = 0µA, the Pulse Train ends after a soft off frequency ramp back to f_{SoftON}.

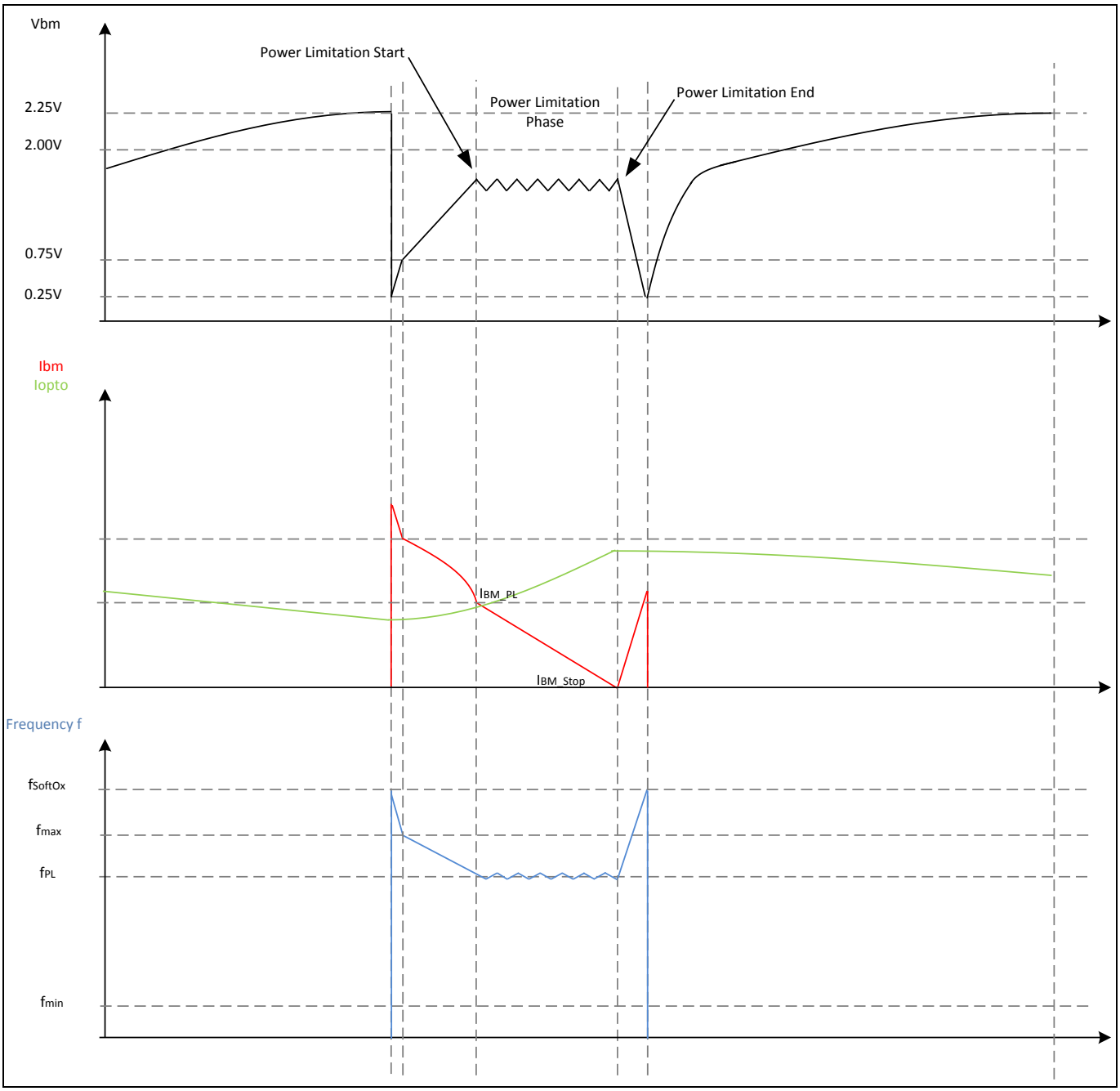

Figure 13 Pulse Train Power Limitation

In Phase III, a serial resistor R_{PL} (see Figure 14) from LSCS to the shunt will set the power limit during burst pulse. The value of this resistor should be between R_{PL} = 200Ω and 1k.

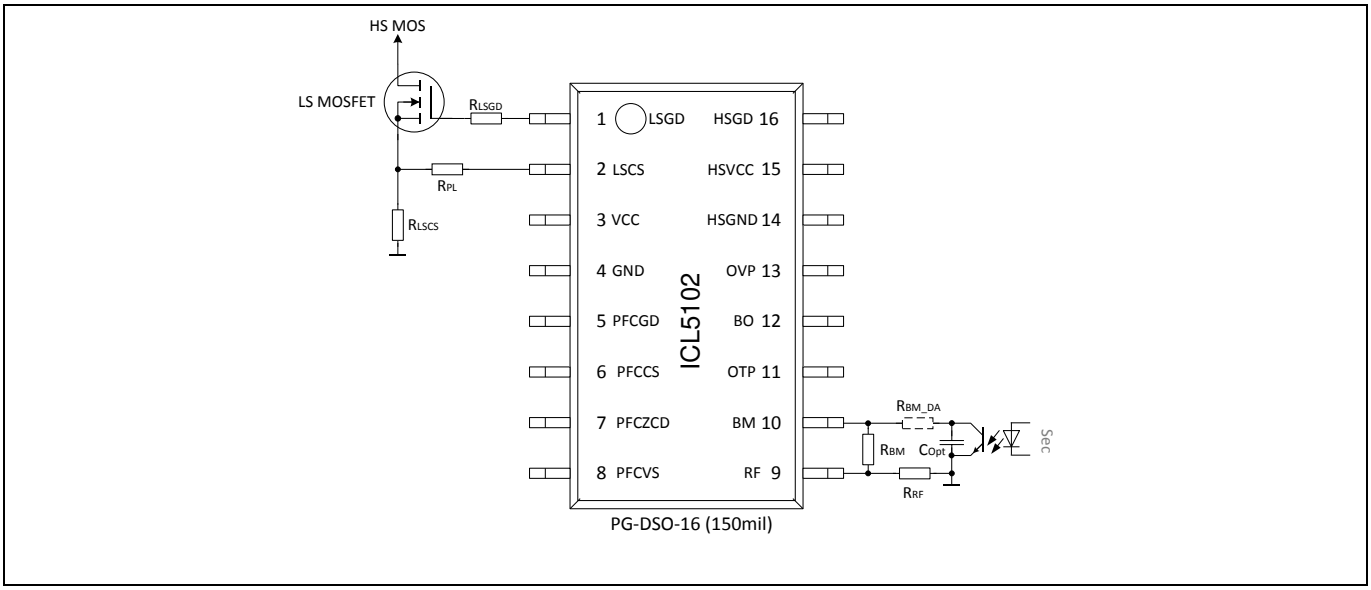

Figure 14 Power Limitation Resistance Setting R_{PL}

During burst pulse power regulation phase, an internal power limitation is active. The threshold of the power limitation can be set by the value of R_{PL} as shown in Figure 14. The voltage at the LSCS PIN will be integrated and compared internally with a 100µA signal see Figure 15.

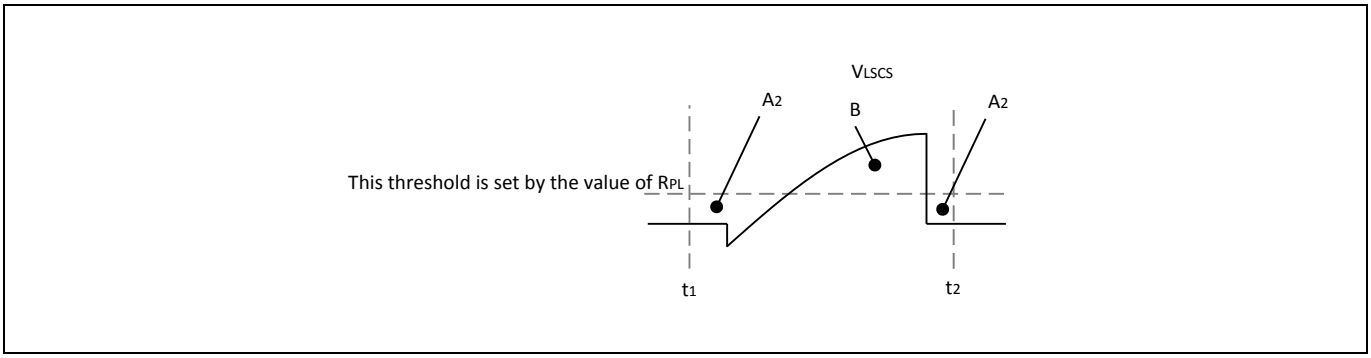

Figure 15 Low Side Current Sense Threshold for Power Limitation

If the area B is greater / less than the areas A1+A2 zero the power limiter increases / decreases the frequency at the same slope as the frequency ramp described in 2.4.7

2.5 Burst Mode EXIT

The ICL5102 Burst Mode Concept has 4 different EXIT conditions to jump out of the burst mode operation. The ICL5102 differentiates between 4 load steps conditions during: burst pulse, burst sleep, burst pulse timeout and high static load.

2.5.1 EXIT 1: Load Step during Burst OFF (Sleep)

The condition of exit 1 is a voltage increase from V_{BM} = 2.0V up to V_{BM} = 2.25V within t < 400µs caused due to a load step on the output stage.

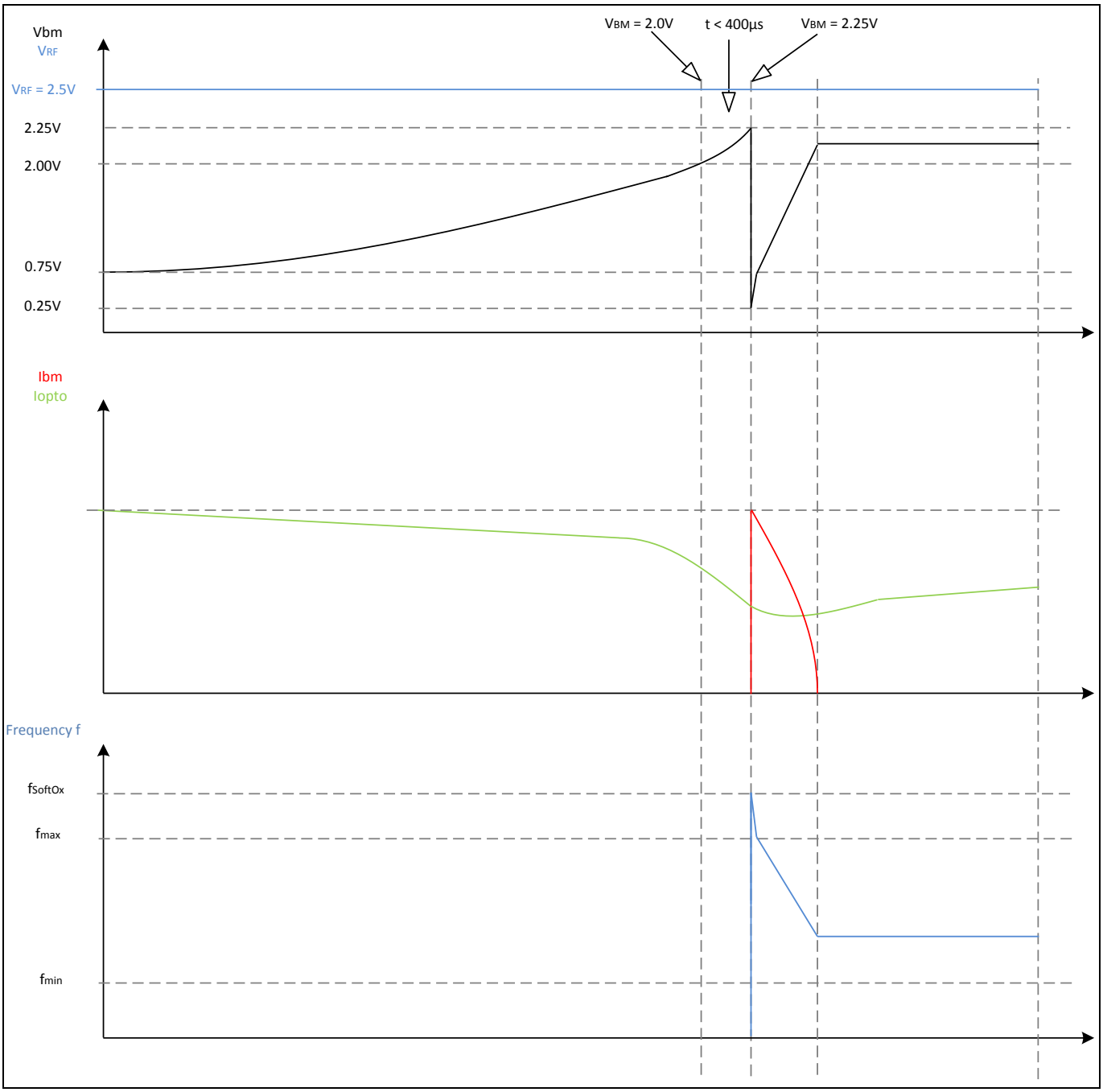

Figure 16 Burst Mode EXIT 1

2.5.2 EXIT 2: Load Step during Burst Pulse (Train)

If the BM – voltage increases ΔV_{BM} = + 100mV within 8 cycles, the ICL5102 detects a load step during burst pulse and exits the burst mode operation into normal mode. Background: in case of a load jump, the secondary voltage drops and changes the converters transfer ratio. In order to hold a constant power, the IC reduces the frequency.

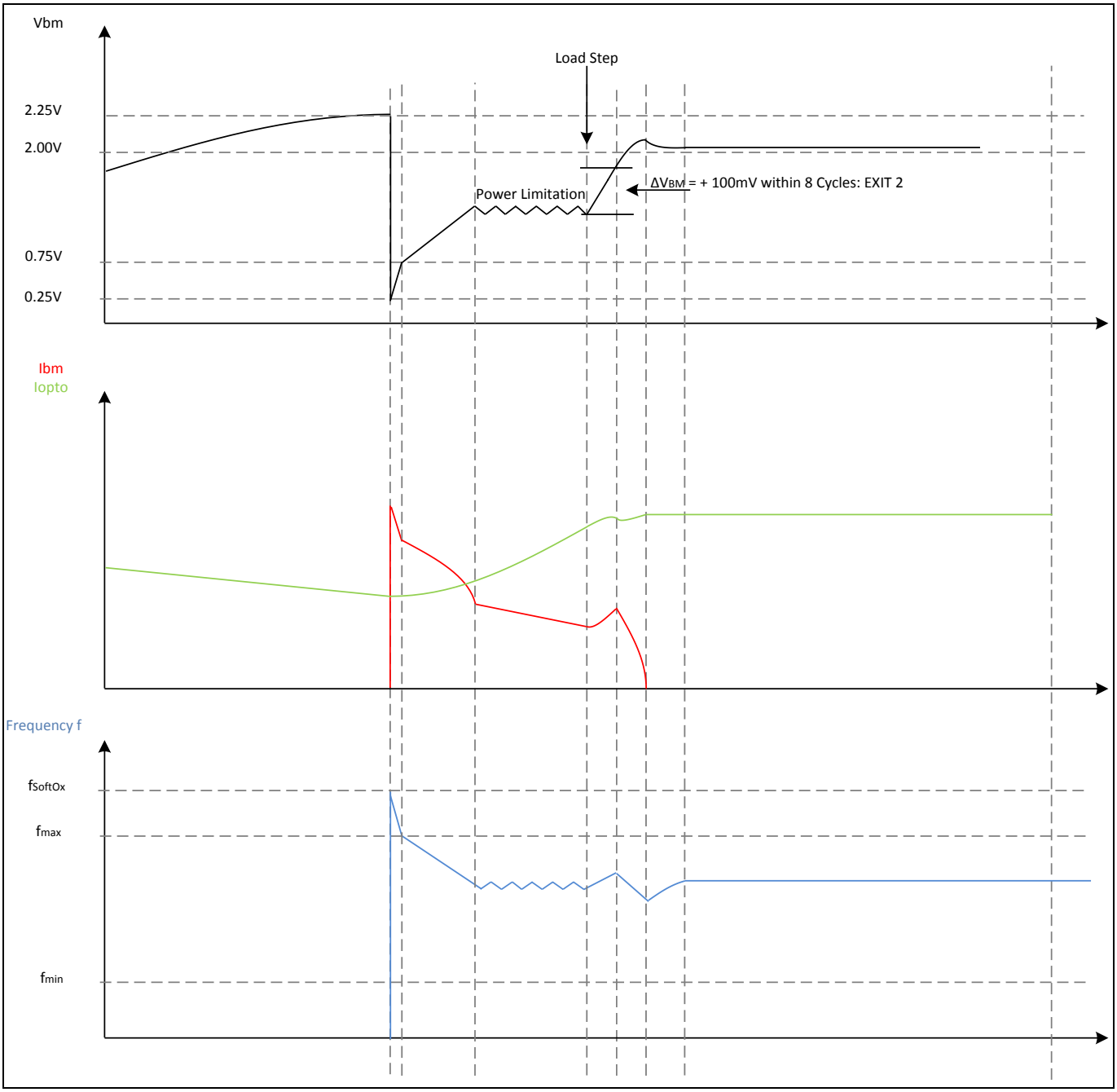

Figure 17 Burst Mode EXIT 2