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MAXIM

3 1/2 Digit A/D Converter With Display Hold

ICL7116/7117

General Description

The Maxim ICL7116 and ICL7117 are 3 1/2 digit monolithic analog to digital converters. They differ from the Maxim ICL7106 and ICL7107 in that the ICL7116 and ICL7117 have a Hold pin which makes it possible to hold or "freeze" a reading. These integrating A/D converters have very high input impedances and directly drive LCD (ICL7116) and LED (ICL7117) displays.

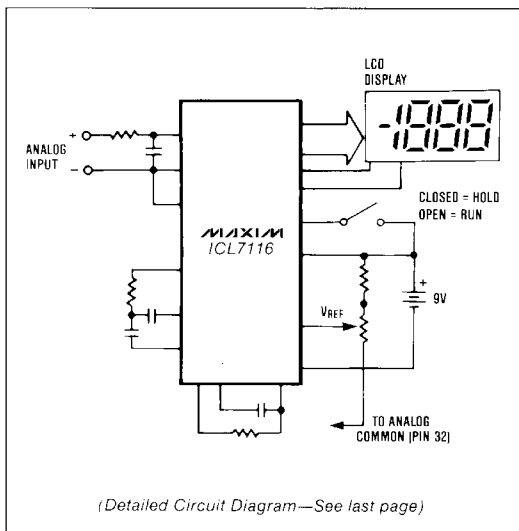
Versatility and accuracy are inherent features of these converters. The dual-slope conversion technique automatically rejects interference signals common in industrial environments. The true differential input is particularly useful when making ratiometric measurements (ohms or bridge transducers). Maxim has added a zero-integrator phase to the ICL7116 and ICL7117, eliminating overrange hangover and hysteresis effects. Finally, these devices offer high accuracy by lowering rollover error to less than one count and zero reading drift to less than 1 μ V/ $^{\circ}$ C.

Applications

These devices can be used in a wide range of digital panel meter applications. Most applications, however, involve the measurement and display of analog data:

- | | |
|-------------|--------------------|
| Pressure | Conductance |
| Voltage | Current |
| Resistance | Speed |
| Temperature | Material Thickness |

Typical Operating Circuit



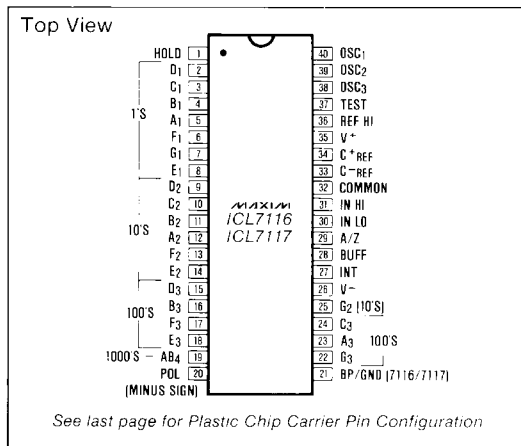
Features

- ◆ Improved 2nd Source! (See 3rd page for "Maxim Advantage™").
- ◆ Hold Pin Allows Indefinite Display Hold
- ◆ Guaranteed First Reading Recovery from Overrange
- ◆ On Board Display Drive Capability — No External Circuitry Required: LCD-ICL7116, LED-ICL7117
- ◆ High Impedance CMOS Differential Inputs
- ◆ Low Noise (< 15 μ V p-p) Without Hysteresis or Overrange Hangover
- ◆ Clock and Reference On-Chip
- ◆ Zero Input Gives Zero Reading
- ◆ True Polarity Indication for Precision Null Applications

Ordering Information

PART	TEMP. RANGE	PACKAGE
ICL7116CPL	0 $^{\circ}$ C to +70 $^{\circ}$ C	40 Lead Plastic DIP
ICL7116CJL	0 $^{\circ}$ C to +70 $^{\circ}$ C	40 Lead Cerdip
ICL7116CQ	0 $^{\circ}$ C to +70 $^{\circ}$ C	44 Lead Plastic Chip Carrier
ICL7116C/D	0 $^{\circ}$ C to +70 $^{\circ}$ C	Dice
ICL7117CPL	0 $^{\circ}$ C to +70 $^{\circ}$ C	40 Lead Plastic DIP
ICL7117CJL	0 $^{\circ}$ C to +70 $^{\circ}$ C	40 Lead Cerdip
ICL7117CQ	0 $^{\circ}$ C to +70 $^{\circ}$ C	44 Lead Plastic Chip Carrier
ICL7117C/D	0 $^{\circ}$ C to +70 $^{\circ}$ C	Dice

Pin Configuration



The "Maxim Advantage™" signifies an upgraded quality level. At no additional cost we offer a second-source device that is subject to the following: guaranteed performance over temperature along with tighter test specifications on many key parameters; and device enhancements, when needed, that result in improved performance without changing the functionality.

3½ Digit A/D Converter With Display Hold

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		Power Dissipation (Note 2)	
ICL7116, V ⁺ to V ⁻	15V	Ceramic Package	1000mW
ICL7117, V ⁺ to GND	+6V	Cerdip Package	800mW
ICL7117, V ⁻ to GND	-9V	Plastic Package	800mW
Analog Input Voltage (either input) (Note 1)	V ⁺ to V ⁻	Operating Temperature Range	0°C to +70°C
Reference Input Voltage (either input)	V ⁺ to V ⁻	Storage Temperature Range	-65°C to +160°C
Clock Input		Lead Temperature (soldering, 60 sec.)	+300°C
ICL7116	Test to V ⁺		
ICL7117	GND to V ⁺		

- Note 1:** Input voltage may exceed supply voltages, provided the input current is limited to ±100μA
Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	V _{IN} = 0.0V Full Scale = 200.0mV	-000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	V _{IN} = V _{REF} = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full Scale)	-V _{IN} = +V _{IN} = 200.0mV	-1	±0.2	+1	Counts
Linearity (Max. Deviation from Best Straight Line Fit)	Full Scale = 200mV or Full Scale = 2.000mV	-1	±0.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	V _{CM} = ±1V, V _{IN} = 0V Full Scale = 200.0mV	50		μV/V	
Noise (Pk-Pk Value Not Exceeded 95% of the Time)	V _{IN} = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	V _{IN} = 0V		1	10	pA
Zero Reading Drift	V _{IN} = 0V, 0°C < T _A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	V _{IN} = 199.0mV 0°C < T _A < 70°C (Ext. Ref. 0ppm/°C)		1	5	ppm/°C
V ⁺ Supply Current (Does Not Include LED Current for 7117)	V _{IN} = 0		0.8	1.8	mA
V ⁻ Supply Current 7117 Only			0.6	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25Ω Between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25Ω Between Common & Pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V _{IL} , Pin 1 (7116 Only)				TEST -1.5	V
V _{IL} , Pin 1 (7117 Only)				GND +1.5	V
V _{IH} , Pin 1 (Both)		V ⁺ - 1.5			V
7116 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V ⁺ to V ⁻ - 9V	4	5	6	V
		4	5	6	V
7117 Only (Except Pin 19) Segment Sinking Current (Pin 19 Only)	V ⁺ = 5.0V Segment Voltage = 3V	5	8.0		mA
		10	16		

- Note 3:** Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{Clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.
Note 4: Refer to "Differential input" discussion. (See Maxim's ICL7106/ICL7107 data sheet)
Note 5: Backplane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.
Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin1, to GROUND, pin 21.

The electrical characteristics above are a reproduction of a portion of Intersil's copyrighted 1983/1984 data book. This information does not constitute any representation by Maxim that Intersil's products will perform in accordance with these specifications. The "Electrical Characteristics Table" along with descriptive excerpts from the original manufacturer's data sheet have been included in this data sheet solely for comparative purposes.



3½ Digit A/D Converter With Display Hold

- ◆ Guaranteed Overload Recovery Time
- ◆ Significantly Improved ESD Protection (Note 8)
- ◆ Low Noise
- ◆ Key Parameters Guaranteed Over Temperature
- ◆ Negligible Hysteresis
- ◆ Maxim Quality and Reliability
- ◆ Increased Maximum Rating for Input Current (Note 9)

ABSOLUTE MAXIMUM RATINGS: This device conforms to the Absolute Maximum Ratings on adjacent page.

ELECTRICAL CHARACTERISTICS: Specifications below satisfy or exceed all "tested" parameters on adjacent page. ($V^+ = 9V$, $T_A = 25^\circ C$, $f_{CLOCK} = 48kHz$; test circuit - Figure 1 (ICL7116), Figure 2 (ICL7117) unless noted)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	$V_{IN} = 0.0V$, Full Scale = 200.0mV $T_A = 25^\circ C$ (Note 7) $0^\circ C \leq T_A \leq 70^\circ C$ (Note 11)	-000.0 -000.0	± 000.0 ± 000.0	+000.0 +000.0	Digital Reading
Ratiometric Reading	$V_{IN} = V_{REF} = 100mV$ $T_A = 25^\circ C$ (Note 7) $0^\circ C \leq T_A \leq 70^\circ C$ (Note 11)	999 998	999/1000 999/1000	1000 1001	Digital Reading
Rollover Error (Difference in Reading for Equal Positive and Negative Reading Near Full Scale)	$-V_{IN} = +V_{IN} = 200.0mV$ $T_A = 25^\circ C$ (Note 7) $0^\circ C \leq T_A \leq 70^\circ C$ (Note 11)	-1	± 0.2 ± 0.2	+1	Counts
Linearity (Max. Deviation from Best Straight Line Fit)	Full Scale = 200mV or Full Scale = 2.000mV	-1	± 0.2	+1	Counts
Common Mode Rejection Ratio	$V_{CM} = \pm 1V$, $V_{IN} = 0V$ Full Scale = 200.0mV		50		$\mu V/V$
Noise (Pk-Pk Value Not Exceeded 95% of the Time)	$V_{IN} = 0V$ Full Scale = 200.0mV		15		μV
Input Leakage Current	$V_{IN} = 0V$, $T_A = 25^\circ C$ (Note 7) $0^\circ C \leq T_A \leq 70^\circ C$		1 20	10 200	pA
Zero Reading Drift	$V_{IN} = 0V$ $0^\circ C \leq T_A \leq 70^\circ C$ (Note 7)		0.2	1	$\mu V/^\circ C$
Scale Factor Temperature Coefficient	$V_{IN} = 199.0mV$ $0^\circ C \leq T_A \leq 70^\circ C$ (Ext. Ref. 0ppm/ $^\circ C$)		1	5	ppm/ $^\circ C$
V^+ Supply Current (Does Not Include LED Current for 7117)	$V_{IN} = 0V$ $T_A = 25^\circ C$ $0^\circ C \leq T_A \leq 70^\circ C$		0.8	1.8 2	mA
V^- Supply Current 7117 Only			0.6	1.8	mA
Analog Common Voltage (With Respect to Pos. Supply)	25k Ω Between Common & Pos. Supply	2.4	2.8	3.2	V
Temp. Coeff. of Analog Common (With Respect to Pos. Supply)	25k Ω Between Common & Pos. Supply		75		ppm/ $^\circ C$
Input Resistance, Pin 1 (Note 6)		30	70		k Ω
V_{IL} , Pin 1 (7116 Only)				TEST +1.5	V
V_{IL} , Pin 1 (7117 Only)				GND +1.5	V
V_{IH} , Pin 1 (Both)		$V^+ - 1.5$			V
7116 Only (Note 5) Pk-Pk Segment Drive Voltage, Pk-Pk Backplane Drive Voltage	V^+ to $V^- = 9V$	4	5	6	V
7117 Only (Except Pin 19) Segment Sinking Current (Pin 19 Only)	$V^+ = 5.0V$ Segment Voltage = 3V	5 10	8.0 16		mA mA
7116 Only — Test Pin Voltage	With Respect to V^+	4	5	6	V
Overload Recovery Time (Note 10)	V_{IN} changing from $\pm 10V$ to 0V		0	1	Measurement Cycles

Note 7: Test condition is V_{IN} applied between pins IN-HI and IN-LO, i.e., 1M Ω resistor in Figures 1 and 2.

Note 8: All pins are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per MIL Std. 883C, Method 3015.2)

Note 9: Input voltages may exceed the supply voltage provided the input current is limited to $\pm 1mA$ (This revises Note 1 on the adjacent page).

Note 10: Number of measurement cycles for display to give accurate reading.

Note 11: 1M Ω resistor is removed in Figures 1 and 2.



ICL7116/7117

3½ Digit A/D Converter With Display Hold

Detailed Description

The Maxim ICL7116 and ICL7117 3½ digit A/D converter are similar to the Maxim ICL7106 and ICL7107, except for the addition of a Hold pin. For a detailed product description, package dimensions, and applications information (other than the operation of the Hold pin described below) refer to Maxim's ICL7106 and ICL7107 data sheet.

Hold Input

The Hold input is a digital input with a logic threshold approximately midway between V^+ and Test (ICL7116) or V^+ and Ground (ICL7117). The ICL7116/7117 continuously performs conversions, independent of the Hold input. When the Hold input is connected to V^+ ,

however, the display latch pulse is inhibited, and the display latches are not updated. The Hold input has a 70 kilohm pulldown resistor to Test (ICL7116) or Ground (ICL7117) and the Hold input will be pulled low if it is left open. When Hold is low the ICL7116/ICL7117 updates the display at the end of each conversion. The Hold input is CMOS compatible, and can also be driven by a switch connected to V^+ (Figure 1 and 2) or by a PNP transistor.

Unlike the ICL7106 and the ICL7107, the ICL7116 and ICL7117 do not have a Reference Low input. Apply the reference voltage between Reference High (REF HI) and Common.

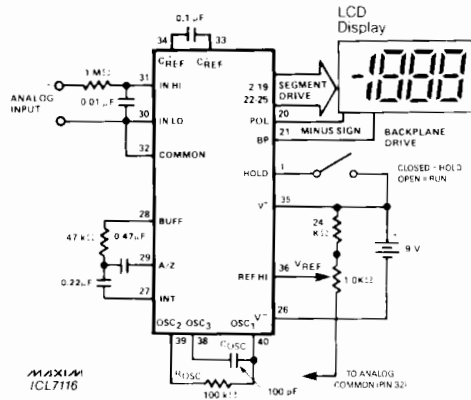


Figure 1. Maxim ICL7116 Typical Operating Circuit, 200mV Reference

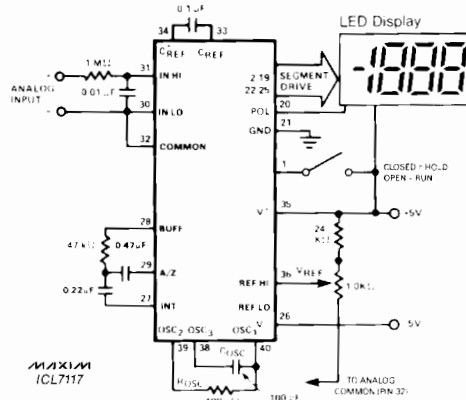
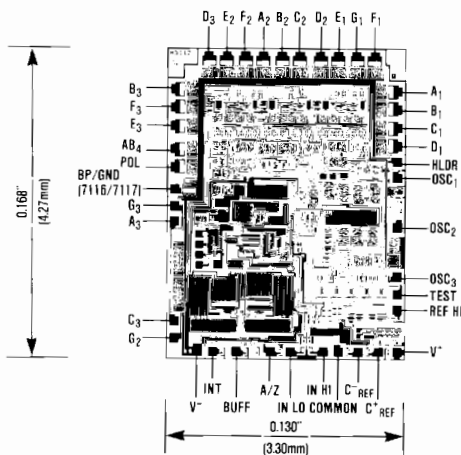
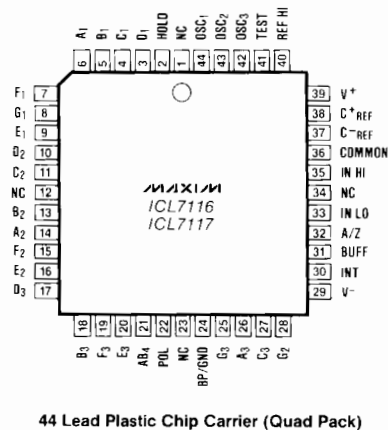


Figure 2. Maxim ICL7117 Typical Operating Circuit, 200mV Reference

Chip Topography



Pin Configuration



44 Lead Plastic Chip Carrier (Quad Pack)

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