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# MAXIM

# 4-1/2 Digit Single-Chip A/D Converter with LCD Driver



## General Description

The Maxim ICL7129A/MAX7129 is a high precision monolithic 4-1/2 digit A/D converter that directly drives a multiplexed liquid crystal display. Using a novel "successive integration" technique, the ICL7129A/MAX7129 has a ±20,000 count resolution on both 2.00000V and 200.00mV ranges. It features high impedance differential inputs, excellent differential linearity, true ratiometric operation and auto polarity. The only external active component required to make precision DVM/DPMs is a reference. The overrange and underrange outputs and the 10:1 range changing input facilitate the design of autoranging systems. The ICL7129A/MAX7129 detects and flags a LOW BATTERY condition and also checks for continuity, giving a visual indication and a logic level output which can be used to generate an audible signal.

The MAX7129 has a fullscale accuracy of 0.0005%, resolution of 10μV, zero reading drift of 0.5μV/°C, an input bias of 10pA max, and a rollover error of less than 1 count. Maxim has reduced the noise of the ICL7129A to 3μV—significantly lower than the MAX7129.

## Applications

This device can be used for a wide range of precision digital voltmeter, multimeter and panelmeter applications. Most applications involve the measurement and display of analog data:

| | |
|---|---|
| Pressure | Weight |
| Voltage | Current |
| Resistance | Speed |
| Temperature | Material Thickness |

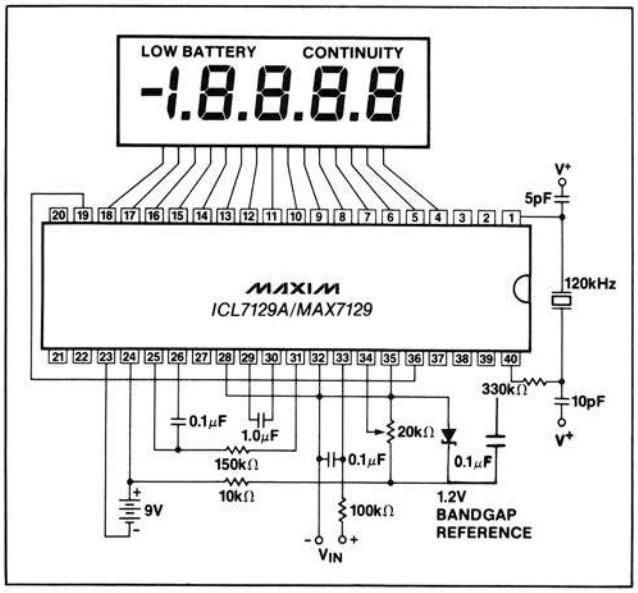
## Features

- ±19,999 Count Resolution
- 10pA Max Input Bias Current (MAX7129)
- 3μV peak to peak noise (ICL7129A)
- Onboard Multiplexed LCD Display Driver 4-1/2 Digits, 4 Decimal Points, 3 Annunciators
- Instant Continuity Detector
- Low Battery Detector and Indicator
- Overrange/Underrange Outputs
- Precise 10:1 Range Select
- 10μV Resolution
- Significantly improved ESD protection
- Monolithic, Low Power CMOS Design
- Eliminates Need for Compensation Capacitor

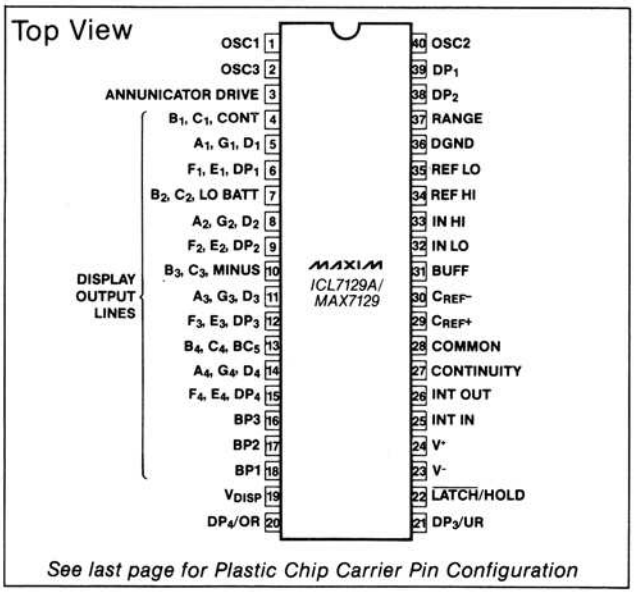
## Ordering Information

| PART | TEMP. RANGE | PACKAGE |
|---|---|---|
| MAX7129CPL | 0°C to +70°C | 40 Lead Plastic DIP |
| MAX7129CJL | 0°C to +70°C | 40 Lead CERDIP |
| MAX7129CQH | 0°C to +70°C | 44 Lead Plastic Chip Carrier |
| MAX7129C/D | 0°C to +70°C | Dice |
| ICL7129ACPL | 0°C to +70°C | 40 Lead Plastic DIP |
| ICL7129ACJL | 0°C to +70°C | 40 Lead CERDIP |
| ICL7129ACQ | 0°C to +70°C | 44 Lead Plastic Chip Carrier |
| ICL7129AC/D | 0°C to +70°C | Dice |

## Typical Operating Circuit




## Pin Configuration




*See last page for Plastic Chip Carrier Pin Configuration*

# 4-1/2 Digit Single-Chip A/D Converter with LCD Driver

## ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+$ to $V^-$) ..... 15V
Reference Voltage (REF HI or REF LO) ..... $V^+$ to $V^-$
Input Voltage (Note 1)
(IN HI or IN LO) ..... $V^+$ to $V^-$
$V_{DISP}$ ..... $V^+$ to DGND - 0.3V
Digital Input Pins
1, 2, 19, 20, 21, 22, 27,
37, 38, 39, 40 ..... DGND to $V^+$
Analog Input Pins
25, 29, 30 ..... $V^+$ to $V^-$

Power Dissipation (Note 2)
CERDIP package ..... 1000mW
Plastic package ..... 800mW
Plastic Chip Carrier
(Quad) Package ..... 700mW
Operating Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... -65°C to +160°C
Lead Soldering Temperature (10 sec.) ..... 300°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## ELECTRICAL CHARACTERISTICS (MAX7129)

($V^+$ to $V^-$ = 9V, $V_{REF}$ = 1.00V. $T_A$ = +25°C, $f_{CLK}$ = 120kHz, unless otherwise noted.)

| PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Zero Input Reading | $V_{IN}$ = 0V, 200mV Scale | -0000 | 0000 | +0000 | Reading |
| Zero Reading Drift | $V_{IN}$ = 0V, 0°C ≤ $T_A$ ≤ +70°C | | ±0.5 | | µV/°C |
| Ratiometric Reading | $V_{IN}$ = $V_{REF}$ = 1000mV, RANGE = 2V | 9998 | 9999 | 10000 | Reading |
| Range Change Accuracy | $V_{IN}$ = 0.10000V on Low Range ÷ $V_{IN}$ = 0.10000V on High Range | 0.9999 | 1.0000 | 1.0001 | Ratio |
| Rollover Error | -$V_{IN}$ = +$V_{IN}$ = 199mV | | 0.5 | 1.0 | Counts |
| Linearity Error | 200mV Scale | | 0.5 | | Counts |
| Input Common-Mode Rejection Ratio | $V_{CM}$ = 1.0V, $V_{IN}$ = 0V 200mV Scale | | 110 | | dB |
| Input Common-Mode Voltage Range | $V_{IN}$ = 0V 200mV Scale | ($V^-$) + 1.5 | | ($V^+$) - 0.5 | V |
| Noise (p-p Value not Exceeded 95% of Time) | $V_{IN}$ = 0V 200mV Scale | | 7.0 | | µV |
| Input Leakage Current | $V_{IN}$ = 0V, IN HI<br>$V_{IN}$ = 0V, IN LO | | 1<br>3 | 10<br>40 | pA<br>pA |
| Scale Factor Tempco | $V_{IN}$ = 199mV, 0°C ≤ $T_A$ ≤ +70°C External $V_{REF}$ = 0ppm/°C | | 2 | 5 | ppm/°C |
| COMMON Voltage | $V^+$ to Pin 28 | 2.8 | 3.2 | 3.5 | V |
| COMMON Sink Current | ΔCommon = +0.1V | 0.1 | 2.0 | | mA |
| COMMON Source Current | ΔCommon = -0.1V | 1 | 9 | 15 | µA |
| DGND Voltage | $V^+$ to Pin 36 | 4.5 | 5.3 | 5.8 | V |
| DGND Sink Current | ΔDGND = +0.5V | 0.5 | 1.2 | | mA |
| Supply Voltage Range | $V^+$ to $V^-$ | 6 | 9 | 14 | V |
| Supply Current Excluding COMMON Current | | | 1.0 | 1.4 | mA |
| Clock Frequency | | | 120 | 360 | kHz |
| Display Multiplex Rate | | | 100 | | Hz |
| $V_{DISP}$ Resistance | $V_{DISP}$ to $V^+$ | 20 | 50 | 100 | kΩ |
| Low Battery Flag Activation Voltage | $V^+$ to $V^-$ | 6.3 | 7.2 | 7.7 | V |
| CONTINUITY Comparator Threshold Voltages | $V_{OUT}$ Pin 27 = HI<br>$V_{OUT}$ Pin 27 = LO | 100 | 200<br>200 | <br>400 | mV<br>mV |
| Pull-Down Current | Pins 37, 38, 39 | 0.25 | 2 | 10 | µA |
| "Weak Output" Current | Pin 20, 21 | 0.25 | 3/3 | 10 | µA |
| Sink, Source | Pin 27 Sink/Source | 0.25 | 3/9 | 15 | µA |
| Pin 22 Source Current<br>Pin 22 Sink Current | | 1<br>0.25 | 40<br>3 | 100<br>10 | µA<br>µA |

**ABSOLUTE MAXIMUM RATINGS:** This device conforms to the Absolute Maximum Ratings on adjacent page.

## ELECTRICAL CHARACTERISTICS (ICL7129A)

($V^+$ to $V^-$ = 9V, $V_{REF}$ = 1.00V. $T_A$ = +25°C, $f_{CLK}$ = 120kHz, unless otherwise noted. Test Circuit without $C_C$.)

| PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| Zero Input Reading | $V_{IN}$ = 0V, 200mV Scale | -0000 | 0000 | +0000 | Reading |
| Zero Reading Drift | $V_{IN}$ = 0V, 0°C ≤ $T_A$ ≤ +70°C | | ±0.5 | | µV/°C |
| Ratiometric Reading | $V_{IN}$ = $V_{REF}$ = 1000mV, RANGE = 2V | 9998 | 9999 | 10000 | Reading |
| Range Change Accuracy | $V_{IN}$ = 0.10000V on Low Range ÷ $V_{IN}$ = 0.10000V on High Range | 0.9999 | 1.0000 | 1.0001 | Ratio |
| Rollover Error | -$V_{IN}$ = +$V_{IN}$ = 199mV | | 0.5 | 1.0 | Counts |
| Linearity Error | 200mV Scale | | 0.5 | | |
| Input Common-Mode Rejection Ratio | $V_{CM}$ = 1.0V, $V_{IN}$ = 0V 200mV Scale | | 110 | | dB |
| Input Common-Mode Voltage Range | $V_{IN}$ = 0V 200mV Scale | ($V^-$) + 1.5 | | ($V^+$) - 0.5 | V |
| Noise (p-p Value not Exceeded 95% of Time) | $V_{IN}$ = 0V 200mV Scale | | 3.0 | (Note 4) | µV |
| Input Leakage Current | $V_{IN}$ = 0V, IN HI<br>$V_{IN}$ = 0V, IN LO | | 13<br>15 | 20<br>40 | pA |
| Scale Factor Tempco | $V_{IN}$ = 199mV, 0°C ≤ $T_A$ ≤ +70°C External $V_{REF}$ = 0ppm/°C | | 2 | 5 | ppm/°C |
| COMMON Voltage | $V^+$ to Pin 28 | 2.8 | 3.2 | 3.5 | V |
| COMMON Sink Current | ΔCommon = +0.1V | 0.1 | 2.0 | | mA |
| COMMON Source Current | ΔCommon = -0.1V | 1 | 9 | 15 | µA |
| DGND Voltage | $V^+$ to Pin 36, $V^+$ to $V^-$ = 9V | 4.2 | 5.3 | 5.8 | V |
| DGND Sink Current | ΔDGND = +0.5V | 0.5 | 1.2 | | mA |
| Supply Voltage Range | $V^+$ to $V^-$ | 6 | 9 | 14 | V |
| Supply Current Excluding COMMON Current | $V^+$ to $V^-$ = 9V | | 1.0 | 1.4 | mA |
| Clock Frequency | | | 120 | 360 | kHz |
| Display Multiplex Rate | $f_{CLK}$ = 120kHz | | 100 | | Hz |
| $V_{DISP}$ Resistance | $V_{DISP}$ to $V^+$ | 20 | 50 | 100 | kΩ |
| Low Battery Flag Activation Voltage | $V^+$ to $V^-$ | 6.3 | 7.2 | 7.7 | V |
| CONTINUITY Comparator Threshold Voltages | $V_{OUT}$ Pin 27 = HI<br>$V_{OUT}$ Pin 27 = LO | 100 | 200<br>200 | <br>400 | mV<br>mV |
| Pull-Down Current | Pins 37, 38, 39 | 0.25 | 2 | 10 | µA |
| "Weak Output" Current | Pins 20, 21 | 0.25 | 3/3 | 10 | µA |
| Sink, Source | Pin 27 Sink/Source | 0.25 | 3/9 | 15 | µA |
| Pin 22 Source Current<br>Pin 22 Sink Current | | 1<br>0.25 | 40<br>3 | 100<br>10 | µA<br>µA |

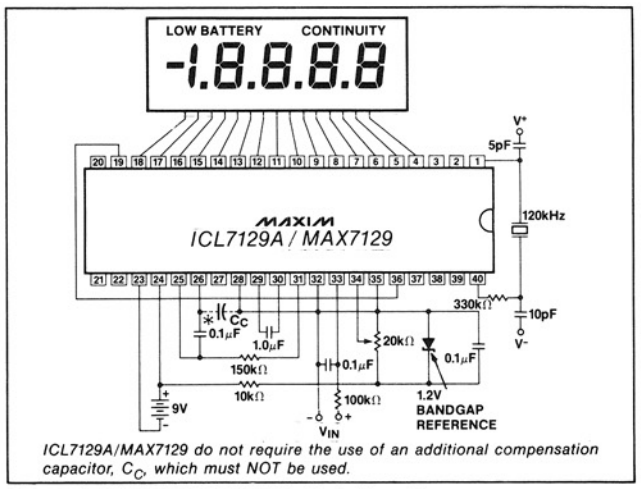
**Note 1:** Input voltages may exceed the supply voltages provided that input current is limited to ±400µA. Current above this value may result in invalid display readings but will not destroy the device if limited to ±mA.

**Note 2:** Dissipation ratings assume device is mounted with all leads soldered to printed circuit board.

**Note 3:** All pins on Maxim's MAX7129 and ICL7129A are designed to withstand electrostatic discharge (ESD) levels in excess of 2000V. (Test circuit per Mil. Std. 883, Method 3015.1)

**Note 4:** The Maxim ICL7129A uses innovative noise reduction techniques to achieve a 3µV noise level. This ensures that for any specific input voltage, the ICL7129A continuously displays one number or fluctuates between two adjacent numbers. In no case will the ICL7129A display three different numbers for a constant input voltage.

# 4-1/2 Digit Single-Chip A/D Converter with LCD Driver




*ICL7129A/MAX7129 do not require the use of an additional compensation capacitor, $C_C$, which must NOT be used.*

*Figure 1. MAX7129/ICL7129A Test Circuit*

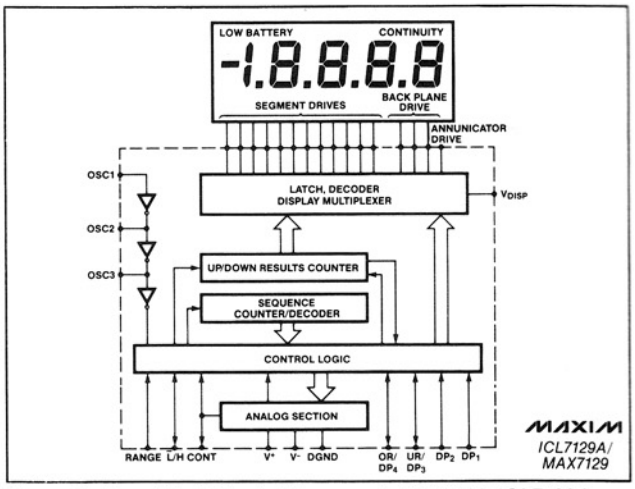



*Figure 2. Simplified Block Diagram of MAX7129/ICL7129A Digital Section*

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | OSC1 | Input to first clock inverter. |
| 2 | OSC3 | Output of second clock inverter. |
| 3 | ANNUNCIATOR DRIVE | Backplane squarewave output for driving annunciators. |
| 4 | $B_1$, $C_1$, CONT | Output to display segments. |
| 5 | $A_1$, $G_1$, $D_1$ | Output to display segments. |
| 6 | $F_1$, $E_1$, $DP_1$ | Output to display segments. |
| 7 | $B_2$, $C_2$, LO BATT | Output to display segments. |
| 8 | $A_2$, $G_2$, $D_2$ | Output to display segments. |
| 9 | $F_2$, $E_2$, $DP_2$ | Output to display segments. |
| 10 | $B_3$, $C_3$, MINUS | Output to display segments. |
| 11 | $A_3$, $G_3$, $D_3$ | Output to display segments. |
| 12 | $F_3$, $E_3$, $DP_3$ | Output to display segments. |
| 13 | $B_4$, $C_4$, $BC_5$ | Output to display segments. |
| 14 | $A_4$, $G_4$, $D_4$ | Output to display segments. |
| 15 | $F_4$, $E_4$, $DP_4$ | Output to display segments. |
| 16 | BP3 | Backplane #3 output to display. |
| 17 | BP2 | Backplane #2 output to display. |
| 18 | BP1 | Backplane #1 output to display. |
| 19 | $V_{DISP}$ | Negative supply for display drivers. |
| 20 | $DP_4$/OR | INPUT: Turns on most significant decimal point when HI.<br>OUTPUT: Pulled HI when result count exceeds ±19,999. |
| 21 | $DP_3$/UR | INPUT: When floating, MAX7129/ICL7129 significant decimal point when HI.<br>OUTPUT: Pulled HI when result count is less than ±1,000. |
| 22 | $\overline{\text{LATCH}}$/HOLD | INPUT: When floating, ICL7129 operates in the free-run mode. When pulled HI, the last displayed reading is held. When pulled LO, the result counter contents are shown incrementing during the de-integrate phase of cycle.<br>OUTPUT: Negative going edge occurs when the data latches are updated. Can be used as a converter status signal. |
| 23 | $V^-$ | Negative power supply terminal. |
| 24 | $V^+$ | Positive power supply terminal, and positive supply for display drivers. |
| 25 | INT IN | Integrator amplifier input. |
| 26 | INT OUT | Integrator amplifier output. |
| 27 | CONTINUITY | INPUT: When LO, continuity flag on the display is off. When HI, continuity flag is on.<br>OUTPUT: HI when voltage between inputs is less than +200mV. LO when voltage between inputs is more than +200mV. |
| 28 | COMMON | Sets common-mode voltage of 3.2V below $V^+$ for DE, 10X, etc. |
| 29 | $C_{REF}+$ | Positive side of external reference capacitor. |
| 30 | $C_{REF}-$ | Negative side of external reference capacitor. |
| 31 | BUFFER | Buffer amplifier output. |
| 32 | IN LO | Negative input voltage terminal. |
| 33 | IN HI | Positive input voltage terminal. |
| 34 | REF HI | Positive reference voltage input. |
| 35 | REF LO | Negative reference voltage input. |
| 36 | DGND | Ground reference for digital section. |
| 37 | RANGE | 3μA pull-down for 200mV scale. Pulled HIGH externally for 2V scale. |
| 38 | $DP_2$ | Internal 3μA pull-down. When HI, decimal point 2 will be on. |
| 39 | $DP_1$ | Internal 3μA pull-down. Turns on least significant decimal point when HI. |
| 40 | OSC2 | Output of first clock inverter. Input of second clock inverter. |

**Table 1. PIN ASSIGNMENTS AND FUNCTIONS**

## Detailed Description

### Conversion Technique

The ICL7129A/MAX7129 differs from earlier integrating A/Ds in two ways. First, it uses a variant of the dual-slope method called "successive integration." Secondly, it uses digital autozeroing rather than an analog autozero loop requiring an external autozero capacitor. Earlier converters stored an offset correction voltage on the autozero capacitor. Although this method worked well for 100$\mu V$ resolution A/Ds, the autozero loop resulted in greatly increased noise in the earlier generation of integrating A/Ds, making them unsuitable for 10$\mu V$ resolution systems. The ICL7129A/MAX7129 eliminates the autozero capacitor and the noise associated with the autozero loop by performing two conversions with 5½ digit resolution. The first conversion is performed with the A/D connected to the external inputs, Input HI and Input LO. The second conversion is performed with the A/D inputs internally shorted together. The results of this second conversion, which is proportional to the A/D's offset, is digitally subtracted from the first reading to generate an offset-corrected, autozeroed measurement result.

The ICL7129A/MAX7129 enhances the dual slope conversion technique through multiple dual slope conversions, with each successive conversion having 10 times the resolution of the preceding conversion. The key to this "successive integration" technique is the multiplication of the residual voltage on the integrator capacitor after each conversion. The ICL7129A/MAX7129 first performs a 3½ digit dual slope conversion. The De-integration cycle terminates on the next positive clock edge after the integrator output crosses zero, leaving a small residue of voltage on the integrator capacitor. Unlike other A/D convertors, the ICL7129A/MAX7129 multiplies this residue by a factor of 10, then performs another dual slope conversion. Since the residue on the integrator capacitor has been multiplied by 10 the resolution of the second De-integration cycle is also increased by a factor of 10, and the ICL7129A/MAX7129 achieves 4½ digit resolution during the second De-integration cycle. The integrator capacitor residue left after the second De-integration cycle is again multiplied by 10, and the ICL7129A/MAX7129 performs a third De-integration cycle, this time with 5½ digit resolution.

Figure 2 shows a simplified block diagram of the ICL7129A/MAX7129 digital section. The sequence counter/decoder section keeps track of the many separate phases required for each conversion cycle and provides timing signals to the control logic. The sequence counter runs continuously and is independent of the up/down results counter, which is activated only when the integrator is De-integrating. The data remaining in the results counter at the end of a conversion is latched, decoded and multiplexed to the liquid crystal display.

Figure 3 shows a block diagram of the analog section including all of the analog switches used to configure the voltage sources and amplifiers in the different phases of the conversion cycle. The reference switching and input schemes are very similar to those in other less accurate, integrating A/D converters. A typical waveform on the integrator output is illustrated

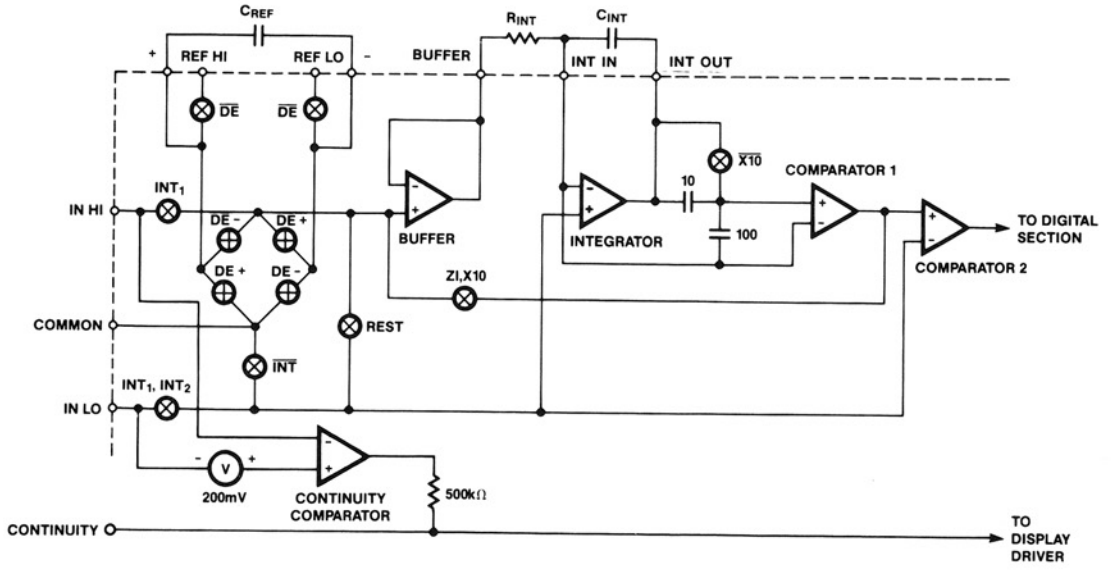



*Figure 3. Analog Section Block Diagram*

# 4-1/2 Digit Single-Chip A/D Converter with LCD Driver

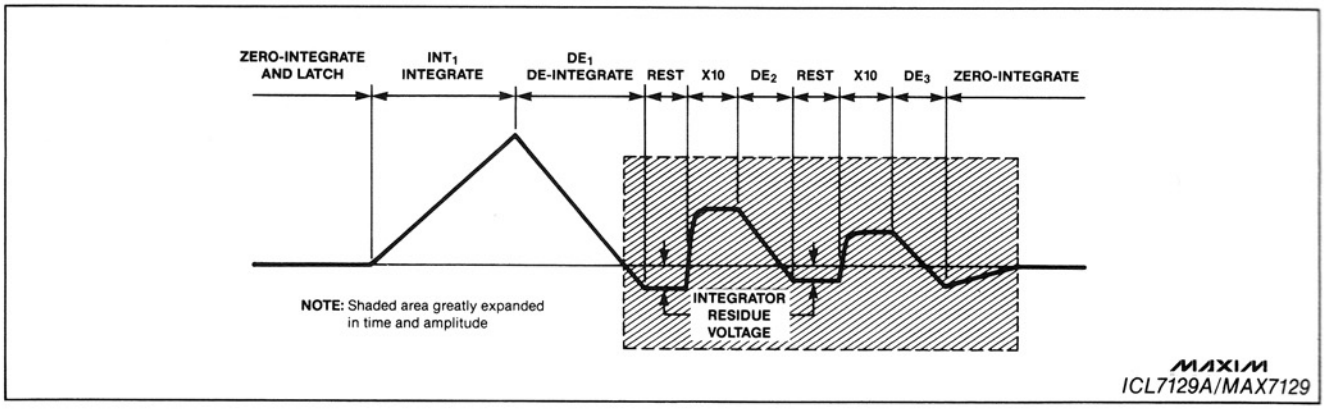



*Figure 4. Integrator Waveform for a Negative Input Voltage*

in Figure 4. $INT_1$ refers to the signal integrate phase where the input voltage is applied to the integrator amplifier via the buffer amplifier. In this phase, the integrator ramps over a fixed period of time in a direction opposite to the polarity of the input voltage. In the De-integrate phases, $DE_1$, $DE_2$, and $DE_3$, the reference capacitor is connected to the buffer amplifier and the integrator ramps back down towards Common, the level at which it started integrating. Since the De-integrate phase can terminate only at a clock pulse transition, there is always a small overshoot of the integrator past the starting point. The ICL7129A/MAX7129 amplifies this overshoot by -10 in the X10 phase and $DE_2$ begins. Similarly $DE_2$'s overshoot is amplified by -10 and $DE_3$ begins. At the end of $DE_3$ the results counter holds a number with 5½ digits of resolution. This result is obtained by feeding counts to the results counter at the 3½ digit level during $DE_1$, to the 4½ digit counter during $DE_2$ and the 5½ digit level during $DE_3$. The effects of offset in the buffer, integrator, and comparator can now be cancelled by repeating this entire sequence with the inputs shorted together and subtracting the results from the original reading. The $INT_2$ switch for this phase is closed so the integrator's common mode voltage is the same as the measurement cycle, thus ensuring excellent CMRR. The data in the up/down results counter at the end of the conversion cycle, accurate to 0.005% of full scale, is sent to the onboard display driver for decoding and multiplexing.

## Digital Section

### Oscillator and Clock Generator

The ICL7129A/MAX7129 has an oscillator suitable for either crystal or RC operation. The oscillator's output is internally divided by two to generate a system clock with a precise 50% duty cycle. All references to clock cycles in this data sheet refer to the system clock, which is half the frequency of the oscillator.

The crystal oscillator shown in Figure 5A is recommended for most applications. The crystal frequency should be 120kHz for maximum normal mode rejection at 60Hz, and 100kHz for maximum normal mode rejection at 50Hz.

Since an RC oscillator has more short term frequency jitter than a crystal oscillator, a crystal oscillator should be used for 4½ digit, 10μV resolution measurements.

The RC oscillator shown in Figure 5B is adequate for low resolution applications, (3½ digits at 100μV resolution). The capacitor value should be 51pF for all frequencies, and the resistor value calculated from $f_{OSC} = 0.45/RC$.

### Sequence Counter and Control Logic

This section provides the signals that control the operation of the analog section. The comparator output is the only input from the analog to the digital

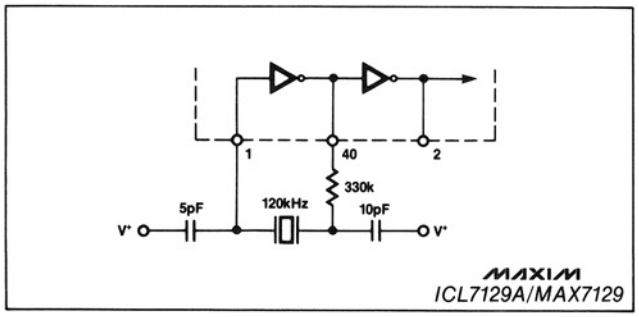



*Figure 5A. Crystal Oscillator Circuits*

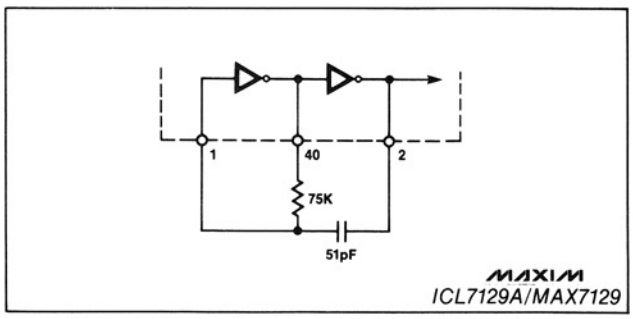



*Figure 5B. RC Oscillator Circuit*

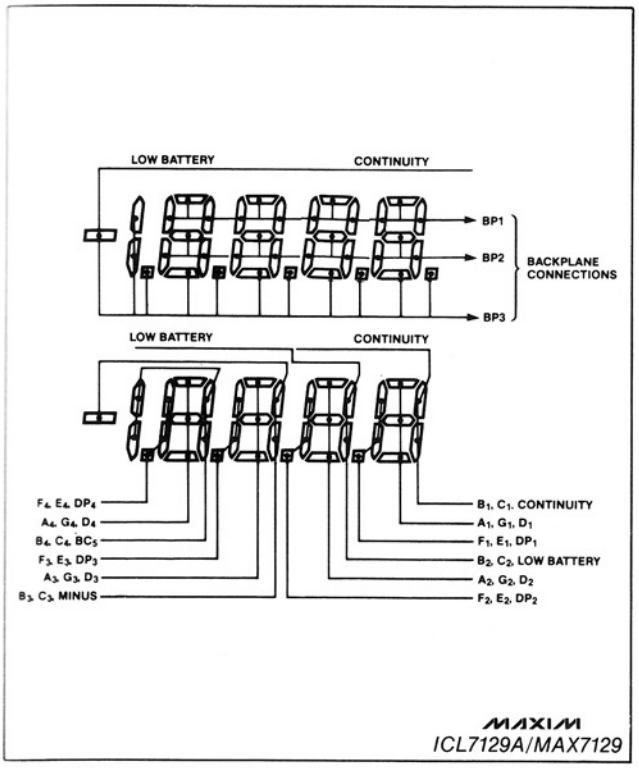



*Figure 6. Triplexed Liquid Crystal Display Layout*

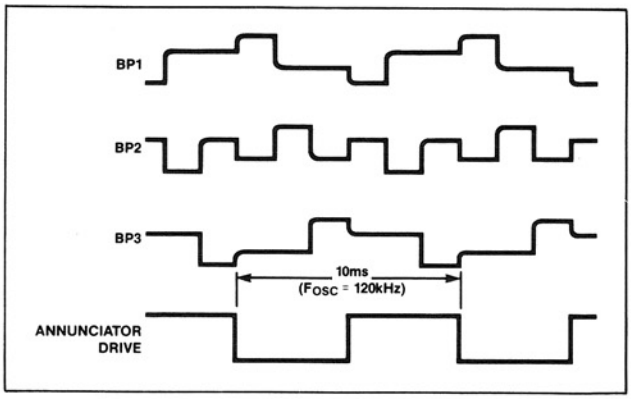



*Figure 7. Backplane and Annunciator Drive Waveforms*

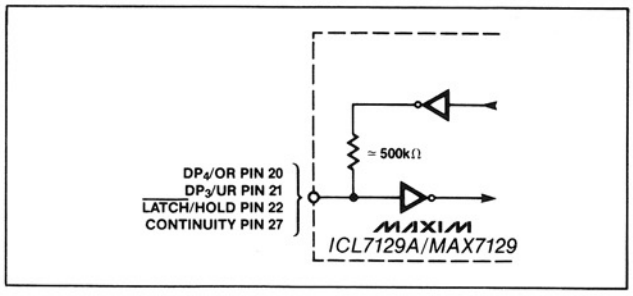



*Figure 8. "Weak Output" Digital I/O Pins*

section. The digital section uses the comparator output to determine the polarity of the integrator's output and to gate clock counts into the Up/Down Results Counter. The control logic also responds to the external digital inputs: Range, Hold, and Continuity. It also generates the digital outputs: Overrange, Underrange, Latch, and Continuity.

### Display Driver

The ICL7129A/MAX7129 can be used to drive a triplexed liquid crystal display with three backplanes. In addition to driving 4½—7 segment digits, the ICL7129A/MAX7129 can directly drive the decimal points, polarity sign, "Continuity," and "Low Battery" annunciators. Figure 6 shows the assignment of the 36 display segments to the three backplanes and 12 segment drive lines. The ICL7129A/MAX7129 divides the oscillator frequency by 1200 to generate the backplane frequency, resulting in a backplane frequency of 100Hz with a 120kHz oscillator crystal or 83.3Hz with a 100kHz crystal. Figure 7 shows the backplane and annunciator output waveforms.

### Range Input

With a 1V reference, the ICL7129A/MAX7129 has a 2V full scale when the Range input is high and a 200mV full scale when the Range input is low or open. The ICL7129A/MAX7129 achieves a precise 10:1 change in scale factor by reducing the integration period from 10,000 clock cycles on the 200mV range to 1000 clock cycles on the 2V range.

### Digital I/O Pins

Four of the ICL7129A/MAX7129's pins are quasi-directional and can be used as either inputs or outputs. As shown in Table 1, DP4/OR, DP3/UR, Latch/Hold, and Continuity each have dual input/output functions. Figure 8 shows a simplified schematic of these input/output pins. Since there is approximately 500kΩ in series with these outputs, they can only drive very light loads such as 4000 series, 74CXX type CMOS logic, or other high input impedance devices. Since the output drive current is limited to only a few microamps, the outputs are easily overdriven by 4000 series CMOS when the pin is used as an input.

### Latch/Hold

The Latch/Hold pin puts out a low-going pulse during the last 100 clock cycles of each conversion. This low-going pulse latches the conversion data into the onboard display driver section. The ICL7129A/MAX7129 will not update the display, and the display will continue to show the previous reading if the Latch/Hold pin is held high. If the Latch/Hold pin is held low, the display latches are transparent and the counting of the sequence counter can be observed during the de-integrating phases.

OverRange (OR pin 20) and UnderRange (UR pin 21) outputs are valid on the falling edge of Latch/Hold and remain in that state until the end of the next conversion cycle.

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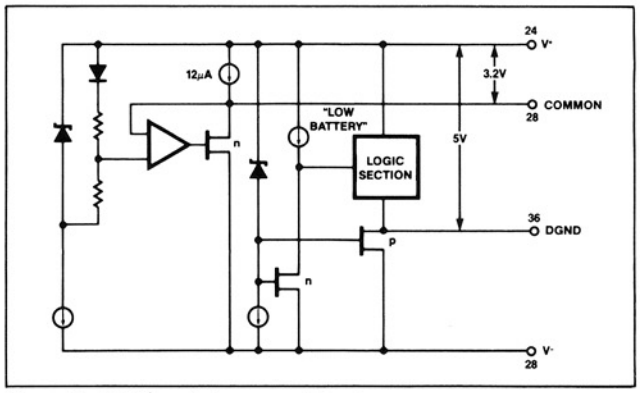


*Figure 9. DGND and Common Outputs*

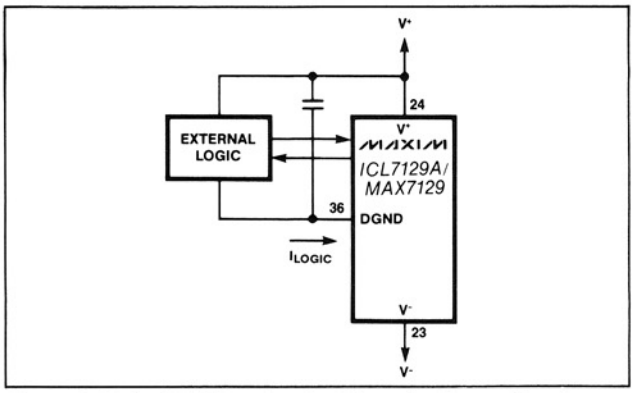


*Figure 10. Using DGND as Supply Voltage for External Logic*

### Overrange and Underrange Outputs

The DP4/OR (Decimal Point 4/Overrange) output goes high if the measurement result is greater than ±19,999. Similarly, the DP3/UR (Decimal Point 3/Underrange) output goes high if the measurement result is less than ±1000. These signals are updated at the end of each conversion, unless Latch/Hold is held high. These pins are also inputs that control the decimal points, DP3 and DP4. A high level input on these pins turns on the decimal point segments of the display. If these decimal points are not required, they can be used as logic level controlled annunciators.

### Continuity

An internal comparator with a 200mV threshold is connected directly between the INPUT HI and INPUT LO pins of the ICL7129A/MAX7129 (see Figure 3). The Continuity output (pin 27) will be pulled high whenever the voltage between the analog inputs is less than 200mV. This activates the Continuity annunciator on the display. The Continuity annunciator can also be controlled by an external source if desired, since the Continuity pin is one of the four quasi-bidirectional pins of the ICL7129A/MAX7129. A pull-down resistor connected between Continuity and DGND (pin 36) disables the continuity function when it is not desired.

## Analog Section

### Common, Digital GrouND, and Low Battery

Figure 9 shows how the Common and DGND (Digital GrouND) outputs of the ICL7129A/MAX7129 are generated from internal zener diodes. Common can be used to set the common mode voltage in applications where the input signals float with respect to the ICL7129A/MAX7129's power supplies, which is typical for battery powered applications. Common can also function as a pre-regulator for an external precision reference voltage source.

The voltage between $V^+$ and DGND is the internal supply voltage for the logic section of the ICL7129A/MAX7129. Both Common and DGND are capable of sinking current from external loads, but care should be taken to ensure that these outputs are not overloaded. The connection of external logic circuitry to the ICL7129A/MAX7129 is shown in Figure 10. This connection will work provided that the supply current requirements of the logic do not exceed the 1.2mA current sink capability of the DGND pin. The buffer in Figure 10 can be used to keep the loading on DGND to a minimum if more supply current is required. COMMON can source approximately 12μA whereas DGND has no source capability.

### Low Battery

The "Low Battery" annunciator of the display turns on when the supply voltage between $V^+$ and $V^-$ drops below 7.2V. The exact point at which this occurs is determined by the 6.3V zener diode and threshold voltage of the n-channel transistor connected to the $V^-$ rail shown in Figure 9.

### Buffer

The ICL7129A/MAX7129 buffer has a common mode input voltage range of $V^-$ + 1.5V to $V^+$ - 1.0V and can supply up to 20μA of output current.

### Integrator

The integator can swing to within 0.3V of the supply rails while delivering 20μA of output current. It should also be noted that, unlike the ICL7129, Maxim's ICL7129A/MAX7129 provides stable operation without the need for an additional capacitor between the Integrator Output and Common pins. The compensation cap used with the ICL7129 must be omitted for correct operation of the ICL7129A/MAX7129.

### X10 Amplifier

The X10 ("times ten") amplifier provides a precise gain of -10, without using any external components. This amplifier, unique to the "successive integrator" A/D, is used to multiply the residue left on the integrator capacitor after the $DE_1$ and $DE_2$ phases.

### Comparator

The comparator has the high gain and bandwidth needed to rapidly detect zero crossing. The comparator's output is used by the digital control logic to select the correct polarity for De-integration, and to gate clock pulses into the up/down results counter during the De-integration phases.

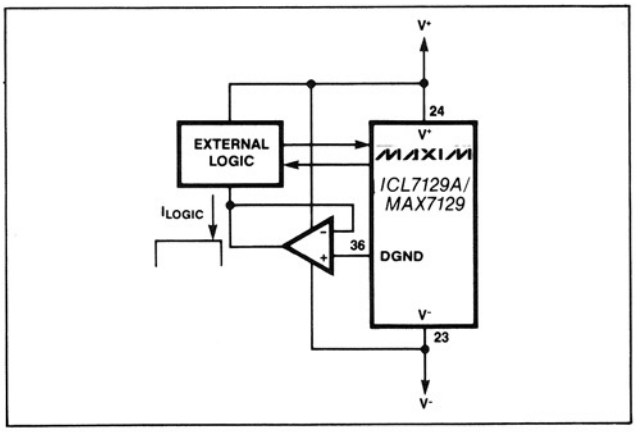


*Figure 11. DGND Buffer*

## Component Selection

### Integrating Resistor

Optimum linearity is obtained by choosing the integrating resistor value is chosen so that the buffer's maximum output current is between 5 and 20μA. The quiescent current of the buffer is 70μA, and can supply 13μA of output current with excellent linearity. The buffer's maximum output current occurs with a full scale input voltage, and the optimum value of integrating resistor can be calculated as:

$$R_{INT} = \frac{\text{full scale voltage}}{13\mu A} = \frac{2V}{13\mu A} = 150k\Omega$$

Too high a value for the integrating resistor increases the sensitivity to noise pickup and increases errors caused by stray leakage currents. Too low a value degrades integral linearity by attempting to draw more current from the buffer and integrator than they can provide without degrading linearity.

### Integrating Capacitor

The maximum swing of the integrator during the signal integrate phase can be calculated as

$$Vswing = \frac{I_{INT} \times T_{INT}}{C_{INT}}$$

where $I_{INT}$ = 13μA if $R_{INT}$ is chosen as described above and $T_{INT}$ = 1,000 clock periods (16.7ms for 120kHz oscillator frequency). The integrator swing range should be maximized while avoiding saturation of the integrator output. The integrator will not saturate unless its output is within 0.3V of either supply, but for the best integral linearity the integrator's output should remain at least 1V away from either supply. Since Common is a approximately 3V below $V^+$, the integrator swing should be 2V. Substituting these values in the above formula, $C_{INT}$ can now be calculated as:

$$C_{INT} = \frac{13.3\mu A \times 16.7ms}{2V} = 0.1\mu F$$

Too low a value for $C_{INT}$ increases integrator swing to the point where the integrator saturates and causes integral linearity errors. Too high a value for $C_{INT}$ reduces the integrator swing range and increases the effect of comparator noise. If a positive common mode voltage is applied to IN LO the value of $C_{INT}$ must be reduced to keep the integrator output voltage at least 1V below $V^+$.

The integrating capacitor must have low dielectric absorption to obtain low integral nonlinearity, rollover, and ratiometric errors. The result of measurements with the reference tied to the Input HI is a good indication of the amount of dielectric absorption in the integrator capacitor. A good integrating capacitor will result in a reading of 9999, and any deviation from this reading is probably due to dielectric absorption. Polypropylene capacitors have been found to be suitable, as have Teflon™ capacitors. In less critical applications polystyrene and polycarbonate capacitors may also be used.

### Reference Capacitor

The reference capacitor's dielectric absorption is rarely critical. Low dielectric absorption reference capacitors are required only where fast settling time is needed in systems with a rapidly changing reference voltage such as ratiometric ohms measurement in digital multimeters.

The reference capacitor must be a low leakage capacitor since it stores the reference voltage while floating during both the Integrate and De-integrate phases. Any leakage or charge loss during these phases causes a change in the scale factor of the ICL7129A/MAX7129. Low cost film capacitors such as polyester or polystyrene are suitable for most applications.

In addition to leakage requirements, another effect that sets a lower limit on the value of the reference capacitor is the "charge suckout" caused by stray capacitance on the reference capacitor terminals. In most applications the Ref Lo Input terminal is connected to Common, and the Ref Hi Input is 1V above Common. During the integration and idle phases the reference capacitor is connected to the Reference Inputs ($C_{REF}^+$ to Ref Hi and $C_{REF}^-$ to Ref Lo). At the end of the integration phase the comparator determines the polarity at the integrator output and the digital section closes analog switches so that the reference capacitor is connected to Common and the buffer input with a polarity such that the integrator output will return toward Common during the De-integrate phase. A negative input signal during the integrate phase drives the integrator output positive and the ICL7129A/MAX7129 digital section will connect the $C_{REF}^-$ terminal to Common during the De-integrate phase. Since the $C_{REF}^-$ terminal was also connected to Common during the Integrate phase, the $C_{REF}$ terminals do not change voltage during the transition from Integrate phase to De-integrate phase. If, however, the input voltage during the Integrate phase is positive, the ICL7129A/MAX7129 digital section will connect the Ref $Cap^+$ terminal to Common. In

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this case the two terminals of the reference capacitor both move 1V more negative. Any stray capacitance on the reference capacitor terminals must also be charged during the 1V movement, thereby reducing the voltage on the reference capacitor and changing the scale factor for positive input voltages. This error, called "rollover error" can be reduced to less than 1 count by using a reference capacitor value of 1μF or greater.

### Crystal Oscillator Components

The ICL7129A/MAX7129 crystal oscillator is designed to work with tuning fork type crystals such as the Statek CX-1V series. The two capacitors are not critical components and can be the low cost disc ceramic type. The crystal frequency should be 120kHz to reject 60Hz normal mode signals and 100kHz to reject 50Hz normal mode signals. With these crystal frequencies the integration will be 10 cycles of the 60/50Hz signal on the 200mV range and 1 cycle on the 2V range. There is no single oscillator frequency that results in good normal mode rejection of both 50Hz and 60Hz on the 2V range, but a 100kHz oscillator frequency will reject both 50Hz and 60Hz on the 200mV scale.

## Component Manufacturers

The following list of component suppliers is intended to be of assistance in identifying suitable external components for use with the ICL7129A/MAX7129. The list is not intended to be comprehensive, nor does it constitute an endorsement by Maxim of the companies listed.

### Triplexed Liquid Crystal Displays

Epson America, Inc., Torrance, CA.
(213) 534-4500
Part #: LD-H7960A

Crystaloid, Inc., Hudson, OH
(216) 655-2429

Hamlin, Inc., Lake Mills, WI
(414) 648-2361

UCE, Inc., Norwalk, CT
(203) 838-7509

LXD INC, Cleveland, OH
(216) 292-3300
Part #: 353E3/8R03H

Varitronix Limited, Los Angeles, CA
(213) 661-8883
Part #: VIM-503-DP

### Display Mounting Bezels

Techknits, Inc., Cranford, N.J.
(201) 272-5500

Conductive Rubber Technology, Santa Barbara, CA.
(805) 969-5807

### Crystals

Statek, Inc., Orange, CA
(714) 639-7810
Part #: CX-1V 120C

Saronix, Inc., Palo Alto, CA
(415) 856-6900

### Polypropylene Capacitors

West Lake Capacitors, West Lake Village, CA
(818) 889-4120

Seacor, Inc., Westwood, N.J.
(201) 666-5600

TRW Capacitors, Ogallala, NE
(308) 284-3611

Sprague Electric Co., North Adams, MA
(413) 664-4411

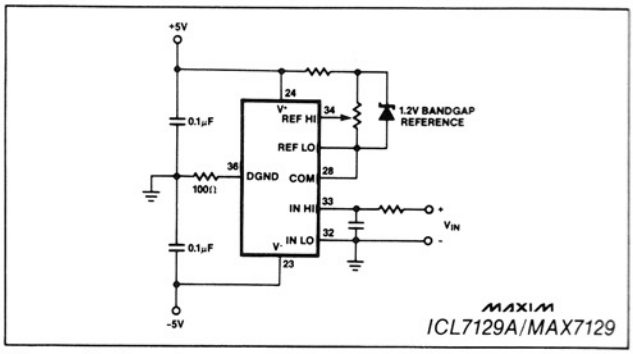


*Figure 12. Powering the ICL7129A/MAX7129 from +5V and -5V Power Supplies*

## Applications

### Power Supply

The ICL7129A/MAX7129 may be operated as a battery powered hand-held instrument or integrated into larger systems that have more sophisticated power supplies.

The standard battery connection using a 9V battery is shown in the Typical Operating Circuit on the front page of this data sheet.

Figure 12 shows the power connection for systems with +5V and -5V supplies. Note that measurements are given with respect to ground. COMMON is not connected to INPUT LO and is used only as a pre-regulator for the external voltage reference. Digital ground of the ICL7129A/MAX7129 (DGND, pin 36) is not directly connected to power supply ground. The ICL7129A/MAX7129's digital inputs have protective diodes to DGND and should not be driven to any voltage below DGND. This problem is handled by placing a 100Ω resistor between the ICL7129A/MAX7129's DGND terminal and the ±5V system's digital ground, which pulls down the ICL7129A/MAX7129's DGND terminal if it reaches a voltage more positive than the ±5V system's digital ground. This prevents the forward biasing of the input protection diodes. If DGND voltage is more negative than the system digital ground the 10Ω resistor will limit the amount of current that DGND sinks.

A power supply with single polarity can be used to power the ICL7129A/MAX7129 in applications where battery operation is not convenient or appropriate. Measurements must be made with respect to COMMON or some other voltage within the ICL7129A/MAX7129's input common mode range.

### Voltage References

The Common output has a typical temperature coefficient of ±80ppm/°C. Since the ICL7129A/MAX7129 has a resolution of 1 count in 20,000 or 50ppm, a precision external reference is needed unless the ambient temperature is held constant. The diagram of the Typical Operating Circuit on the front page of this data sheet shows a 1.2V bandgap voltage source used as the reference for the ICL7129A/MAX7129, with Common used only as a pre-regulator for the bandgap

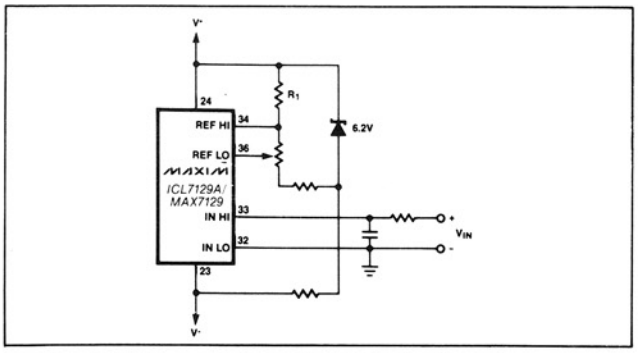


*Figure 13. Using a 6.2V Reference Diode with the ICL7129A/MAX7129.*

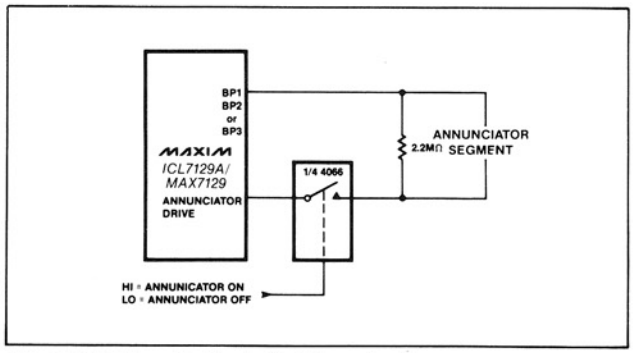


*Figure 14. Externally Controlled Annunicators*

reference. The ICL7129A/MAX7129 reference voltage is approximately 1.000V for both 2V and 200mV full-scale operation. To trim the reference voltage, first apply a precision 1000.05mV input voltage, then adjust the reference voltage until the display reading alternates equally between 10000 and 10001.

Figure 13 shows the ICL7129A/MAX7129 with an external 6.8V zener reference voltage.

### Annunciator Drivers

The Annunciator Drive output is a square wave at the backplane frequency, swinging from $V^+$ to $V_{DISP}$. Any segment connected to Annunciator Drive will be turned on, regardless of which backplane drives that segment. Figure 14 shows how to control annunciator segments with external logic levels.

### Display Voltage Compensation

An adequate display can be obtained in most applications by connecting $V_{DISP}$ (pin 19) to DGND (pin 36). In applications where a wide temperature range is expected, the voltage drive levels for some triplexed liquid crystal displays may need to vary with temperature in order to maintain good display contrast and viewing angle. The amount of temperature compensation will depend upon the type of liquid crystal used. Display manufacturers usually specify the temperature variation of the LCD threshold voltage, which is approximately 1/3 of the optimum peak display voltage. The peak display voltage is equal to ($V^+ - V_{DISP}$), so a typical -4mV/°C temperature coefficient of an LCD threshold corresponds to a +12mV/°C temperature coefficient at the $V_{DISP}$ pin. Two circuits that can be adjusted to give a temperature compensation of approximately +12mV/°C at $V_{DISP}$ are shown in Figure 15. The diode between DGND and $V_{DISP}$ should have a low turn-on voltage to ensure that $V_{DISP}$ is never driven more than 300mV negative with respect to DGND.

### Input Protection

The input pins of the ICL7129A/MAX7129 have protection diodes built in to protect it from electrostatic discharges (ESD) of up to 2000V (Mil Standard 883, Method 3015.1 test circuit). These diodes also protect the ICL7129A/MAX7129 from excessive input voltage overload in multimeter circuits, provided that the current into these diodes is limited to less than 1mA. The ICL7129A/MAX7129 will therefore be fully protected for input voltages up to 1000V if the input current limiting resistor is 1MΩ.

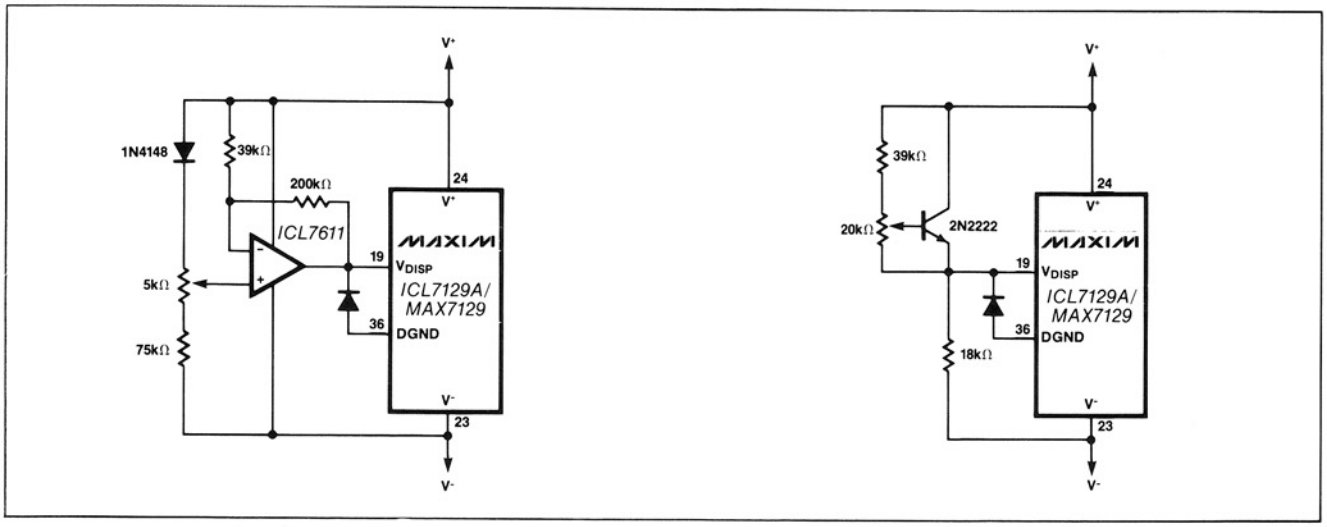


*Figure 15. $V_{DISP}$ Temperature Compensation*

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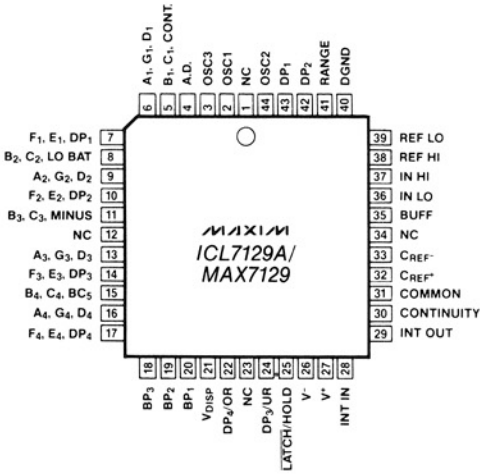
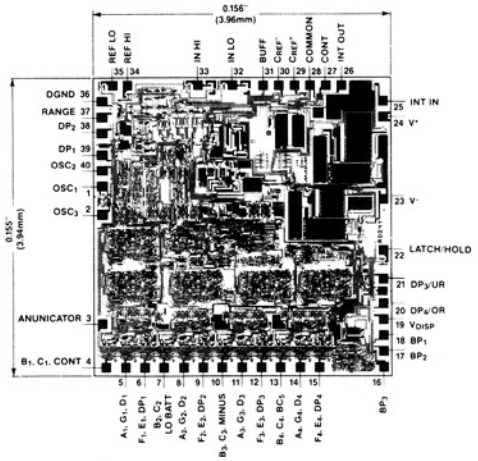
## Pin Configuration




**44 Lead Plastic Chip Carrier (Quad Pak)**

## Chip Topography




**Substrate is Connected to V+.**