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Data Sheet | March 4, 2010 | FN3403.5

Dual, Low Power CMOS Operational Amplifiers

The ICL761X/762X series is a family of monolithic CMOS operational amplifiers. These devices provide the designer with high performance operation at low supply voltages and selectable quiescent currents. They are an ideal design tool when ultra low input current and low power dissipation are desired.

The basic amplifier will operate at supply voltages ranging from ±1V to ±8V, and may be operated from a single Lithium cell. The output swing ranges to within a few millivolts of the supply voltages.

The quiescent supply current of these amplifiers is set to 100µA at the factory. This results in power consumption as low as 200µW per amplifier.

Of particular significance is the extremely low (1pA) input current, input noise current of 0.01pA/$\sqrt{Hz}$, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

The inputs are internally protected. Outputs are fully protected against short circuits to ground or to either supply.

Because of the low power dissipation, junction temperature rise and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7621DCPA	7621 DCPA	0 to +70	8 Ld PDIP - D Grade - I_Q = 100µA	E8.3
ICL7621DCPAZ* (Note 2)	7621 DCPAZ	0 to +70	8 Ld PDIP - D Grade - I_Q = 100µA	E8.3
ICL7621DCBA (Note 1)	7621 DCBA	0 to +70	8 Ld SOIC - D Grade - I_Q = 100µA	M8.15
ICL7621DCBAZ (Notes 1, 2)	7621 DCBAZ	0 to +70	8 Ld SOIC - D Grade - I_Q = 100µA	M8.15

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTES:

1. Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

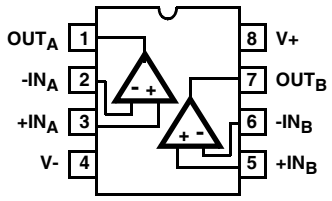
- Wide Operating Voltage Range . . . . . ±1V to ±8V
- High Input Impedance . . . . . $10^{12}\Omega$
- Input Current Lower Than BIFETs . . . . . 1pA (Typ)
- Output Voltage Swing . . . . . V+ and V-
- Available as Duals (Refer to ICL7611 for Singles)
- Low Power Replacement for Many Standard Op Amps

Applications

- Portable Instruments
- Telephone Headsets
- Hearing Aid/Microphone Amplifiers
- Meter Amplifiers
- Medical Instruments
- High Impedance Buffers

Pinouts

ICL7621
(8 LD PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage V+ to V- 18V
Input Voltage . . . . . V- -0.3 to V+ +0.3V
Differential Input Voltage (Note 3) . . . . . [(V+ +0.3) - (V- -0.3)]V
Duration of Output Short Circuit (Note 4). . . . . Unlimited

Operating Conditions

Temperature Range . . . . . 0°C to +70°C

Thermal Information

Thermal Resistance (Typical, Note 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PDIP Package	120	N/A
SOIC Package	160	N/A

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. Long term offset voltage stability will be degraded if large input differential voltages are applied for long periods of time.
4. The outputs may be shorted to ground or to either supply, for $V_{SUPPLY} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.
5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm 5V$, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Input Offset Voltage	V_{OS}	$R_S \leq 100k\Omega$	+25	-	-	15	mV
			Full	-	-	20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \leq 100k\Omega$	-	-	25	-	$\mu V/^oC$
Input Offset Current	I_{OS}		+25	-	0.5	30	pA
			0 to +70	-	-	300	pA
			-55 to +125	-		800	pA
Input Bias Current	I_{BIAS}		+25	-	1.0	50	pA
			0 to +70	-	-	400	pA
			-55 to +125	-	-	4000	pA
Common Mode Voltage Range	V_{CMR}	$I_Q = 100\mu A$	+25	± 4.2	-	-	V
Output Voltage Swing	V_{OUT}	$I_Q = 100\mu A$, $R_L = 100k\Omega$	+25	± 4.9	-	-	V
			0 to +70	± 4.8	-	-	V
			-55 to +125	± 4.5	-	-	V
Large Signal Voltage Gain	A_{VOL}	$V_O = \pm 4.0V$, $R_L = 100k\Omega$, $I_Q = 100\mu A$	+25	80	102	-	dB
			0 to +70	75	-	-	dB
			-55 to +125	68	-	-	dB
Unity Gain Bandwidth	GBW	$I_Q = 100\mu A$	+25	-	0.48	-	MHz
Input Resistance	R_{IN}		+25	-	10^{12}	-	Ω
Common Mode Rejection Ratio	CMRR	$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	+25	70	91	-	dB
Power Supply Rejection Ratio ($V_{SUPPLY} = \pm 8V$ to $\pm 2V$)	PSRR	$R_S \leq 100k\Omega$, $I_Q = 100\mu A$	+25	80	86	-	dB
Input Referred Noise Voltage	e_N	$R_S = 100\Omega$, f = 1kHz	+25	-	100	-	$nV/\sqrt{Hz}$
Input Referred Noise Current	i_N	$R_S = 100\Omega$, f = 1kHz	+25	-	0.01	-	$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPPLY}	No Signal, No Load, $I_Q = 100\mu A$	+25	-	0.1	0.25	mA
Channel Separation	V_{O1}/V_{O2}	$A_V = 100$	+25	-	120	-	dB

Electrical Specifications V_{SUPPLY} = ±5V, Unless Otherwise Specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	TEMP. (°C)	MIN (Note 6)	TYP	MAX (Note 6)	UNITS
Slew Rate	SR	A_V = 1, C_L = 100pF, V_{IN} = 8V_{P-P}, I_Q = 100µA, R_L = 100kΩ	+25	-	0.16	-	V/µs
Rise Time	t_R	V_{IN} = 50mV, C_L = 100pF, I_Q = 100µA, R_L = 100kΩ	+25	-	2	-	µs
Overshoot Factor	OS	V_{IN} = 50mV, C_L = 100pF, I_Q = 100µA, R_L = 100kΩ	+25	-	10	-	%

NOTE:

6. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Schematic Diagram

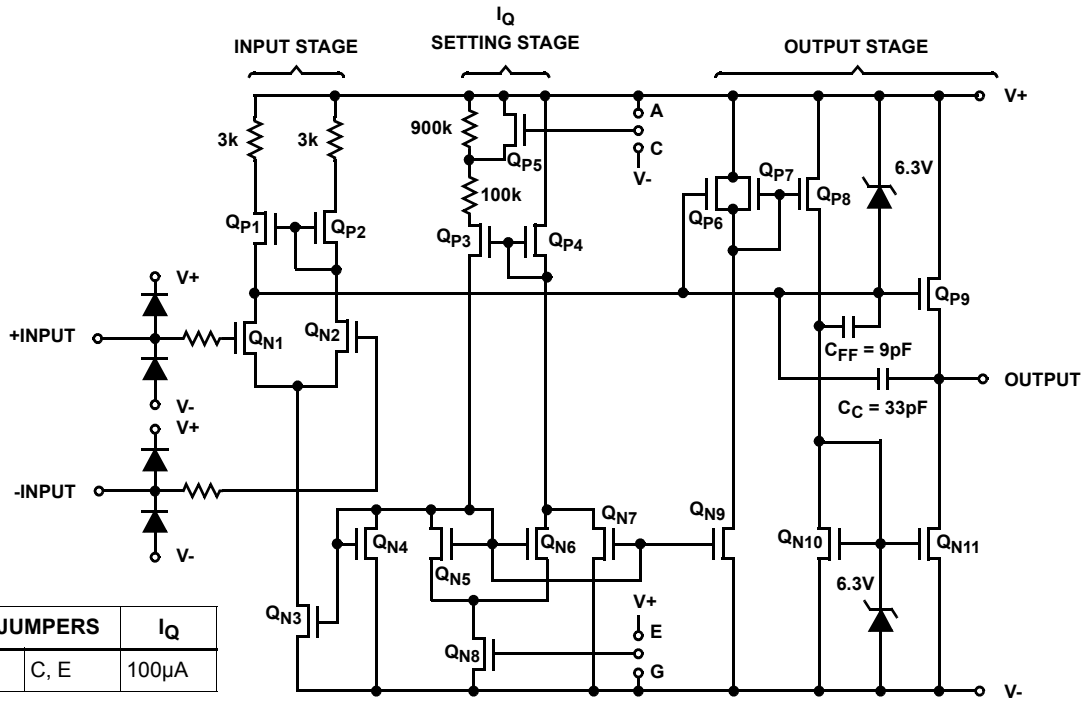


TABLE OF JUMPERS		I_Q
ICL7621	C, E	100µA

Application Information

Static Protection

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

Latchup Avoidance

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (PNPN) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2mA to prevent latchup.

Choosing the Proper I_Q

Each device in the ICL76XX family has a similar I_Q setup scheme, which allows the amplifier to be set to nominal quiescent currents of 10µA, 100µA or 1mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. The ICL7621 has a fixed I_Q setting of 100µA.

Output Stage and Load Driving Considerations

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1MΩ, 100kΩ, and 10kΩ, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB for higher output currents (see graphs in "Typical Performance Curves" beginning on page 6). During the transition from Class A to Class B operation, the output transfer characteristic is nonlinear and the voltage gain decreases.

Frequency Compensation

The ICL76XX are internally compensated, and are stable for closed loop gains as low as unity with capacitive loads up to 100pF.

Typical Applications

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

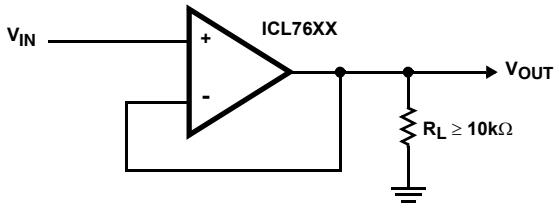


FIGURE 1. SIMPLE FOLLOWER

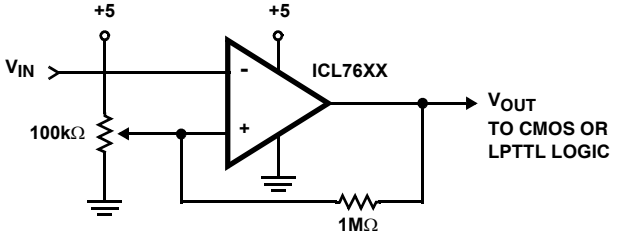
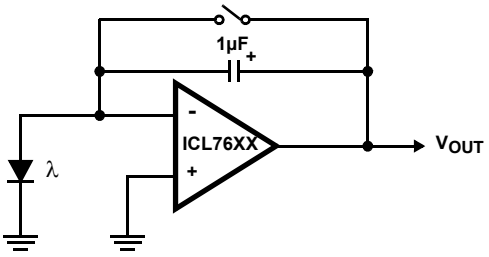
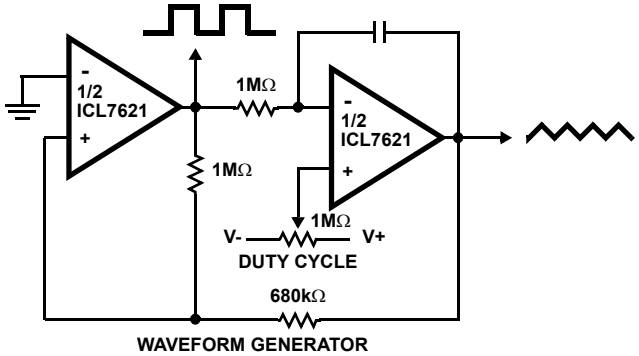


FIGURE 2. LEVEL DETECTOR



NOTE: Low leakage currents allow integration times up to several hours.

FIGURE 3. PHOTOCURRENT INTEGRATOR



WAVEFORM GENERATOR

NOTE: Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

FIGURE 4. TRIANGLE/SQUARE WAVE GENERATOR

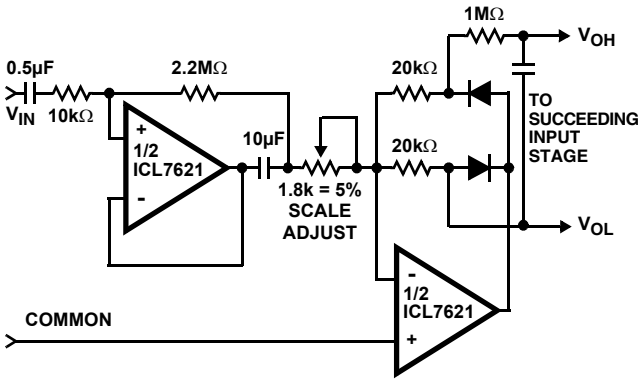


FIGURE 5. AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, ICL7107, ICL7109, ICL7116, ICL7117

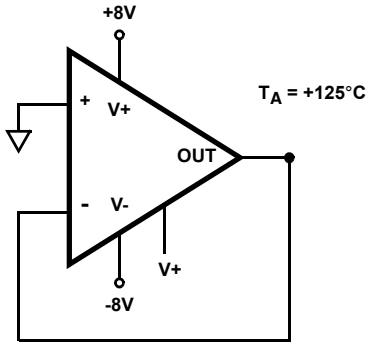
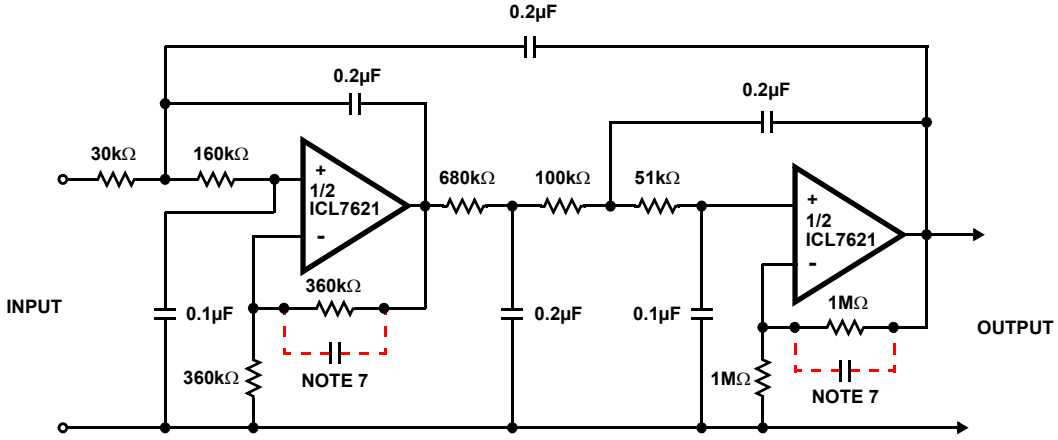


FIGURE 6. BURN-IN AND LIFE TEST CIRCUIT



NOTES:

7. Small capacitors (25pF to 50pF) may be needed for stability in some cases.
8. The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff. f_C = 10Hz, AV_{CL} = 4, Passband ripple = 0.1dB.

FIGURE 7. FIFTH ORDER CHEBYCHEV MULTIPLE FEEDBACK LOW PASS FILTER

Typical Performance Curves

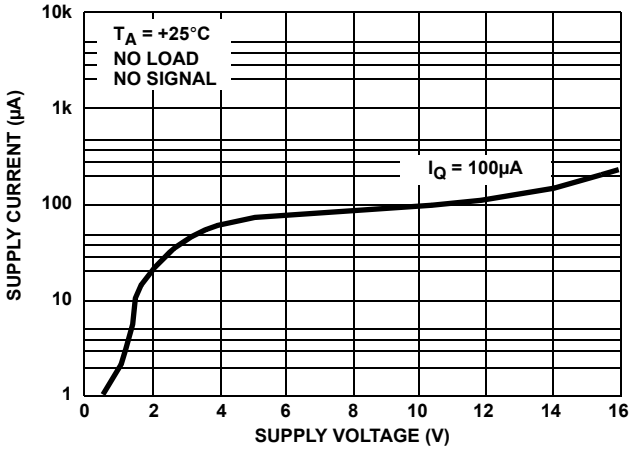


FIGURE 8. SUPPLY CURRENT PER AMPLIFIER vs SUPPLY VOLTAGE

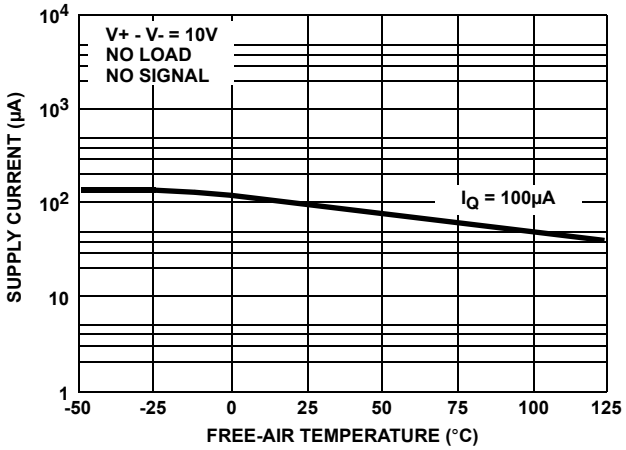


FIGURE 9. SUPPLY CURRENT PER AMPLIFIER vs FREE-AIR TEMPERATURE

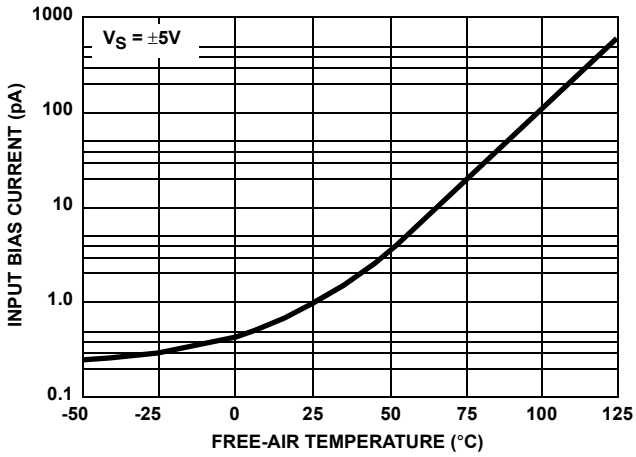


FIGURE 10. INPUT BIAS CURRENT vs TEMPERATURE

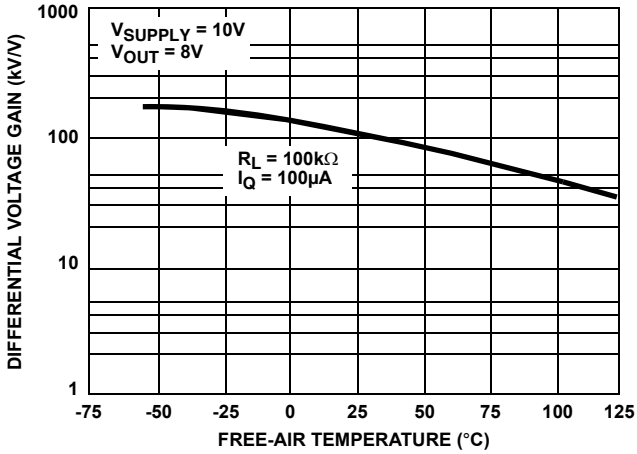


FIGURE 11. LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN vs FREE-AIR TEMPERATURE

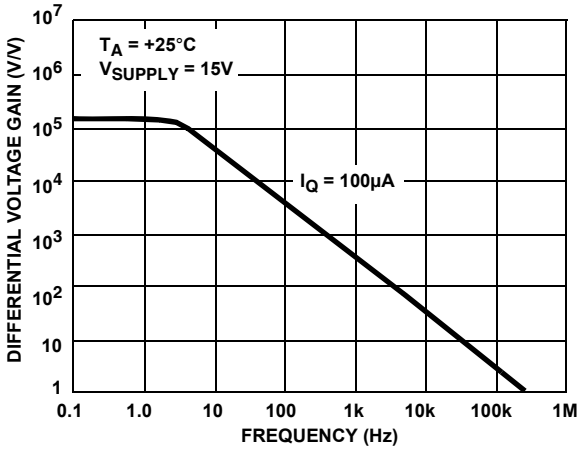


FIGURE 12. LARGE SIGNAL FREQUENCY RESPONSE

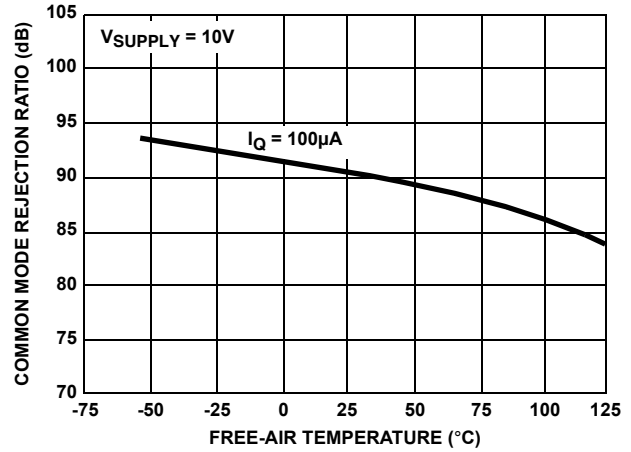


FIGURE 13. COMMON MODE REJECTION RATIO vs FREE-AIR TEMPERATURE

Typical Performance Curves (Continued)

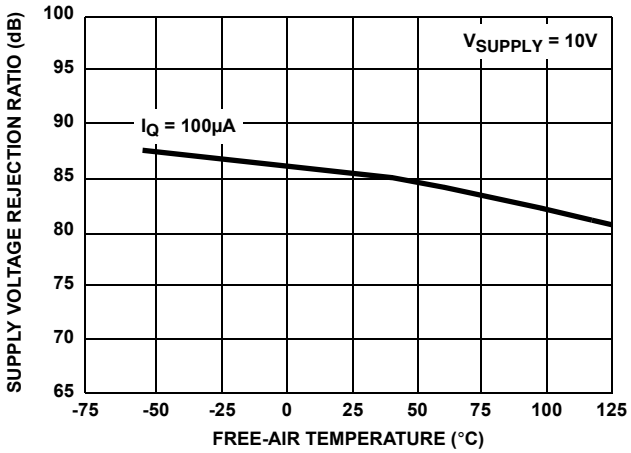


FIGURE 14. POWER SUPPLY REJECTION RATIO vs FREE-AIR TEMPERATURE

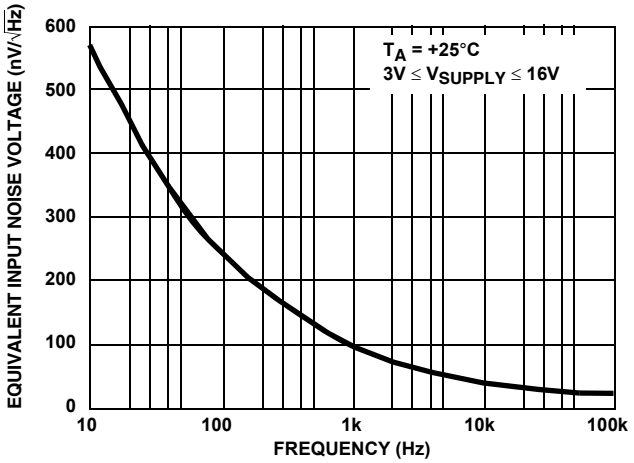


FIGURE 15. EQUIVALENT INPUT NOISE VOLTAGE vs FREQUENCY

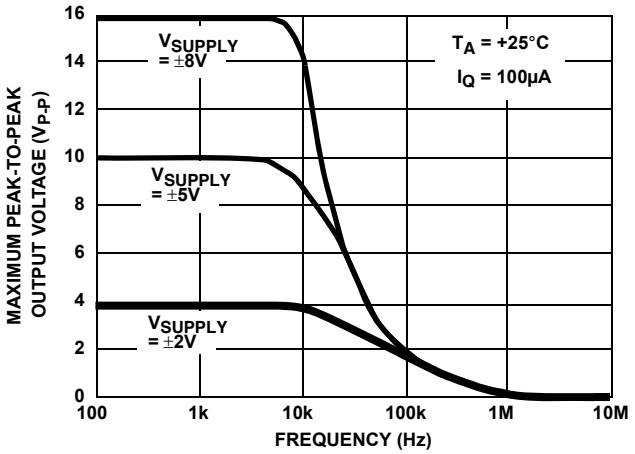


FIGURE 16. OUTPUT VOLTAGE vs FREQUENCY

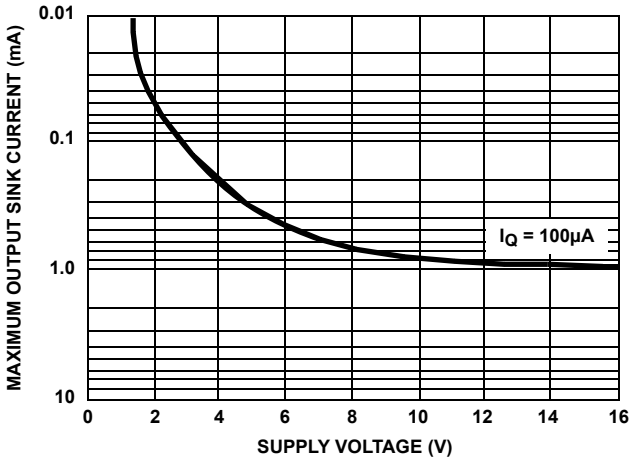


FIGURE 17. OUTPUT SINK CURRENT vs SUPPLY VOLTAGE

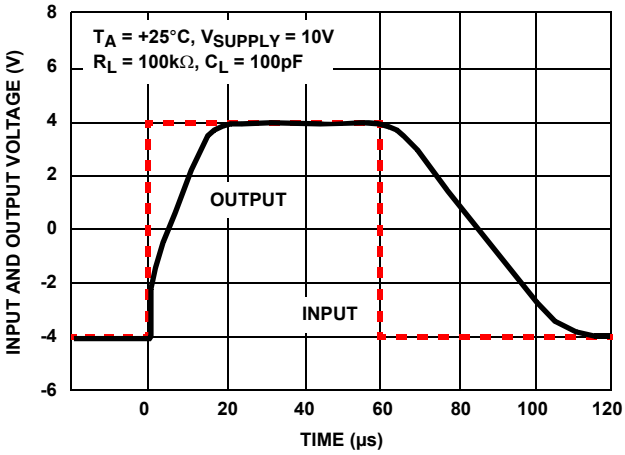
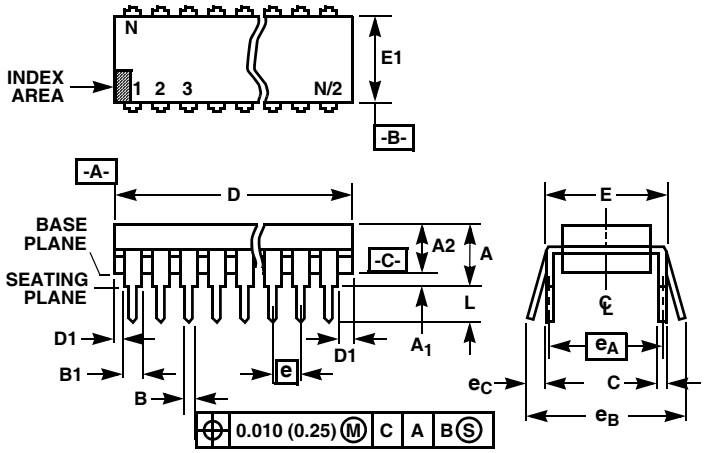


FIGURE 18. VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE (I_Q = 100µA)

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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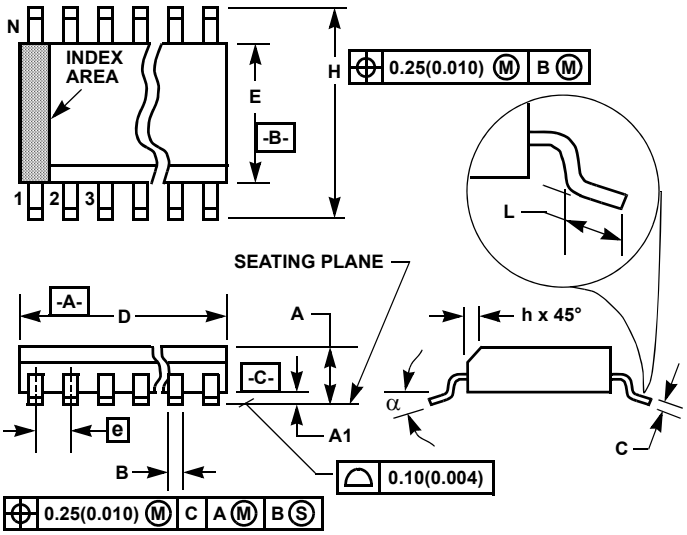
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0°	8°	0°	8°	-

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