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# ICL8105 - Digital Flyback Controller IC

XDP™ digital power

Datasheet

## About this document

### Scope and purpose

This document contains information about Infineon high-performance single-stage digital flyback controller ICL8105 for LED lighting applications. Features and electrical characteristics are listed and explained.

### Intended audience

This document is intended for customers wishing to design high-performance single-stage digital flyback AC-DC converters for LED lighting based on the ICL8105 controller

## Revision History

| <b>Revision History</b>     |  |
|-----------------------------|--|
| <b>Page or Item</b>         | <b>Subjects (major changes since previous revision)</b>  |
| <b>Rev. 2.0, 2016-08-01</b> |  |
| Cover page                  | Change “.dp digital power 2.0” to “XDP™ digital power”.  |
| Page 4 & 5                  | Added product highlight & schematic for primary side micro-controller dimming application. Updated schematic for secondary side 0-10V dimming application from using dimming transformer to CDM10V.  |
| Page 6                      | Updated pin SQW, ZCD definition and function in Table 2.   |
| Page 7                      | Updated Section 2.1 to introduce “ICL8105 supports primary side micro-controller dimming application”  |
| Section 2.2.4               | Updated Figure 9 and description for parameter naming correction from I <sub>out_min</sub> to I <sub>out_dim_min</sub> . Added note to indicate V <sub>dim_max</sub> is fixed at 1.72V.  |
| Section 2.2.5               | Updated description and figure for isolated dimming interface circuitry from using dimming transformer to CDM10V   |
| Section 2.2.6               | Updated section title from “output voltage” to “output load voltage”. Added description to indicate wide output load voltage range condition (more than 2 times of the minimum output load voltage)  |
| Section 2.2.7               | Updated application note description for the auto-discharge circuit reference.   |
| Section 2.2.9               | Added footnote for parameter n <sub>ss</sub>   |
| Section 2.3                 | Table 4: Changed UVLO protection reaction from “auto-restart” to “hardware restart” and added note for VCC overvoltage protection reaction to indicate it is configurable. Added startup output undervoltage protection for V <sub>out</sub> . Updated Section 2.3.3 description.  |
| Section 2.4.1               | Added description about ICL8105 excel tool and changed description from 40W form factor board to 40W reference design with CDM10V  |
| Section 2.4.2               | Updated example value and configuration range of parameters in Table 5. Moved t <sub>min_demag</sub> from fine-tuning section to multimode section in Table 5. Moved parameter Reaction_VCCP, a_DIM, N_DCM_MOD_GAIN, V_DIM_MIN & V_DIM_OFF, from Table 6 to Table 5, Moved parameter V <sub>outUV</sub> from Table 5 to Table 6, Changed parameter V_GD value (from 9V to 10.5V), Changed parameter naming from EN_STOP to Debug_mode. Added parameter f_DCM_init and remove parameter EN_EPFC. Added selection of “Narrow_24.9V” for parameter V <sub>CC_SUPPLY</sub> . |
| Page 24                     | Added section 2.4.3 about “Debug mode support”.  |
| Table 10                    | Added row with Ta(max) =105 °C, Tj(max) =150 °C, Added note of Ta(max), Tj(max) limit based on f <sub>sw_max</sub> setting   |
| Table 11                    | Added row with t <sub>MCLK</sub> (typ) = 20.9ns, Added note of t <sub>MCLK</sub> (typ) selection based on f <sub>sw_max</sub>  |
| Table 15                    | Added V_OCP1 tolerance based on lower V_OCP1 setting range. Added V_OCP2 selection of 0.6V and changed the range of V_OCP1 in the note for V_OCP2 selection  |
| Table 16                    | Changed V_GD typical value from 9.0V to 10.5V  |

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## Overview

### Product highlights

- Highly accurate primary side controlled output current (Line/load regulation typical within +/- 3%)
- High power quality (typical PF up to 0.99 and THD < 10%)
- High Efficiency (up to 91%)
- Configurable output current with no BOM change
- Supports universal input voltage (85 – 305 V AC)
- Supports wide output load voltage (up to 4 times of minimum output load voltage)
- Ideal for application with dimming signal from micro-controller on primary side
- Supports fully isolated 0 – 10 V dimming with Infineon CDM10V
- Supports low output current dimming.
- Low standby power

### Features

- Single stage QR Flyback with PFC and high precision primary side controlled constant current output
- Excellent line and load regulation
- Supports AC input (45 ~ 65 Hz) and/or DC input voltage operation
- Integrated 600 V startup cell
- Low Bill Of Material (BOM)
- Configurable parameters, e.g. adjustable voltage and current ranges, protection modes
- Supports non-dimmed and/or dimmed applications.
- Intelligent thermal management with adaptive thermal protection

### Applications

- Electronic control gear for LED luminaires (5 W to 80 W)

### Description

The ICL8105 is a high performance microcontroller-based digital single-stage flyback controller with power factor correction (PFC) for constant output current applications. The IC is available in a DSO-8 package and supports a wide feature set, requiring a minimum of external components. The digital engine offers the possibility to configure operational parameters and protection modes, which helps to ease the design phase and allows a reduced number of hardware variants in production. Accurate primary side output current control is implemented to eliminate the need for secondary side feedback circuitry.

**Table 1**

| Product Type | Package  |
|--------------|----------|
| ICL8105      | PG-DSO-8 |

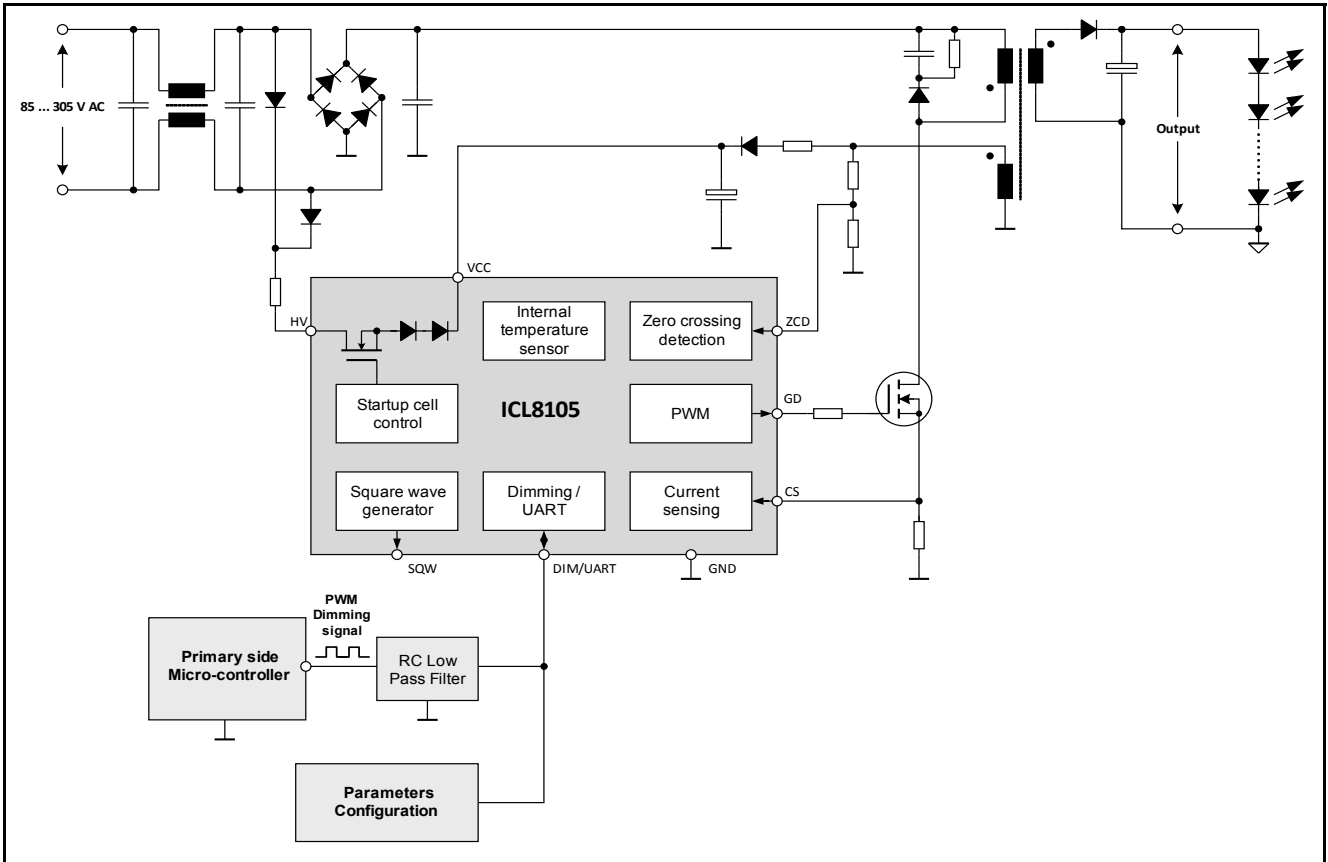


Figure 1 Typical application 1 (Primary side micro-controller dimming)

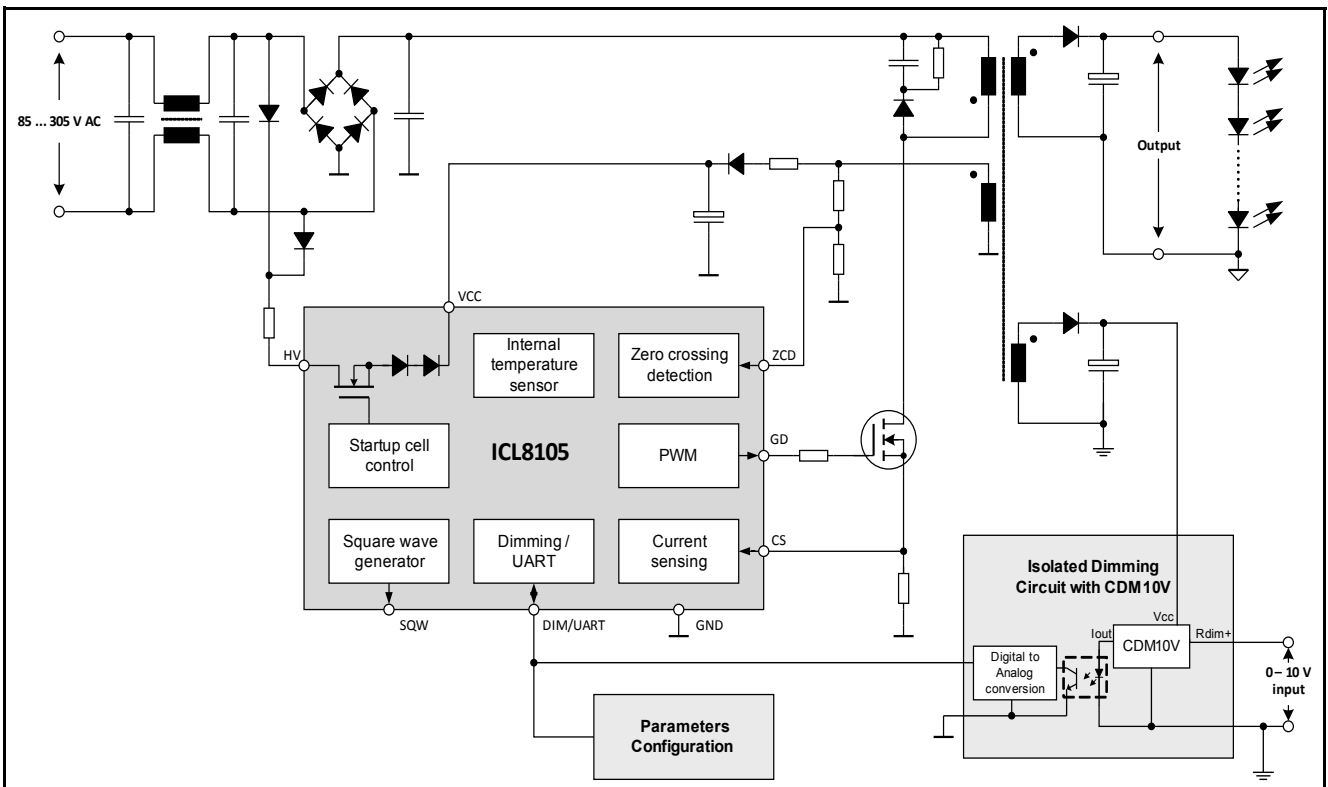
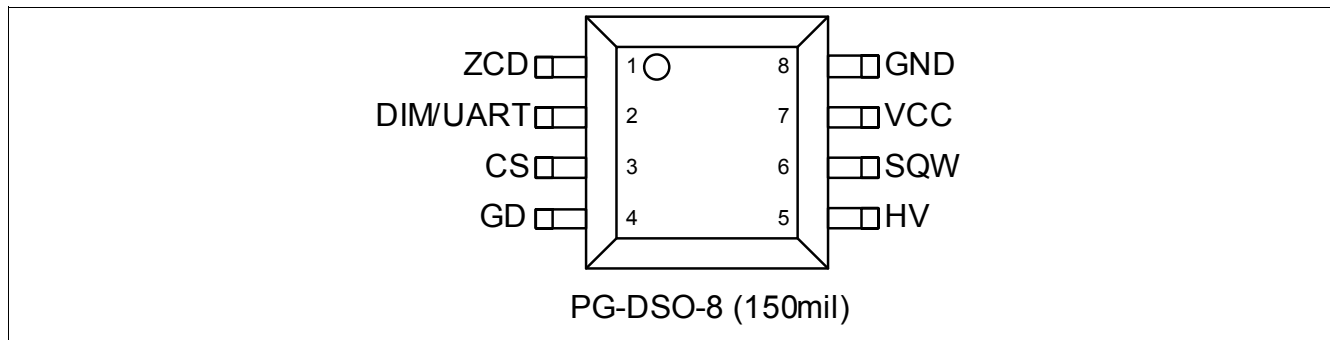


Figure 2 Typical application 2 (Secondary side 0-10V dimming)

Pin configuration and description

## 1 Pin configuration and description

The pin configuration is shown in **Figure 3**. The pin functions are listed and described in **Table 2**.



**Figure 3** Pin configuration

**Table 2** Pin definitions and functions

| Symbol   | Pin | Type | Function  |
|----------|-----|------|---|
| ZCD      | 1   | I    | <b>Zero crossing detection</b><br>Pin ZCD is connected to an auxiliary winding via the resistor divider for zero crossing detection. Output & input voltage are also measured with the sampled positive & negative voltage sensing.   |
| DIM/UART | 2   | I/O  | <b>Dimming / UART</b><br>Shared functioning pin with either as dimming Input or UART configuration. The dimming input voltage, $V_{DIM}$ sensing range is from 0.1 to 2V. Once the pin voltage exceeds 2.2V (for example when the isolated USB interface board is connected to the IC), this pin will function as UART configuration and the IC will stay in non-dimming operation unless it is reset or restarted. |
| CS       | 3   | I    | <b>Current sense</b><br>Pin CS is connected to an external shunt resistor and the source of the power MOSFET.   |
| GD       | 4   | O    | <b>Gate driver</b><br>Output signal to drive an external power MOSFET.  |
| HV       | 5   | I    | <b>High voltage</b><br>Pin HV is connected to the rectified input voltage via external resistor. An internal 600 V HV startup-cell is used to pre-charge VCC for IC startup once the mains input voltage is applied. Furthermore sampled high voltage sensing is used for synchronization with the input voltage frequency.   |
| SQW      | 6   | O    | <b>Square wave generator</b><br>Pin SQW is capable of providing a square wave signal for driving the isolated dimming transformer circuit, if necessary. Otherwise, this signal can be turned off by configuration.   |
| VCC      | 7   | I    | <b>Voltage supply</b><br>IC power supply  |
| GND      | 8   | —    | <b>Power and signal ground</b>  |

**Functional description**

## **2 Functional description**

The functional description provides an overview about the integrated functions and features as well as their relationship. The mentioned parameters and equations are based on typical values at  $T_A = 25^\circ\text{C}$ . The corresponding min. and max. values are shown in the electrical characteristics.

### **2.1 Introduction**

The ICL8105 is a digital AC/DC flyback controller with Power Factor Correction (PFC). The PFC function enables a rectified sinusoidal input current waveform with a power factor typically up to 0.99 and THD < 10% for a wide range of operating conditions. ICL8105 provides primary side constant output current control that avoids the secondary side control feedback loop circuitry usually needed in isolated power converters. This approach supports a low part count that is necessary to build up the application. ICL8105 has multi-mode operations and it selects the best mode of operation based on operating conditions. The multi-mode operation will automatically switch between quasi-resonant mode (QRM) and discontinuous mode (DCM) and active burst mode (ABM). In addition, ICL8105 supports both secondary side 0 - 10 V dimming and primary side micro-controller dimming application. Digital and RF interfaces can be supported by a microcontroller using a digital-to-analog converter.

The ICL8105 provides a high flexibility in the design-in of the application. A graphic user interface (GUI) tool supports users to tune a set of configurable parameters. The configuration can be done via a single pin UART interface at pin DIM/UART.

### **2.2 Controller features**

**Table 3** gives an overview about the controller features that are described in the mentioned chapters.

**Table 3 Controller features**

|   |                       |
|---|-----------------------|
| <b>Primary side voltage and current sensing</b>                     | <b>Chapter 2.2.1</b>  |
| <b>Primary side control scheme for output current control</b>       | <b>Chapter 2.2.2</b>  |
| <b>Power factor correction (PFC)</b>                                | <b>Chapter 2.2.3</b>  |
| <b>Dimming via pin DIM/UART</b>                                     | <b>Chapter 2.2.4</b>  |
| <b>Isolated dimming interface with CDM10V (optional)</b>            | <b>Chapter 2.2.5</b>  |
| <b>Wide output load voltage range circuit (optional)</b>            | <b>Chapter 2.2.6</b>  |
| <b>Automatic output discharge circuit (optional)</b>                | <b>Chapter 2.2.7</b>  |
| <b>VCC startup function combined with direct input monitoring</b>   | <b>Chapter 2.2.8</b>  |
| <b>Configurable soft start</b>                                      | <b>Chapter 2.2.9</b>  |
| <b>Configurable gate voltage rising slope at pin GD (Lower EMI)</b> | <b>Chapter 2.2.10</b> |



Functional description

2.2.1 Primary side voltage and current sensing

The ICL8105 provides a primary side control of the output current by means of measuring the input peak current and measuring the conduction period of the output diode. Input and output voltages are measured at pin ZCD using an external resistor divider and an auxiliary winding of the transformer. The voltage signal  $V_{AUX}$  contains the information of the rectified input voltage  $V_{in}$  and the output voltage  $V_{out}$  at the secondary side. **Figure 4** shows typical current and voltage waveforms of the Quasi-Resonant flyback application.

The following topics are described:

- Input current sensing via pin CS and output current calculation (**Chapter 2.2.1.1**)
- Input voltage sensing via pin ZCD (**Chapter 2.2.1.2**)
- Output voltage sensing via pin ZCD (**Chapter 2.2.1.3**)

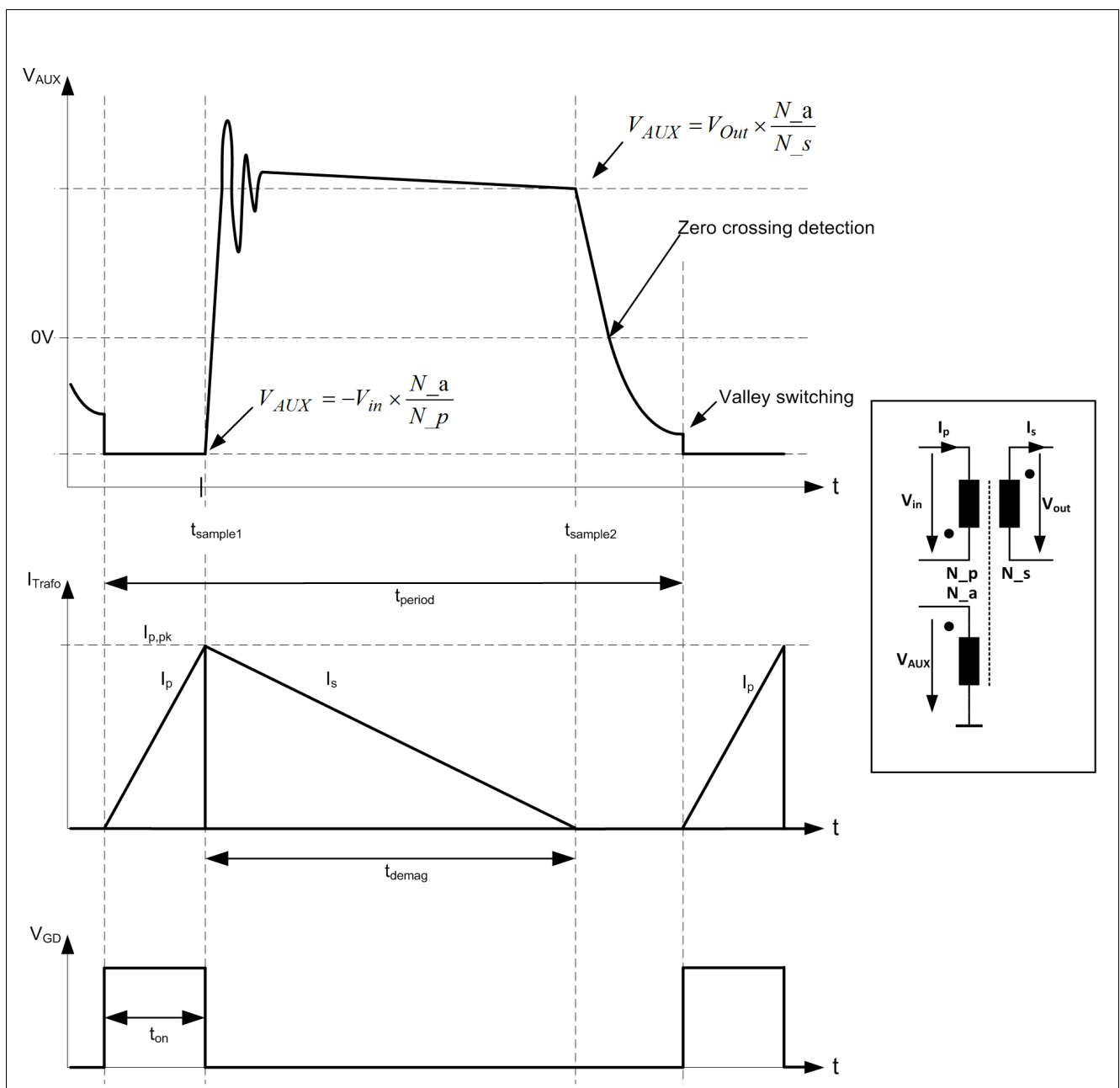


Figure 4 Typical waveforms (Example with QRM valley switching)

Functional description

2.2.1.1 Input current sensing via pin CS and output current calculation

The output current  $I_{out}$  is determined by the primary input peak current  $I_{p,pk}$  which is sensed at pin CS at time  $t_{sample1}$ , by the duration of conduction of the output diode ( $t_{sample2} - t_{sample1}$ ) and by the switching period  $t_{period}$ . The result is used for the control loop and for output overcurrent protections (Chapter 2.3.7).

2.2.1.2 Input voltage sensing via pin ZCD

The input voltage is measured using current  $I_{IV}$  at pin ZCD at time  $t_{sample1}$ . As the voltage  $V_{AUX}$  is a negative voltage, pin ZCD is clamped to a fixed negative voltage  $V_{INPCLN}$  (Figure 5). The negative current  $I_{IV}$  (flowing out of pin ZCD) is proportional to the input voltage. The monitored input voltage is used for input over- and undervoltage protection (Chapter 2.3.4).

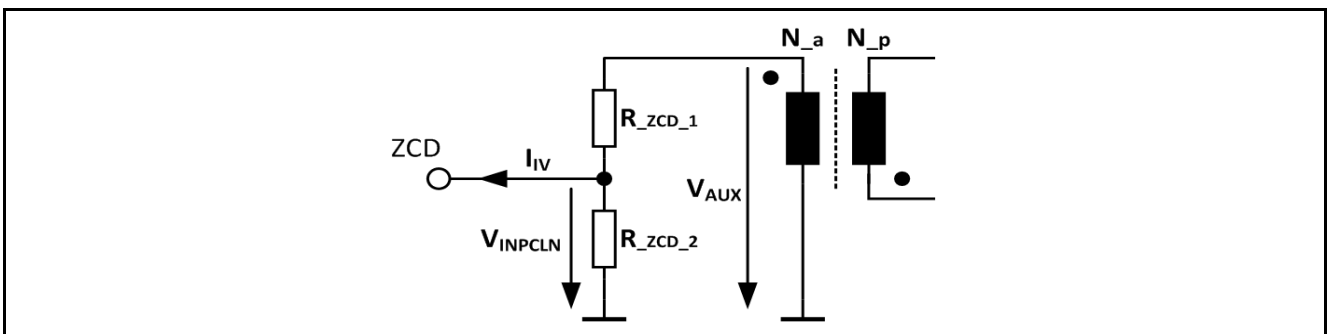


Figure 5 Input voltage sensing via pin ZCD

2.2.1.3 Output voltage sensing via pin ZCD

The output voltage is measured using voltage  $V_{ZCDSH}$  at pin ZCD at time  $t_{sample2}$  (Figure 6). The measured voltage at pin ZCD and the dimensioning of the resistor divider are used to calculate the reflected output voltage  $V_{out,aux}$  at the auxiliary winding.  $V_{out,aux}$  is used for output over- and undervoltage protection (Chapter 2.3.3). The relation between VCC and ZCD can be decoupled by adding a regulator for VCC (Chapter 2.2.6).

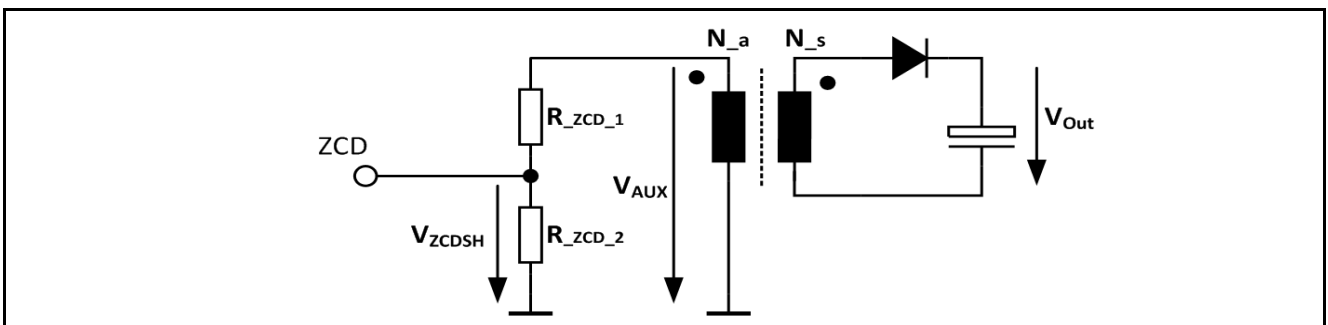


Figure 6 Output voltage sensing via pin ZCD

Note: Please note that the time ( $t_{sample2} - t_{sample1}$ ) has to be longer than  $2.0 \mu s$  to ensure that the reflected output voltage can be correctly sensed at pin ZCD!

Functional description

2.2.2 Primary side control scheme for output current control

The basic control scheme for the primary side constant current control is shown in Figure 7.

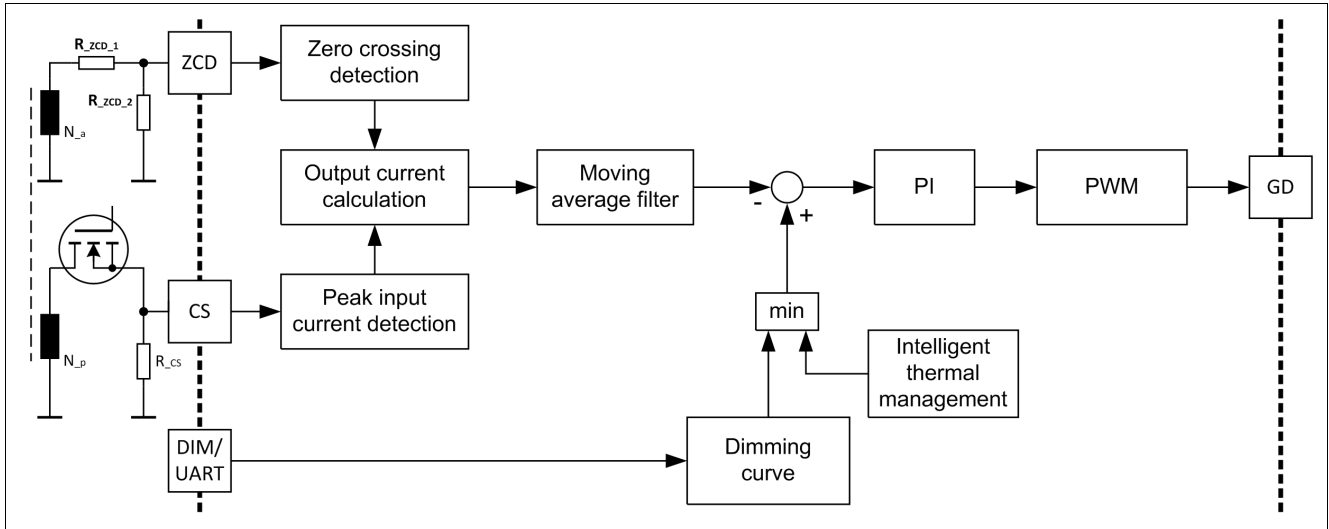


Figure 7 Integrated PI control scheme for output current control

The sampled signal  $V_{CS}$  at pin CS is used to estimate the output current  $I_{out}$  as described in Chapter 2.2.1.1. The internal reference current  $I_{out\_set}$  is weighted according to thermal management and dimming curve. The average estimated output current is compared with the weighted reference current to generate an error signal. The error signal is fed into a PI regulator to control the PWM at pin GD for the power MOSFET. The coefficients of the PI regulator are configurable.

The PI regulator allows different modes of operation as shown in Figure 8:

- Quasi-resonant mode (QRM)  
 This mode controls the on-time and maximizes the efficiency by switching on at the 1st valley of the  $V_{AUX}$  signal. This ensures zero-current switching with a minimum of switching losses.
- Discontinuous mode (DCM)  
 This mode is used if the on-time cannot be reduced further in QRM while the output is being dimmed. The controller will extend the switching period later than the 1st valley to control the output power.
- Active-Burst mode (ABM)  
 To extend the dimming range even further, ICL8105 features an ABM which is automatically aligned with the input frequency to avoid any undesired effects like flicker or shimmer as well as to reduce any audible noise.

The controller will autonomously select the best mode of operation based on operation conditions like input voltage, input frequency and dimming input voltage which defines the output power.

Functional description

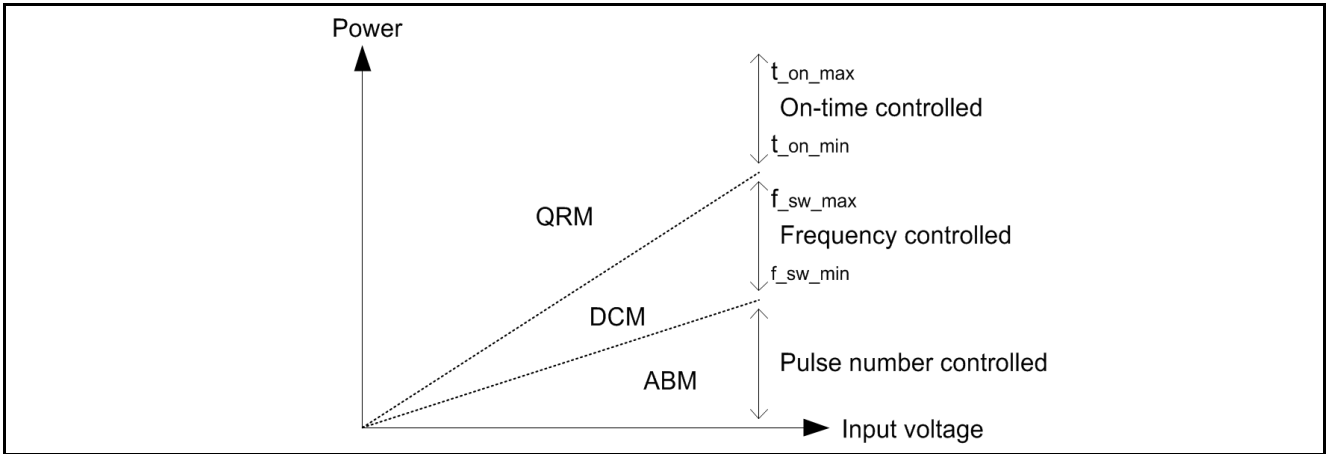


Figure 8 Overview of operation modes

2.2.3 Power factor correction (PFC)

The gate driver GD is used for driving the power MOSFET of the flyback. Constant output current regulation and a sinusoidally shaped input current are achieved by on-time control. The quasi-constant on-time  $t_{on}$  ensures high PF and low THD performance. The internal control signal  $t_{on}$  is calculated by the digital engine so that the output current is close to the target current (Chapter 2.2.2).

Optionally, an enhanced PFC (EPFC) scheme can be enabled to compensate the input current distortion caused by the EMI filter<sup>1)</sup>. In this scheme, the on-time is a function of the internal controller signal  $t_{on}$ , the input voltage  $V_{in}$ , output voltage  $V_{out}$ , output current  $I_{out}$ , phase angle and a configurable gain parameter ( $C_{EMI}$ ) optimizing the input current waveform (Chapter 2.4).

2.2.4 Dimming via pin DIM/UART

The voltage sensed at pin DIM/UART is used to determine the output current level. Figure 9 shows the relation of DIM/UART voltage to the output current target value. Levels of  $V_{DIM\_min}$  and  $V_{DIM\_max}$ <sup>2)</sup> ensure that minimum current  $I_{out\_dim\_min}$  and maximum current  $I_{out\_set}$  can always be achieved, making the application robust against dimmer and other component tolerances. The sampled voltage  $V_{DIM}$  at pin DIM/UART is digitally filtered to stabilize light output. The ICL8105 can also be configured to use a linear or a quadratic dimming curve.

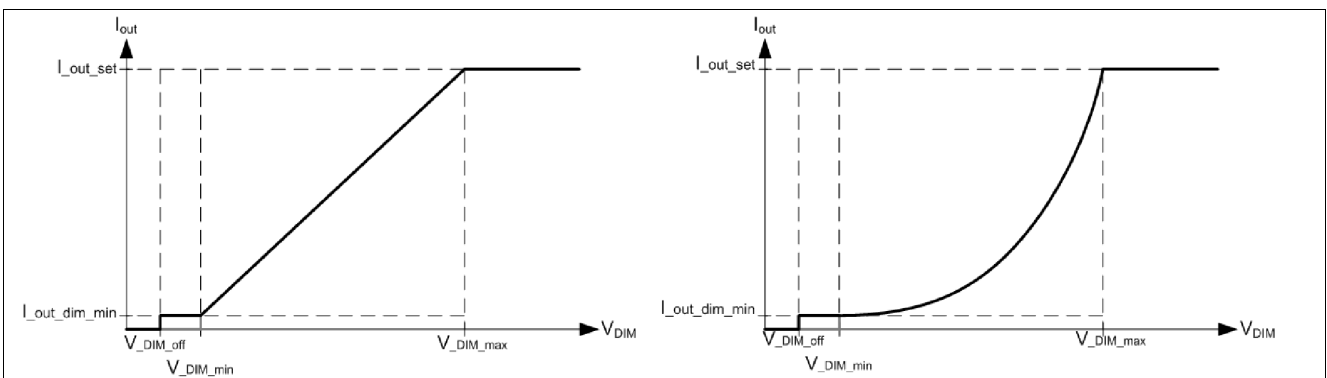


Figure 9 Dimming curves for pin DIM/UART

1) Patent pending  
 2) fixed at 1.72V

**Functional description**

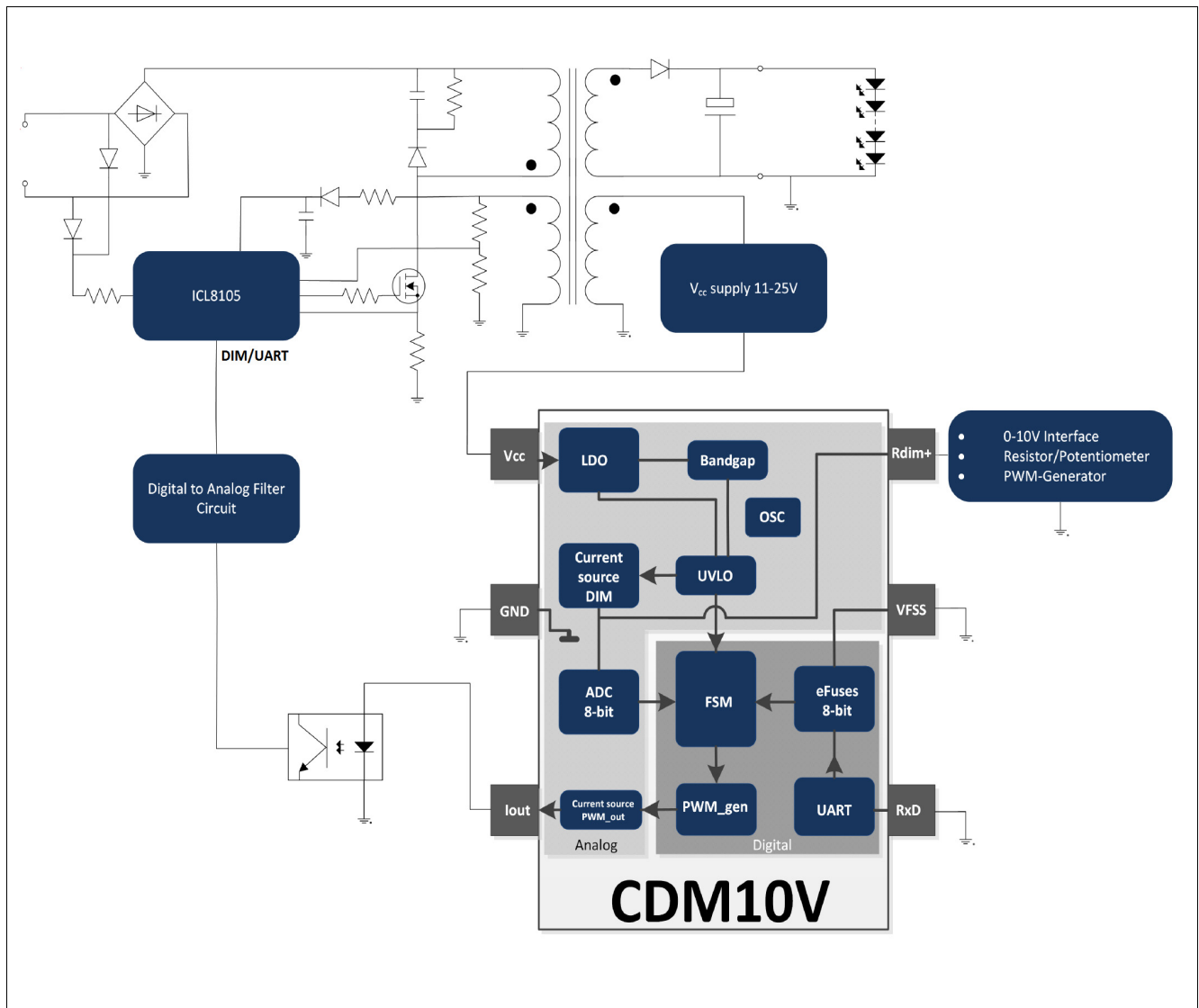
Optionally, The output current can be turned off completely when DIM/UART voltage is  $V_{DIM\_off}$  or below.

*Note: The dim-to-off feature requires an active voltage source to exit the dim-to-off state.*

In some cases where the dimming control circuitry is on the primary side and it is using PWM control, please refer ICL8105 design guide for the RC low pass filter circuit which will convert the PWM dimming signal to an analog dimming voltage for measurement on pin DIM/UART.

**2.2.5 Isolated dimming interface with CDM10V (optional)**

**Figure 10** shows an exemplary schematic of a 0-10V dimming interface for low BOM cost, using CDM10V by Infineon. CDM10V is a fully integrated 0-10V dimming interface IC which transmits secondary side analog voltage based signals from 0-10V dimmer to primary side, by driving an external opto-coupler with a 5mA current based PWM signal. The secondary auxiliary winding is necessary to supply the operating voltage of CDM10V. For more details about CDM10V, please visit Infineon website: <http://www.infineon.com/cdm10v>

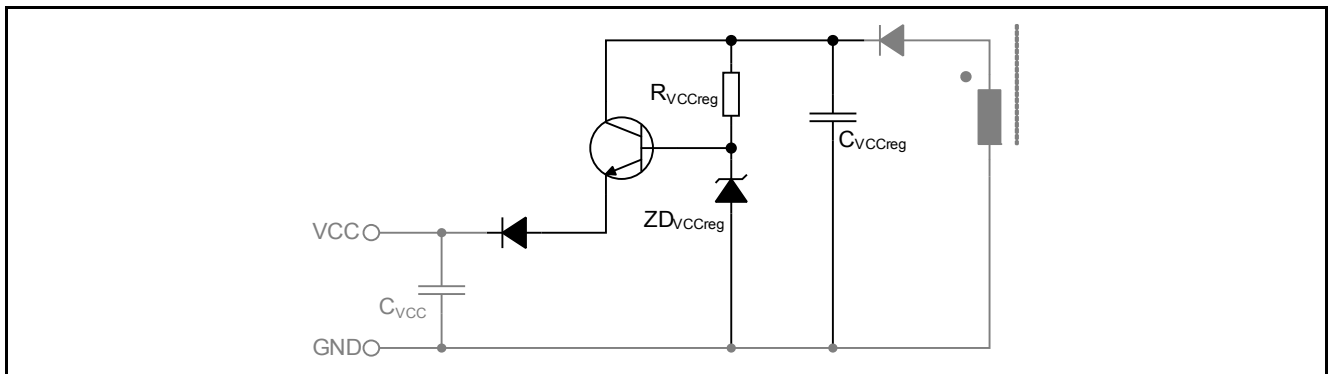


**Figure 10 Optional circuit for isolated dimming with CDM10V**

Functional description

**2.2.6 Wide output load voltage range circuit (optional)**

If wide output load voltage (more than 2 times of the minimum output load voltage) is required, a regulator for VCC is required. This regulator limits the maximum voltage at pin VCC during steady state operation. **Figure 11** shows an exemplary schematic for the optional wide output voltage range support. A wide output voltage range impacts efficiency due to the necessary voltage regulator for VCC.



**Figure 11** Optional wide output voltage range circuit

**2.2.7 Automatic output discharge circuit (optional)**

In case of a fault (e.g. Open Load) the output capacitors stay charged and may keep a high voltage. It is therefore recommended to add an automatic output discharge circuit. This circuit discharges the output capacitors if the main switch stops switching. For the circuit design, please refer the schematic in the application note of the ICL8105 40W reference design with CDM10V.

**2.2.8 VCC startup function combined with direct input monitoring**

There are two main functions supported at pin HV which needs to be connected to the input voltage via resistor and two diodes.

The integrated HV startup-cell is switched on during the VCC startup phase before the IC is activated. Current flows from pin HV to pin VCC via an internal diode, which charges the capacitor at pin VCC. Once the voltage at pin VCC exceeds the  $V_{VCCon}$  threshold, the IC enables the active operating phase and switches off the HV startup-cell.

Furthermore, a direct input monitoring is supported that is controlled by an internal timer. The timer switches on the HV startup cell for a very short time after a defined period. During this short on-time the current is sensed at pin HV by a comparator to synchronize to frequency and phase of the input voltage.

**2.2.9 Configurable soft start**

After startup, the IC initiates a soft-start. During soft-start, the switching stress for the power MOSFET, diode and transformer is minimized. The cycle-by-cycle current limit is increased in steps with a configurable time  $t_{ss}$  for each step. The number of soft start steps is defined by parameter  $n_{ss}^1$ . After the final CS limit level has been reached, the output will be charged up with maximum on-time and maximum CS limitation level to the minimum output voltage that ensures self-supply,  $V_{out\_start}$ . After the minimum output voltage has been reached, the current control loop (**Chapter 2.2.2**) takes over and output undervoltage protection is activated (if enabled by configuration).

1) fixed at 3

Functional description

**2.2.10 Configurable gate voltage rising slope at pin GD (Lower EMI)**

The gate driver output signal can be configured with respect to the rising slope for switching on the power MOSFET. This feature can save BOM components (1 diode & 1 resistor) which are conventionally added to achieve the same purpose for EMI improvement. The maximum gate drive current  $I_{GD\_pk}$  for the gate driver slope can be set between 30 mA and 118 mA (Chapter 2.4). Figure 12 shows the gate driver output signal.

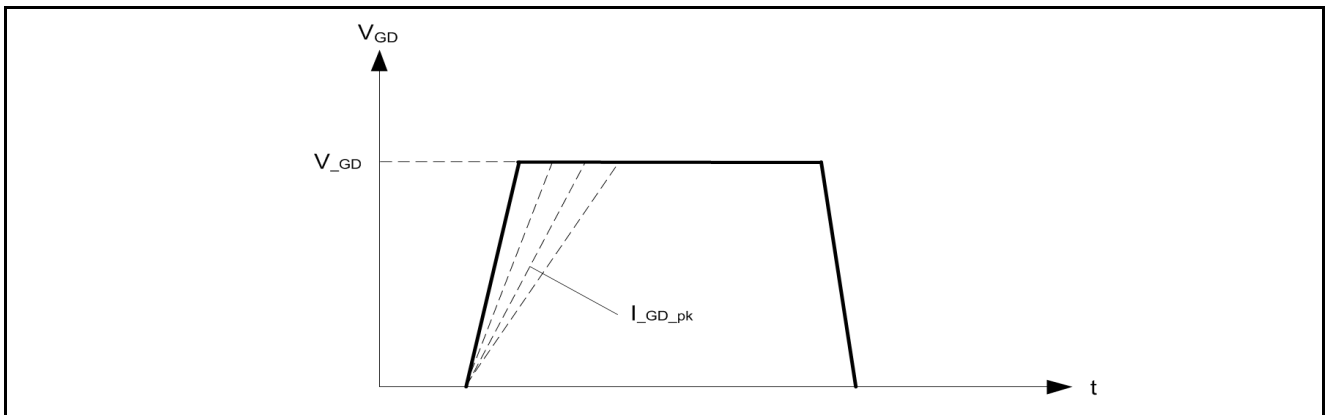


Figure 12 Configurable gate voltage rising slope for lower EMI

**Functional description**

**2.3 Protection features**

**Table 4** gives an overview about the available protection features and corresponding default actions in case a protection feature is triggered. Two protection reactions (auto restart mode and latch mode) are implemented.

**Auto restart mode**

Once the auto restart mode is activated, the IC stops the power MOSFET switching at pin GD and reduces the current consumption to a minimum. After the configurable auto restart time  $t_{\text{auto\_restart}}$  the IC initiates a new start-up<sup>1)</sup>. During this auto restart the HV startup-cell is switched on and off in order to keep the VCC between  $V_{\text{UVLO}}$  and  $V_{\text{OVLO}}$  thresholds<sup>2)</sup>. The auto restart cycle starts first with charging the VCC capacitor by means of switching on the HV startup cell until the  $V_{\text{VCCon}}$  threshold is exceeded. A regular startup procedure with soft start is initiated afterwards.

**Latch mode**

When latch mode is activated, the power MOSFET switching at pin GD is immediately stopped. The HV startup-cell is switched on and off in order to keep the VCC between  $V_{\text{UVLO}}$  and  $V_{\text{OVLO}}$  thresholds. The device stays in this state until input voltage is completely removed and the VCC voltage drops below the  $V_{\text{UVLO}}$  threshold. The IC can then be re-started by applying input voltage.

**Table 4 Protection Features**

| Protection Feature                                   | Active Period (if enabled)            | Reaction                   | Description                   |
|--|---------------------------------------|----------------------------|-------------------------------|
| Undervoltage lockout for VCC                         | Always on                             | Hardware restart           | <a href="#">Chapter 2.3.1</a> |
| Oversvoltage protection for VCC                      | Always on                             | Latch mode <sup>1)</sup>   | <a href="#">Chapter 2.3.2</a> |
| Oversvoltage protection for $V_{\text{out}}$         | Always on                             | Auto restart <sup>1)</sup> | <a href="#">Chapter 2.3.3</a> |
| Undervoltage protection for $V_{\text{out}}$         | Activated after startup <sup>2)</sup> | Auto restart               | <a href="#">Chapter 2.3.3</a> |
| Startup Undervoltage protection for $V_{\text{out}}$ | During startup                        | Auto restart               | <a href="#">Chapter 2.3.3</a> |
| Oversvoltage protection for $V_{\text{in}}$          | Always on <sup>2)</sup>               | Latch mode                 | <a href="#">Chapter 2.3.4</a> |
| Undervoltage protection for $V_{\text{in}}$          | Always on <sup>2)</sup>               | Auto restart               | <a href="#">Chapter 2.3.4</a> |
| Input overcurrent detection level 1                  | Always on                             | Current limiting           | <a href="#">Chapter 2.3.5</a> |
| Input overcurrent protection level 2                 | Always on                             | Latch mode                 | <a href="#">Chapter 2.3.6</a> |
| Output current protection (average)                  | Activated after startup <sup>2)</sup> | Auto restart               | <a href="#">Chapter 2.3.7</a> |
| Output current protection (peak)                     | Activated after startup <sup>2)</sup> | Auto restart               | <a href="#">Chapter 2.3.7</a> |
| Overtemperature protection                           | Always on                             | Latch mode                 | <a href="#">Chapter 2.3.8</a> |
| Firmware protections (1st Watchdog & RAM Parity)     | Always on                             | Auto restart               | <a href="#">Chapter 2.3.9</a> |

1) Protection which its reaction can be configured to either auto restart mode or latch mode.

2) Protection which can be disabled or enabled by configuration.

1) After  $t_{\text{auto\_restart}}$ , the VCC will be charged to  $V_{\text{VCCon}}$  again(see [Chapter 2.2.8](#)). Therefore, the effective auto-restart time is longer than  $t_{\text{auto\_restart}}$

2) This feature can be disabled for applications with externally supplied VCC.



Functional description

**2.3.1 Undervoltage lockout for VCC**

An undervoltage lockout unit (UVLO) is implemented which ensures a defined enabling and disabling of the IC operation depending on the supply voltage at pin VCC. The UVLO contains a hysteresis with the voltage thresholds  $V_{VCCon}$  for enabling the IC and  $V_{UVOFF}$  for disabling the IC. Once the mains input voltage is applied, current flows through an external resistor into pin HV via the integrated diode to pin VCC. The IC is enabled once VCC exceeds the threshold  $V_{VCCon}$  and enters normal operation if no fault condition is detected. In this phase VCC will drop until the self supply via the auxiliary winding takes over the supply at pin VCC. For proper startup, the self supply via auxiliary winding must be in place before the timeout of  $t_{start\_max}$  occurs (See [Chapter 2.3.3](#)) or before VCC falls below  $V_{UVOFF}$  threshold.

**2.3.2 Overvoltage protection for VCC**

Overvoltage detection at pin VCC is implemented via a threshold of  $V_{VCC\_max}$ .

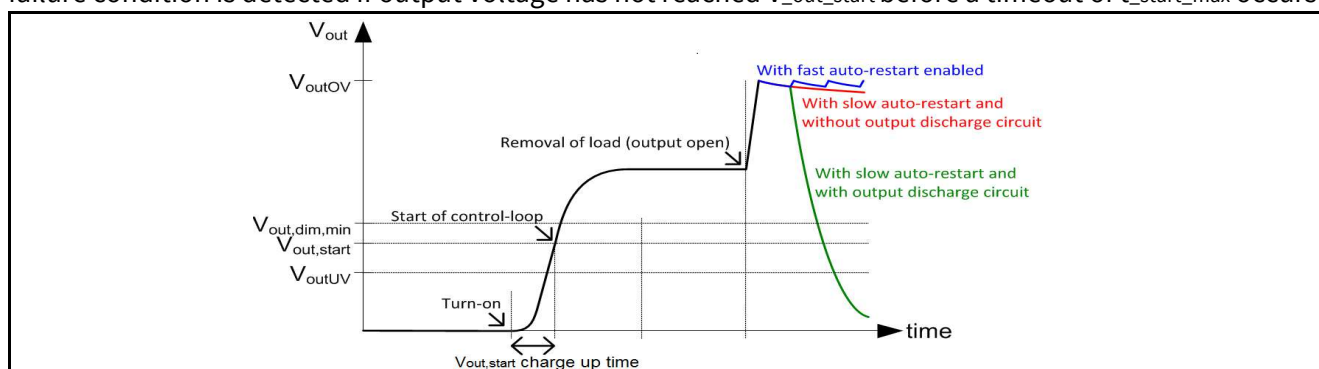
**2.3.3 Over / undervoltage protection for output voltage**

Overvoltage (e.g. Open Load) or undervoltage (e.g. Output short) detection of the output voltage  $V_{out}$  is provided by the measurement and calculation as described in [Chapter 2.2.1.3](#). The overvoltage detection thresholds  $V_{outOV}$  is configurable while the undervoltage detection threshold  $V_{outUV}$  is fixed at 50% of the configurable  $V_{out\_dim\_min}$  threshold. Output undervoltage protection is disabled during startup. For output overvoltage protection in auto-restart reaction, either slow or fast auto-restart can be selected. The startup threshold  $V_{out\_start}$  has to be configured below the fully dimmed minimum output load voltage,  $V_{out\_dim\_min}$ .

*Note: Please note that there are possibilities where critical protection like output over-voltage not working properly (example: wrong parameter configurations loaded). Thus, please consider adding zener diode or any voltage suppressor device/circuit on output for reinforced safety purpose.*

*Note: It is mandatory to have output discharge resistor/circuit which discharges the output capacitor after triggering open load protection at  $V_{outOV}$ . Latch reaction is recommended for open load protection as it can shut down the unit to prevent output overcharged if the discharge resistor ohmic value is too high.*

In case of output short/under-voltage, the auxiliary winding cannot provide power to VCC during startup. Such failure condition is detected if output voltage has not reached  $V_{out\_start}$  before a timeout of  $t_{start\_max}$  occurs



**Figure 13 Voltage threshold for output over / undervoltage protection**

**2.3.4 Over / undervoltage protection for input voltage**

An over / undervoltage detection of the input voltage  $V_{in}$  is provided by the measurement and calculation as described in [Chapter 2.2.1.2](#). Peak values of  $V_{in}$  are compared to the configurable internal input over / undervoltage protection thresholds  $V_{inOV}$  and  $V_{inUV}$  ([Chapter 2.4](#)).

Functional description

Figure 14 shows an exemplary setting of both over- and undervoltage thresholds together with configurable startup thresholds  $V_{in\_start\_min}$  and  $V_{in\_start\_max}$  to create hysteresis for flicker-free operation at auto-restart.

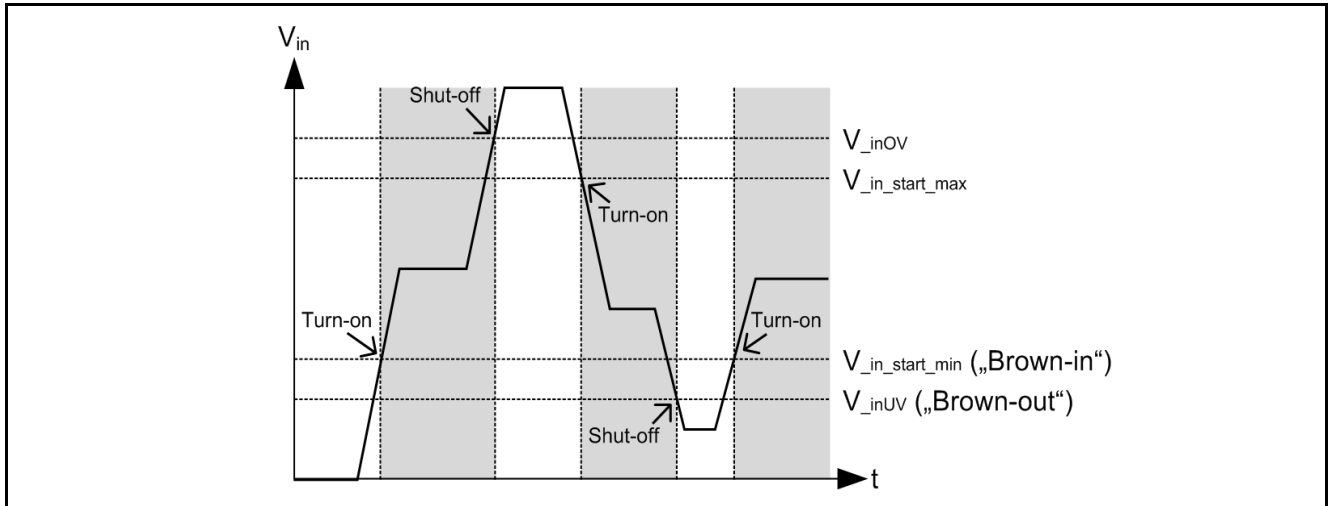


Figure 14 Voltage threshold for input over / undervoltage protection

### 2.3.5 Input overcurrent detection level 1 (OCP1)

The input overcurrent protection level 1 is performed by means of the cycle-by-cycle peak current limitation to  $V_{ocp1}$ . A leading edge blanking,  $t_{CSLEB}$  prevents the IC from falsely switching off the power MOSFET due to a leading edge spike.

### 2.3.6 Input overcurrent protection level 2 (OCP2)

The input overcurrent protection level 2 is meant for covering fault conditions like a short in the transformer primary winding. In this case overcurrent protection level 1 will not limit properly the peak current due to the very steep slope of the peak current. Once the threshold  $V_{ocp2}$  is exceeded for longer than  $t_{CSOCP2}$ , the protection is triggered.

### 2.3.7 Output overcurrent protections

The ICL8105 includes protections against exceeding an average and peak current limit. The average output current is calculated over one half cycle of the input frequency to remove the output current ripple. With auto-restart reaction, either slow auto-restart or fast auto-restart can be selected.

### 2.3.8 Overtemperature protection

ICL8105 offers a conventional as well as an adaptive overtemperature protection scheme using an internal temperature sensor.

*Note: Please note that the internal temperature sensor may not be able to sense and protect the temperature of external components (e.g. power MOSFET, VCC regulator) without sufficient thermal coupling.*

#### Conventional overtemperature protection

The overtemperature protection initiates a thermal shutdown once the internal temperature detection level  $T_{critical}$  is reached. With latch mode protection, IC will turn off and only restart after recycling of input power. At startup, junction temperature has to be below  $T_{start}$ .

Functional description

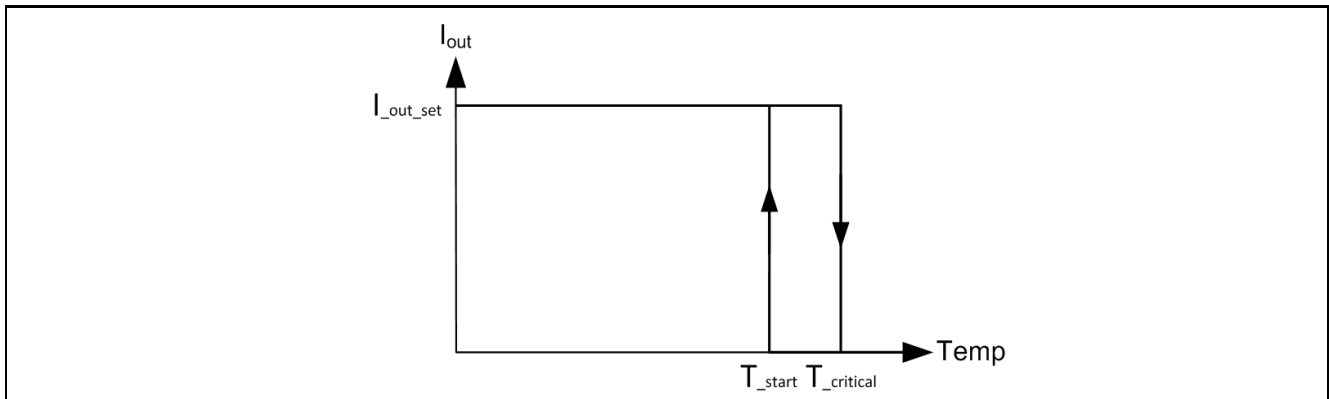


Figure 15 Conventional temperature protection

Adaptive temperature protection

To protect load and driver against overtemperature, ICL8105 features a reduction of output current below maximum current  $I_{out\_set}$ . As long as temperature  $T_{hot}$  is exceeded, the current is gradually reduced as shown in Figure 16. If a reduction down to a minimum current  $I_{out\_red}$  is not able to compensate the increase of temperature, IC will turn off at temperature  $T_{critical}$ .

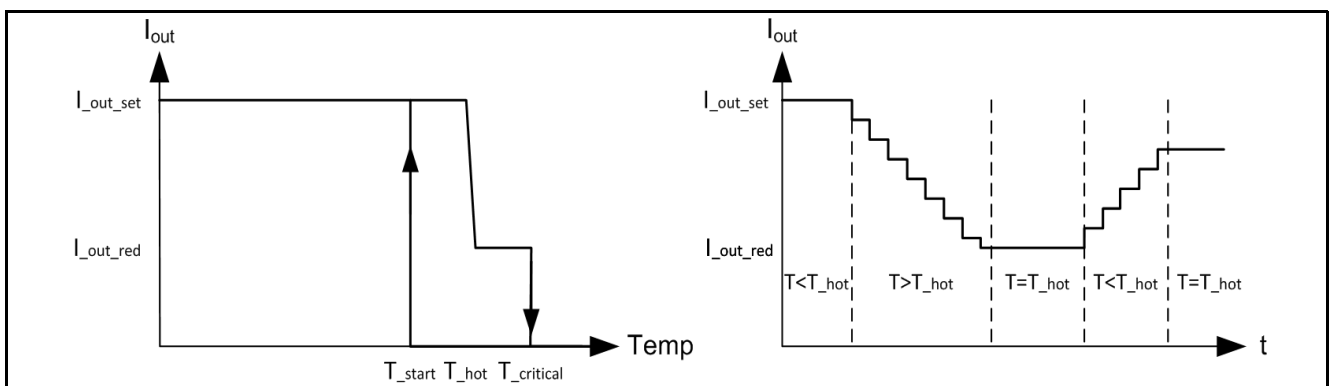


Figure 16 Adaptive temperature protection

2.3.9 Firmware protections

ICL8105 includes several protections to ensure the integrity and flow of the firmware:

- A hardware watchdog triggers a protection in case the firmware does not service the watchdog within a defined time period.
- A RAM parity check triggers a protection in case a bit in the memory flips.
- A cyclic redundancy check (CRC) at each startup verifies the integrity of firmware and parameters.
- A first firmware watchdog triggers a protection if the ADC hardware cannot provide all necessary information within a defined time period. This may occur if timing requirements for the ADC are exceeded.
- A second firmware watchdog triggers a protection if the execution of protection checks and the control loop are not matching a defined time period. This may occur if timing requirements are exceeded (e.g. operation beyond frequency limits).

**Functional description**

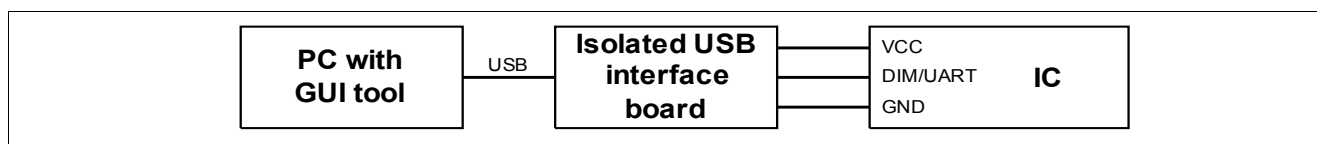
**2.4 Configuration and support**

The configuration of ICL8105 is supported by the GUI tool .dp vision provided by Infineon. This chapter describes the configuration procedure via the UART interface. Furthermore, it contains an overview about the parameters and functions that can be configured.

**2.4.1 Configuration procedure and design-in support**

**Figure 17** shows the setup for the configuration of ICL8105. The Infineon graphic user interface (GUI) .dpVision connects to ICL8105 via the isolated USB interface board called .dp Interface Gen2. The .dp interface Gen 2 provides power via VCC to ICL8105 and connects via UART interface at pin DIM/UART. The common UART interface enables communication with the IC even without the interactive GUI tool. This allows easy configuration during mass production.

When VCC exceeds the  $V_{VCCon}$  threshold, ICL8105 will sense pin DIM/UART for a UART connection. If power is provided by VCC and no input voltage is applied at startup, ICL8105 will enter configuration mode. Also, ICL8105 will enter configuration mode if no parameters have been programmed so far, regardless of input voltage being applied or not.



**Figure 17 Setup for configuration of the IC**

For project development, a graphic user interface called .dp Vision guides the designer through the configuration of parameters. Further information on .dp Vision can be found in the .dp Vision User Manual provided by Infineon.

For production and end user configuration, a simpler graphic user interface called XDP™ GUI is also available. The configurable parameters and configuration range of each parameter in the XDP™ GUI can be customized using the XDP™ GUI Builder software provided by Infineon. Please refer the user manual of this GUI Builder for more details.

The dimensioning of the application design (e.g. transformer design, BOM selection, IC parameterization) can be done easily with an excel tool named ICL8105 system simulation & design creation tool. An ICL8105 40W reference design with CDM10V is available from Infineon to demonstrate the features and performance. The ICL8105 design guide presents the dimensioning process while the reference design application note presents the board performance, fine tuning guide, debugging guide and frequently asked questions.

**2.4.2 Overview configurable parameters and functions**

The ICL8105 provides a generic firmware version that includes all configurable parameters set to zero. The parameter values need to be specified by the user according to the target application. **Table 5** lists the configurable parameters. **Table 6** lists the non configurable parameters which the values are constant or adapted internally according to the configurable parameters settings.

**Table 5 List of configurable parameters**

| Description                             | Parameter            | Example | Configuration Range |
|---|----------------------|---------|---------------------|
| <b>Hardware configuration</b>           |                      |         |                     |
| I <sub>out</sub> set point (non-dimmed) | I <sub>out_set</sub> | 880 mA  | Calculated by GUI   |

**Functional description**

**Table 5 List of configurable parameters (cont'd)**

| <b>Description</b>                      | <b>Parameter</b> | <b>Example</b> | <b>Configuration Range</b>                    |
|---|------------------|----------------|---|
| Transformer primary winding turns       | N_p              | 58             | > 0   |
| Transformer secondary winding turns     | N_s              | 15             | > 0   |
| Transformer auxiliary winding turns     | N_a              | 15             | > 0   |
| Transformer nominal primary Inductance  | L_p              | 0.544 mH       | Calculated by GUI                             |
| Current sense resistor                  | R_CS             | 0.22 ohm       | Calculated by GUI                             |
| Pin CS OCP1 limitation threshold        | V_OCP1           | 0.49 V         | Calculated by GUI                             |
| Pin ZCD series resistor                 | R_ZCD_1          | 56.2 kohm      | Calculated by GUI                             |
| Pin ZCD shunt resistor                  | R_ZCD_2          | 2.00 kohm      | Calculated by GUI                             |
| Vcc Voltage Supply Type                 | VCC_SUPPLY       | Wide           | [External, Narrow, Narrow_24.9V, Wide]        |
| Vcc capacitor total capacitance         | C_VCC            | 15.0 uF        | Calculated by GUI                             |
| Output capacitor maximum Voltage Rating | V_out_cap_rating | 63 V           | ≥ 0   |
| Pin HV series resistor                  | R_HV             | 66 kohm        | Calculated by GUI                             |
| Gate driver peak source current         | I_GD_pk          | 49 mA          | 30 mA to 118 mA (with few mA change per step) |

**Protections**

|  |                     |                                    |                                   |
|--|---------------------|------------------------------------|-----------------------------------|
| Auto restart time                      | t_auto_restart      | 1 s                                | 0.1 s to 25.5 s <sup>1)</sup>     |
| Fast auto restart time                 | t_auto_restart_fast | 0.4 s                              | 0.1 s to 25.5 s <sup>1)</sup>     |
| Output OVP / Open Reaction             | Reaction_OVP_Vout   | Auto restart                       | [Auto restart, Latch mode]        |
| Auto restart speed for output OVP      | Speed_OVP_Vout      | Slow                               | [Slow, Fast]                      |
| Output OVP threshold                   | V_outOV             | 48.4 V                             | V_out_dim_min to V_out_cap_rating |
| Enable output UVP / Short Protection   | EN_UVP_Vout         | Enabled                            | [Enabled, Disabled]               |
| Timeout for short detection at startup | t_start_max         | 10.0 ms                            | Calculated by GUI                 |
| Enable Maximum Average output OCP      | EN_Iout_max_avg     | Enabled                            | [Enabled, Disabled]               |
| Enable Maximum Peak output OCP         | EN_Iout_max_peak    | Enabled                            | [Enabled, Disabled]               |
| Maximum peak Output OCP threshold      | I_out_max_peak      | 1980 mA                            | Calculated by GUI                 |
| Auto restart speed for output OCP      | Speed_OCP_Iout      | Slow                               | [Slow, Fast]                      |
| Enable Input OVP                       | EN_OVP_In           | Enabled                            | [Enabled, Disabled]               |
| Enable Input UVP                       | EN_UVP_In           | Enabled                            | [Enabled, Disabled]               |
| Input OVP threshold                    | V_inOV              | 329 V <sub>rms</sub> <sup>2)</sup> | Calculated by GUI                 |
| Maximum startup input voltage          | V_in_start_max      | 329 V <sub>rms</sub> <sup>2)</sup> | V_in_start_min to V_inOV          |
| Minimum startup input voltage          | V_in_start_min      | 72 V <sub>rms</sub> <sup>2)</sup>  | V_inUV to V_in_start_max          |
| Input UVP threshold                    | V_inUV              | 62 V <sub>rms</sub> <sup>2)</sup>  | Calculated by GUI                 |
| Vcc OVP Reaction                       | Reaction_VCCP       | Latch mode                         | [Auto restart, Latch mode]        |
| Enable Debug mode                      | Debug_mode          | Disabled                           | [Enabled, Disabled]               |

**Temperature guard**

**Functional description**

**Table 5 List of configurable parameters (cont'd)**

| <b>Description</b>   | <b>Parameter</b> | <b>Example</b> | <b>Configuration Range</b>           |
|--|------------------|----------------|--------------------------------------|
| Overtemperature detection threshold                          | T_critical       | 119 °C         | 110°C to (T <sub>J(max)</sub> - 6°C) |
| Enable adaptive temperature protection                       | EN_ITP           | Enabled        | [Enabled, Disabled]                  |
| Temperature to start derating of I <sub>out</sub>            | T_hot            | 110 °C         | 0 °C to T_critical                   |
| Minimum I <sub>out</sub> for adaptive temperature protection | I_out_red        | 220 mA         | 0 mA to I_out_set                    |
| Time step for each I <sub>out</sub> derating                 | t_step           | 10 s           | 2 s to 20 s                          |

**Startup & shutdown**

|   |                   |        |                          |
|---|-------------------|--------|--------------------------|
| Soft start timestep                                     | t_ss              | 0.5 ms | Calculated by GUI        |
| Minimum V <sub>out</sub> when fully dimmed              | V_out_dim_min     | 11.9 V | V_out_start to V_outOV   |
| V <sub>out</sub> to start constant current control loop | V_out_start       | 9.5 V  | V_outUV to V_out_dim_min |
| Initial mode of operation                               | control_loop_init | DCM    | [ABM, DCM, QRM]          |
| Initial DCM frequency at startup                        | f_DCM_init        | 12 kHz | f_sw_min_DCM to f_sw_max |
| Initial number of ABM pulses at startup                 | N_ABM_init        | 100    | Calculated by GUI        |

**Control loop**

|   |           |       |              |
|---|-----------|-------|--------------|
| QRM PI regulator proportional coefficient | PI_KP_QRM | 550   | 10 to 3000   |
| QRM PI regulator integral coefficient     | PI_KI_QRM | 8     | 1 to 1000    |
| DCM PI regulator proportional coefficient | PI_KP_DCM | 17000 | 100 to 30000 |
| DCM PI regulator integral coefficient     | PI_KI_DCM | 200   | 10 to 10000  |
| ABM PI regulator proportional coefficient | PI_KP_ABM | 64    | 1 to 600     |
| ABM PI regulator proportional coefficient | PI_KI_ABM | 32    | 1 to 200     |

**Dimming**

|   |               |           |                        |
|---|---------------|-----------|------------------------|
| Enable Dimming                                    | EN_DIM        | Enabled   | [Enabled, Disabled]    |
| Pin DIM/UART voltage for minimum I <sub>out</sub> | V_DIM_min     | 0.2 V     | V_DIM_off to V_DIM_max |
| Minimum I <sub>out</sub> when fully dimmed        | I_out_dim_min | 88 mA     | Calculated by GUI      |
| Dimming curve shape                               | C_DIM         | Quadratic | [Linear, Quadratic]    |
| Enable dim-to-off                                 | EN_DIM_TO_OFF | Disabled  | [Enabled, Disabled]    |
| Pin DIM/UART voltage for dim-to-off               | V_DIM_off     | 0.18 V    | 0.1 V to V_DIM_min     |
| Enable Square Wave Output for pin SQW             | EN_SQW        | Disabled  | [Enabled, Disabled]    |

**Multimode**

|                                    |              |           |                     |
|------------------------------------|--------------|-----------|---------------------|
| Maximum switching frequency        | f_sw_max     | 180.8 kHz | Calculated by GUI   |
| Maximum on-time                    | t_on_max     | 11.3 us   | Calculated by GUI   |
| Minimum on-time                    | t_on_min     | 1.1us     | 1 us to t_on_max    |
| Minimum demagnetization time       | t_min_demag  | 3.0 us    | 2 us to 10 us       |
| Minimum switching frequency in DCM | f_sw_min_DCM | 12 kHz    | 3 kHz to 20kHz      |
| Enable Active Burst Mode           | EN_ABM       | Disabled  | [Enabled, Disabled] |

**Enhanced PFC**

**Functional description**

**Table 5 List of configurable parameters (cont'd)**

| Description                             | Parameter      | Example   | Configuration Range |
|---|----------------|-----------|---------------------|
| Enhanced PFC compensation gain          | C_EMI          | 0.1000 uF | ≥ 0                 |
| <b>Fine tuning</b>                      |                |           |                     |
| ZCD propagation delay compensation      | t_ZCDPD        | 410 ns    | 0 ns to 1000 ns     |
| CS Propagation delay compensation       | t_PDC          | 200 ns    | 0 ns to 1000 ns     |
| Transformer coupling                    | T_coupling     | 1.020     | 0.000 to 2.000      |
| Input voltage drop compensation         | R_in           | 11.9 ohm  | ≥ 0                 |
| Switching period modulation attenuation | N_DCM_mod_gain | 8         | [0, 8, 16, 32]      |
| Temperature compensation for V_DIM      | a_DIM          | 0mV/K     | -8 mV/K to 8 mV/K   |

- 1) The auto-restart time has to be chosen sufficiently large enough to avoid a stepping up of the output voltage which would exceed the output overvoltage level.
- 2) The input voltage levels refer to AC RMS voltage. If a programmed ICL8105 is operated with both AC or DC, the threshold for DC input voltage is 1.41 times the threshold for AC RMS input voltage.

**Table 6 List of non-configurable parameters**

| Description  | Parameter              | Value                   | Notes  |
|--|------------------------|-------------------------|--|
| <b>Hardware configuration</b>                                    |                        |                         |  |
| Transformer primary leakage inductance                           | L_p_lk                 | L_p * 1% uH             |  |
| Output diode voltage drop  | V_out_diode_drop       | 0.7 V                   |  |
| Gate driver high voltage   | V_GD                   | 10.5 V                  |  |
| <b>Protections</b>   |                        |                         |  |
| Output UVP / Short Reaction                                      | Reaction_UVP_Vout      | Auto restart            |  |
| Output UVP threshold (at steady state)                           | V_outUV                | V_out_dim_min<br>*50% V |  |
| Steady state Output UVP blanking time                            | t_Vout_blank           | 1 ms                    |  |
| Maximum Average output OCP Reaction                              | Reaction_lout_max_avg  | Auto restart            |  |
| Maximum Average Output OCP threshold                             | I_out_max_avg          | I_out_set *<br>150% mA  |  |
| Maximum Peak output OCP Reaction                                 | Reaction_lout_max_peak | Auto restart            |  |
| Input OVP Reaction   | Reaction_OVP_Vin       | Latch mode              |  |
| Input UVP Reaction   | Reaction_UVP_Vin       | Auto restart            |  |
| Input OCP2 / Short Winding Reaction                              | Reaction_OCP2          | Latch mode              |  |
| Vcc OVP Threshold  | V_VCC_max              | 24 V or 24.9V           | if VCC_SUPPLY = Narrow_24.9V,<br>24.9V. Otherwise, 24V |
| Hardware reaction for Firmware Protection (Watchdog, RAM parity) | Reaction_HW            | Auto restart            |  |
| <b>Temperature guard</b>   |                        |                         |  |
| Overtemperature Reaction   | Reaction_TP            | Latch mode              |  |

**Functional description**

**Table 6 List of non-configurable parameters (cont'd)**

| <b>Description</b>                                   | <b>Parameter</b>      | <b>Value</b>                  | <b>Notes</b>   |
|--|-----------------------|-------------------------------|--|
| Maximum startup temperature                          | T_start               | T_hot -2°C or T_critical -2°C | if EN_ITP = enabled, T_hot -2°C, otherwise T_critical -2°C |
| I <sub>out</sub> reduction in each derating step     | I <sub>out_step</sub> | I <sub>out_set</sub> /80      |  |
| <b>Startup &amp; shutdown</b>                        |                       |                               |  |
| Number of soft start steps                           | n <sub>ss</sub>       | 3                             |  |
| <b>Dimming</b>                                       |                       |                               |  |
| Pin DIM/UART voltage for maximum I <sub>out</sub>    | V_DIM_max             | 1.72 V                        |  |
| Square-wave frequency for SQW pin                    | f_SQW                 | 160 kHz                       |  |
| Square-wave voltage for pin SQW                      | V_SQW                 | 7.5 V                         |  |
| <b>Multimode</b>                                     |                       |                               |  |
| Minimum switching frequency in QRM                   | f_sw_min_QRM          | 20 kHz                        |  |
| Enable DCM   | EN_DCM                | Enabled                       |  |
| <b>Fine tuning</b>                                   |                       |                               |  |
| Spike blanking time for OCP2 trigger                 | t_CSOP2               | 240 ns                        |  |
| Leading edge blanking time                           | t_CSLEB               | 480 ns                        |  |
| ZCD ringing suppression time                         | t_ZCDring             | 1200 ns                       |  |
| Blanking time for CCM protection                     | t_CCM                 | 10 ms                         |  |
| Number of digital filter stages for V <sub>DIM</sub> | N_DIM_Filter          | 6                             |  |



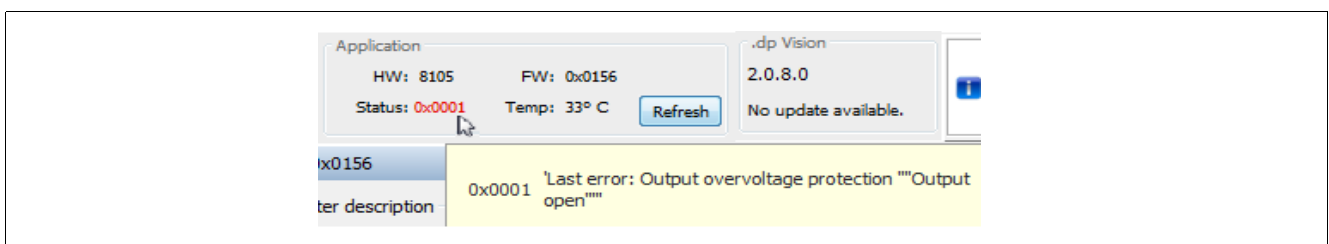
Functional description

2.4.3 Debug mode support

If an unexpected system protection was triggered during testing, user can set parameter Debug\_mode to “Enabled”, which allows the firmware status code readout from the IC to debug which protection was triggered.

For example in **Figure 18**, the firmware status code readout in the GUI shows a number of 0x0001 (in red colour), which the description shows that the output over-voltage protection has been triggered. The description of the status code will be shown automatically when the mouse pointer is hovered around the status code.

*Note: if there is no protection being triggered, the firmware status code should be 0x0000 (in black colour)*



**Figure 18** Firmware status code readout for debugging

Please kindly refer the application note for details on the necessary setup & procedures to read out the firmware status code in debug mode.

Electrical Characteristics

### 3 Electrical Characteristics

All signals are measured with respect to ground (pin 8). The voltage levels are valid if other ratings are not violated.

#### 3.1 Package Characteristics

**Table 7** Package Characteristics

| Parameter                                   | Symbol     | Limit Values |     | Unit | Remarks                |
|---|------------|--------------|-----|------|------------------------|
|   |            | min          | max |      |                        |
| Thermal resistance from junction to ambient | $R_{thJA}$ | —            | 178 | K/W  | PG-DSO-8 <sup>1)</sup> |

1) JEDEC 1s0p at  $P_v = 140$  mW

#### 3.2 Absolute Maximum Ratings

Absolute maximum ratings (**Table 8**) are defined as ratings which when being exceeded may lead to destruction of the integrated circuit. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. These values are not tested during production test.

**Table 8** Absolute Maximum Ratings

| Parameter  | Symbol         | Limit Values |                   | Unit | Remarks  |
|--|----------------|--------------|-------------------|------|--|
|  |                | min          | max               |      |  |
| Voltage externally supplied at pin VCC               | $V_{CC}$       | -0.5         | 26                | V    |  |
| Voltage at pin GD                                    | $V_{GD}$       | -0.5         | $V_{CC} + 0.3$    | V    |  |
| Voltage at pin SQW                                   | $V_{SQW}$      | -0.5         | $V_{CC} + 0.3$    | V    |  |
| Ambient temperature                                  | $T_A$          | -40          | 85                | °C   | $136.4\text{kHz} < f_{sw\_max} \leq 180.8\text{kHz}$ |
|  |                | -40          | 105               | °C   | $f_{sw\_max} \leq 136.4\text{kHz}$                   |
| Junction temperature                                 | $T_J$          | -40          | 125               | °C   | $136.4\text{kHz} < f_{sw\_max} \leq 180.8\text{kHz}$ |
|  |                | -40          | 150 <sup>1)</sup> | °C   | $f_{sw\_max} \leq 136.4\text{kHz}$                   |
| Storage temperature                                  | $T_S$          | -55          | 150               | °C   |  |
| Soldering temperature                                | $T_{Sold}$     | —            | 260               | °C   | Wave soldering <sup>2)</sup>                         |
| ESD capability HBM                                   | $V_{HBM}$      | —            | 2000              | V    | Excluding pin HV <sup>3)</sup>                       |
| ESD capability HBM                                   | $V_{HBM}$      | —            | 1500              | V    | Pin HV <sup>3)</sup>                                 |
| Voltage at pin ZCD                                   | $V_{ZCD}$      | -0.5         | 3.6               | V    |  |
| Voltage at pin CS                                    | $V_{CS}$       | -0.5         | 3.6               | V    |  |
| Voltage at pin DIM/UART                              | $V_{DIM/UART}$ | -0.5         | 3.6               | V    |  |
| Maximum transient input clamping for pins ZCD and CS | $-I_{CLN\_TR}$ | —            | 10                | mA   | <sup>4)</sup>  |