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ICL8201

AC/DC Buck Controller with PFC for LED
Lamps

Data Sheet
Revision V2.0 2015-05-25

Power Management & Multimarket

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Revision History

Major changes since previous revision

Date	Version	Changed By	Change Description
2015-05-25	2.0		First Release


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ICL8201 – Single-Stage Floating Buck Controller IC with Power Factor Correction for LED Lamps

Product Highlights

- Low external component count for smallest form factors and easy design-in
- IC concept allows standard single chokes without auxiliary winding
- True universal AC line input voltage or DC supply
- Compensation of sudden line input voltage changes
- Supports wide output voltage
- Capable of providing an average LED output current up to 800 mA at 50% Duty Cycle
- Typical $\pm 5\%$ output current accuracy over line, load and temperature variation
- Supports PF > 90% / iATHD < 20% over a wide line input voltage range
- System efficiency up to 90%
- Thermally-optimized package PG-SOT23-6-1 for small form factor designs
- Smooth start-up with minimized current overshoot
- Advanced cascode topology eliminates the requirement of high voltage startup cell
- External power switch supports fast time-to-light and high operating temperature
- Operation specified for junction temperature up to $T_j = 150\text{ }^\circ\text{C}$

IC Features

- Critical Conduction operation mode without detection winding
- Constant t_{ON} operation with variable frequency 40 kHz to 150 kHz
- Integrated low-side MOSFET for rated peak current up to 2.65A
- Digital soft-start
- Fully integrated protection:
 - Short load
 - Support open load
 - Short winding at buck inductor
 - Over-current protection (power limitation)
 - Intelligent Over-Temperature Protection @ $T_{jmax} = 150\text{ }^\circ\text{C}$
 - V_{CC} Under-Voltage Lock-Out
 - Short-to-GND of CS pin and Con pin
 - Floating CS pin and Con pin
 - Phase cut dimmer-safe

Target Applications

- A-lamps
- GU10 lamps
- PAR lamps
- Candelabra lamps
- Down lights
- T8 lamps

1 Block Diagram

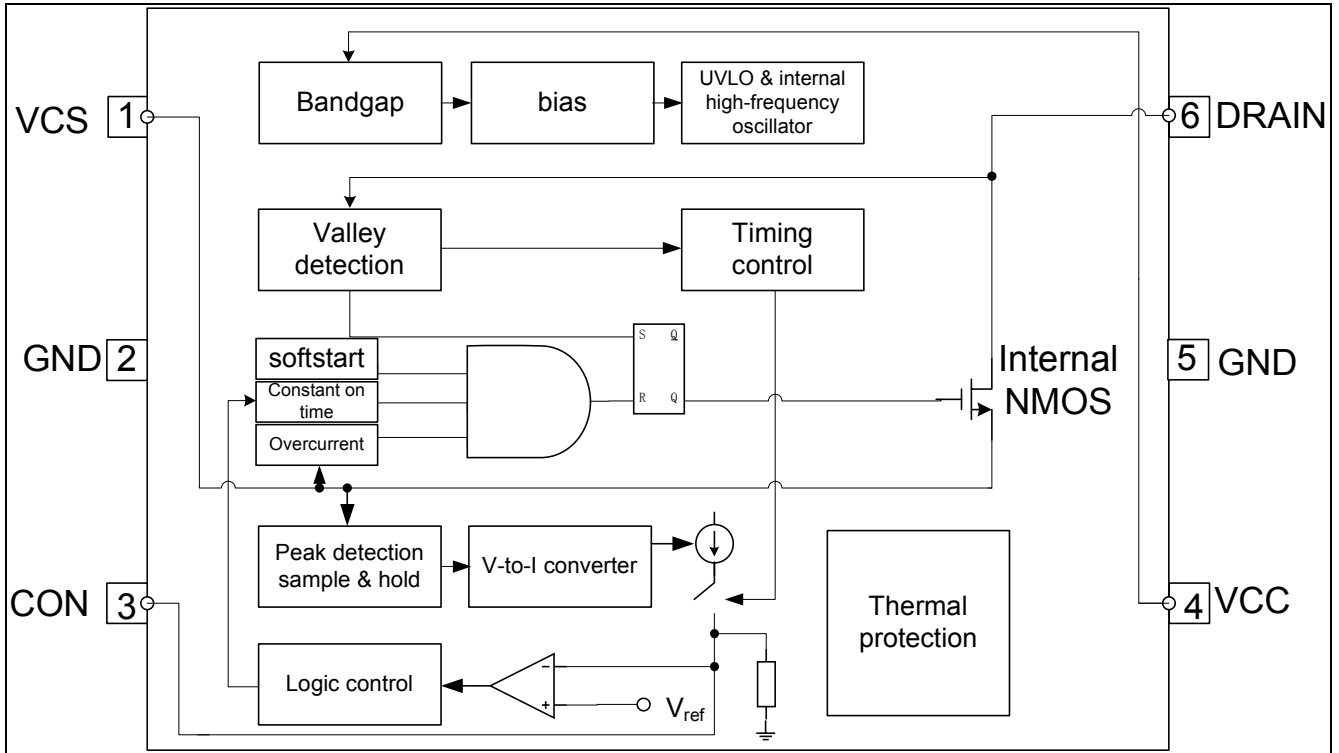


Figure 1 Internal Block Diagram

2 IC and Application Feature Overview

2.1 Application Feature SET

Table 1 Application Feature SET

Single Choke	Transformer Free	Support the use of Standard Chokes
BOM Count	< 22 Components	
Form Factor	Fit into: E14 / GU10 Sockets	
AC Line IN: Wide Range Opportunity	80V _{ACIN} - 325V _{ACIN}	Real Wide Range Design / Regulation of sudden Line Jumps
Star up behaviour		Smooth Start Up of LED Current
Expected Efficiency	86% up to 90%	
Maximum Junction Temperature	T _{JunctionMAX} = 150°C	
Maximum Ambient Temperature	T _{AmbientMAX} = 105°C	Temperature of PCB inside Bulb

2.2 IC Feature SET

Table 2 IC Feature SET

IC Operation MODE	Critical Conduction / DCM Op. / Constant t _{ON}	DCM Operation with Critical Conduction Operation
Package	PG-SOT23-6-1 / R _{thja} = 264K/W / 6 PINs	No Cooling Area ON PCB
Active PINs	4 active PINs + 2 GND	V _{CC} / Con / V _{CS} / DRAIN / GND
MOS Stage inside	R _{DS(on)25°C} = 0.370 Ω / I _{SWpeak} = 0.5A	Low Voltage Low Side MOSFET Integrated
Operating Condition	V _{CCop} = 10V / I _{CCop} around 0.82mA	@ active Gates for Applications up to 15W
f _{RUN}	40kHz up to 150kHz	Operating Frequency Range
Soft-Start	24ms Digital	
Internal System Accuracy (overall)	< 5% Up to T _{Jmax} = 150°C	Stable Overall Accuracy in a wide Temperature Range up to T _J

2.3 Regulation Feature SET

Table 3 Regulation Feature SET

Line Regulation	I _{LED} Variation < ± 5%	85V < V _{ACINnom} < 325V
Load Regulation	I _{LED} Variation < ± 5%	V _{FLED} from 20V up to 60% VIN
Constant OUTPUT Current Operation	I _{LED} Variation < ± 5%	

IC and Application Feature Overview

Compensation of Magnetic Impact		L_p Variation $\pm < 20\%$
Power Factor	Supports : EN61000-3-2	$> 70\%$ up to $\sim 99\%$
iATHD	Supports : EN61000-3-2	$< 20\%$
Harmonic Distortion	Supports : EN61000-3-2	PASS
Lightning Surge	Supports: EN61000-4-5	PASS
EMI	Supports: EN55015	PASS

2.4 Protection Feature SET

Table 4 Protection Feature SET

V_{CS} Short (PIN 1) to GND	$V_{CSth} < 0.1V$ & $V_{Drain} > 0.25V$ during t_{ON} $t_{Blanking} = 200ns$ Blanking Time	Start UP / RUN Mode	Latch
V_{CS} Open (PIN 1)	$V_{CSth} > 1.2V$ & $T_{Blanking} = 100ns$ After LEB triggered With 3 continuous switching cycle	Start UP / RUN Mode	Latch
V_{Con} Short (PIN 3) to GND	$V_{Conth} < 0.2V$ & $t_{Blanking} = 5ms$	Start UP	Latch
V_{Con} OPEN (PIN 3)	$V_{Con} > 1.5V$ & $t_{Blanking} = 18\mu s$	Start UP	Latch
Floating Load Protection (FLP)	$V_{CSth} < 0.12V$ & Start UP: After soft-start with 160ms blanking time Run MODE: After: 160ms Blanking Time	Start UP / RUN Mode Disabled during OTP	Latch
Short OUTPUT	$V_{CSth} > 0.62V$ & No Zero current Detection for continuous 126 Switching Cycles	Start UP / RUN Mode	Latch
Short Winding (Main Choke)	$V_{CSth} > 1.2V$ & $T_{Blanking} = 100ns$ After LEB triggered With 3 continuous switching cycle	Start UP / RUN Mode	Latch
Power Limitation	$V_{CSth} = 0.9V$ Cycle by Cycle	RUN Mode	Limiting

IC and Application Feature Overview

iOTP Intelligent Over Temperature Protection	$T_J > 150^{\circ}\text{C} \pm 10^{\circ}\text{C}$ I_{OUT} from 100% to 50%	Start UP / RUN Mode	De-rating within 7 digital Steps
V_{CC} Under Voltage (UVLO)	$V_{\text{CC}} < 6.0\text{V}$	Start UP / RUN Mode	Auto Restart
Dimmer Input Acceptable	UVLO	Start UP / RUN Mode	Auto Restart
iATHD Feature	On Time Reduction	RUN Mode Disabled during OTP	N.A.
Soft Start digital 24 ms	$V_{\text{CStH}} = 0.1\text{V}$ till 3 ms $V_{\text{CStH}} = 0.2\text{V}$ till 6 ms $V_{\text{CStH}} = 0.3\text{V}$ till 9 ms $V_{\text{CStH}} = 0.4\text{V}$ till 24 ms	Start UP	Limiting

3 Pin Configuration and Functionality

3.1 Pin Configuration with PG-SOT23-6-1

Table 5 Pin configuration

Pin	Symbol	Function
1	V _{cs}	Current Sense
2	GND	Ground
3	Con	Constant Current / Output Current Ripple
4	V _{cc}	Supply Voltage
5	GND	Ground
6	DRAIN	DRAIN of integrated MOSFET

3.2 Package

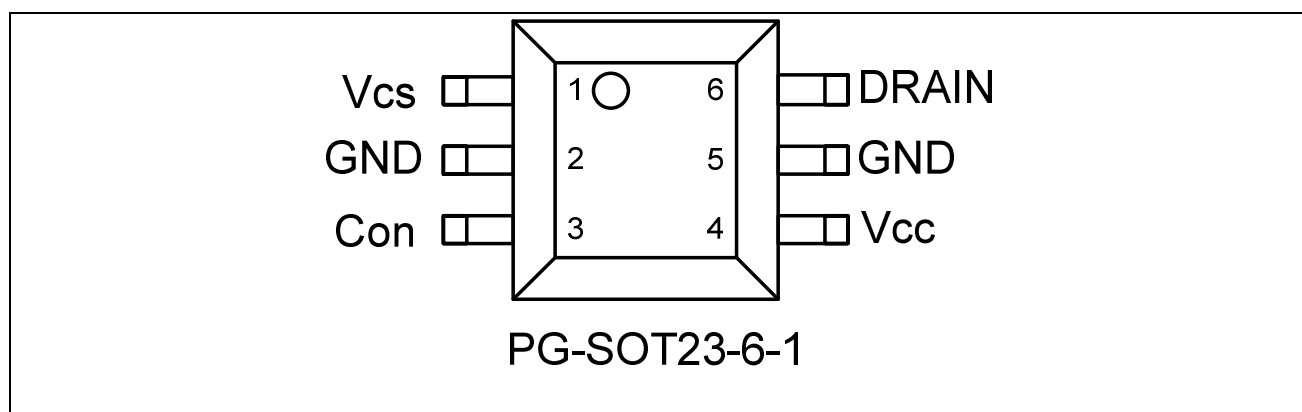


Figure 2 Pin configuration PG-SOT23-6-1 (top view)

3.3 Pin Description

V_{cs} (current sense, pin 1)

This pin is directly connected to the shunt resistor, which is located between the source terminal of the integrated low-side MOSFET and ground.

Internal clamping structures and filtering measures allow sensing of the source current for the low-side power MOSFET without additional filter components.

This pin is for power limitation, output average current regulation & the integrated protection features.

GND (ground, pin 2)

This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate drive and sense signals.

Con (constant current, pin 3)

Regulate the constant current in the output stage of the Floating BUCK converter.

Pin Configuration and Functionality

V_{CC} (supply voltage, pin 4)

This pin provides the power supply of the ground-related section of the IC. There is a UVLO turn-on threshold at 7.5 V ($V_{CC.ON}$) and a UVLO turn-off threshold at 6.0 V ($V_{CC.OFF}$). The maximum V_{CC} supply voltage level is 18.0 V. The chip supply current is typically at $I_{VCC} = 0.82$ mA.

GND (ground, pin 5)

This pin is connected to ground and represents the ground level of the IC for the supply voltage, gate drive and sense signals.

DRAIN (DRAIN, pin 6)

This pin is connected to the drain of the internal low side MOSFET. It is also used for protection features.

4 Functional Description

4.1 Typical Application Circuit

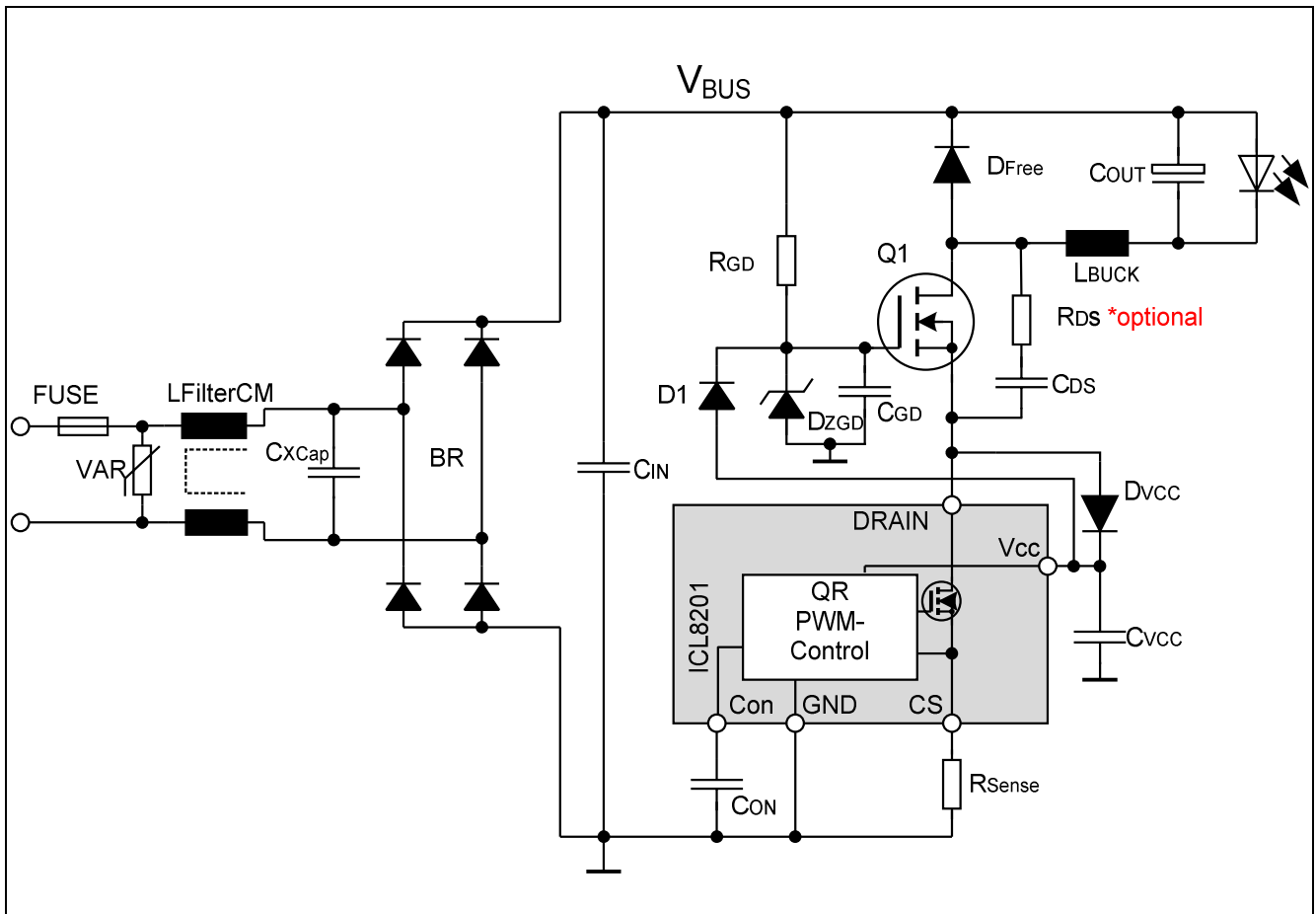


Figure 3 Application Circuit of a LED Driver in a Floating BUCK Topology

Description

The ICL8201 is a cascode structure current mode controller for non-isolated single-choke floating BUCK topologies. The device is tailored for LED applications and provides constant current operation with low output current ripple in a real universal line input voltage range as well as load compensation for a wide output voltage range.

The low PIN count PG-SOT23-6-1 package supports small form factor and low-cost designs. The high level of integration enables a minimum of effort for addition of external components. The ICL8201 control concept supports DC and AC input as well as high Power Factor Correction (PFC), high efficiency levels and reduced EMI designs in critical conduction operation mode without zero crossing detection winding. Along with outstanding integrated regulation and protection features, the cascode arrangement simplifies V_{CC} supply of the IC, that eliminates the need of a depletion MOS. The regulation is done without detecting the AC line input voltage or sensing the output voltage. All these features are implemented with a minimum amount of external components. The device operates in a wide junction temperature range from -25°C to 150°C . The highly efficient integrated low-voltage MOSFET will eliminate the need for any additional thermal management.

4.2 Internal Functional Description

4.2.1 V_{CC} Pre-Charging and Typical V_{CC} voltage profile During Start-up

In ICL8201, a startup cell is not needed. As shown in Figure 4, once the mains input voltage is applied, a rectified voltage V_{BUS} appears across the capacitor C_{IN} . The pull up resistor R_{GD} provides a current to charge the C_{GD} capacitor and gradually generate one voltage level for the gate of external power MOSFET Q_1 . If voltage over C_{GD} is high enough, V_{CC} capacitor will be charged through external LED load, choke inductor L_{BUCK} , external power MOSFET Q_1 , and diode D_{VCC} . Because capacitor C_{GD} is quite small (around 10nF), so charging this capacitor and consequently charging V_{CC} capacitor C_{VCC} will be within very short time. There is one zener diode, D_{ZGD} which is used to clamp voltage over C_{GD} and its breakdown voltage can be 12V, so during startup, V_{CC} voltage will be charged up to $12V - V_{threshold} - V_F$ (where $V_{threshold}$ is threshold voltage of power MOSFET Q_1 and V_F is forward voltage of D_{VCC}).

When V_{CC} voltage reach UVLO turn-on threshold (which is 7.5V), the whole chip will be turned on and system will enter into normal operation after soft start. During normal operation, V_{CC} capacitor will be charged through bypass capacitor C_{DS} and power MOSFET (when V_{CC} is lower than $12V - V_{threshold} - V_F$).

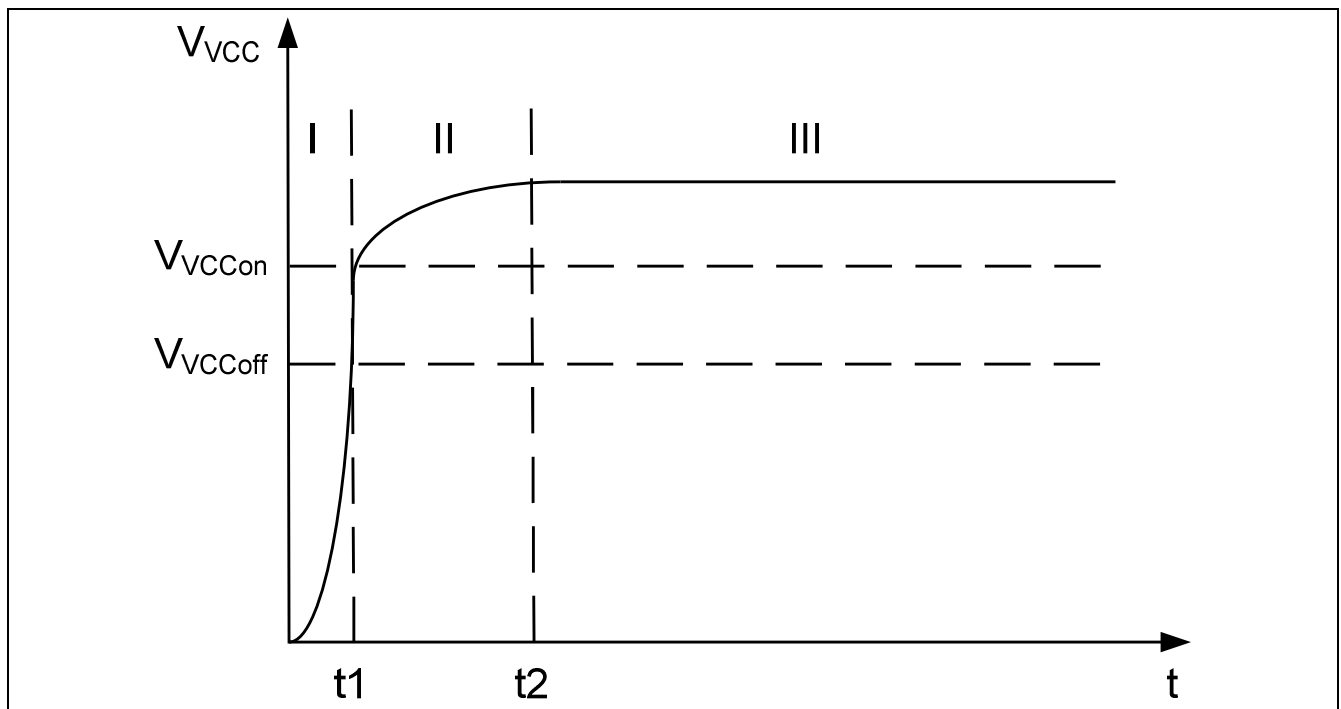


Figure 4 V_{CC} voltage at start up

When the V_{CC} voltage exceeds the V_{CC} turned-on threshold $V_{VCC.ON}$ at time t_1 , the IC begins to operate with soft-start. V_{CC} capacitor will be charged through bypass capacitor C_{DS} , as shown in **Figure 6**. After some time, when V_{CC} voltage is high enough, it will be clamped by the external Zener diode D_{ZGD} .

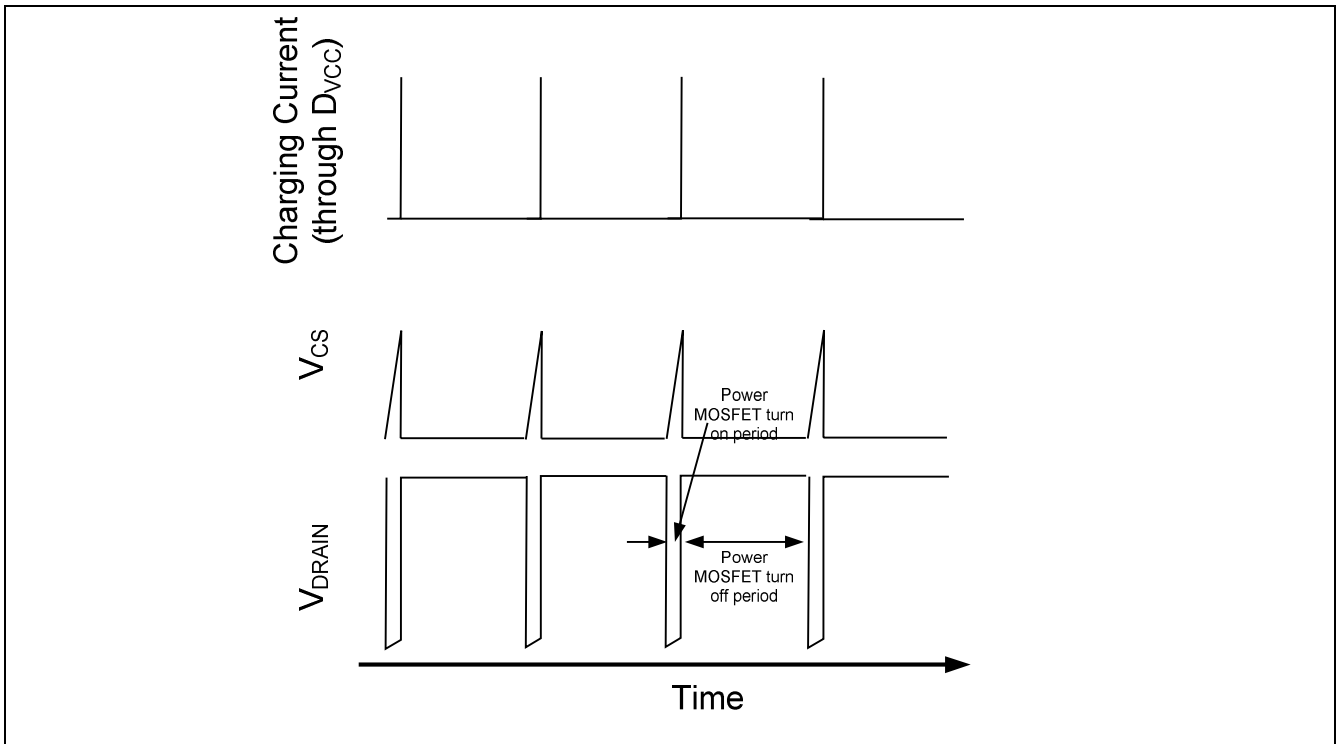


Figure 5 Charging current to V_{CC} capacitor during normal operation

4.2.2 Soft Start

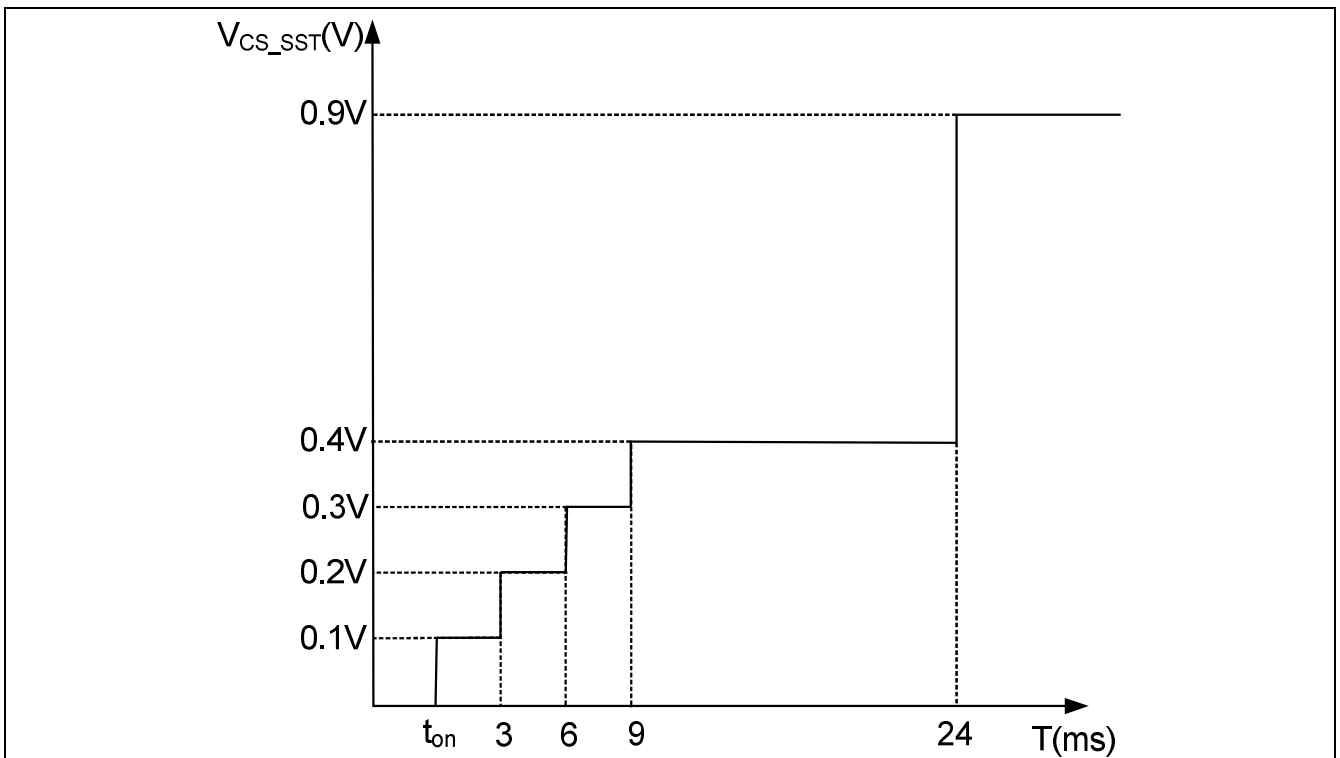


Figure 6 Soft-Start profile

As shown in Figure 7, at time t_{on} , the IC begins to operate with a soft-start. By using this soft-start, the switching stresses for the switch, diode and choke inductor are minimized. The Soft-Start implemented in ICL8201 is a digital time-based function. The preset soft-start time is t_{SS} (24ms) with 4 steps. If not limited by other functions, the peak voltage on V_{CS} pin will increase step by step from 0.1V to 0.4V finally.

After soft start, the peak V_{CS} is limited by 0.9V current limitation.

4.2.3 Normal Regulation Operation

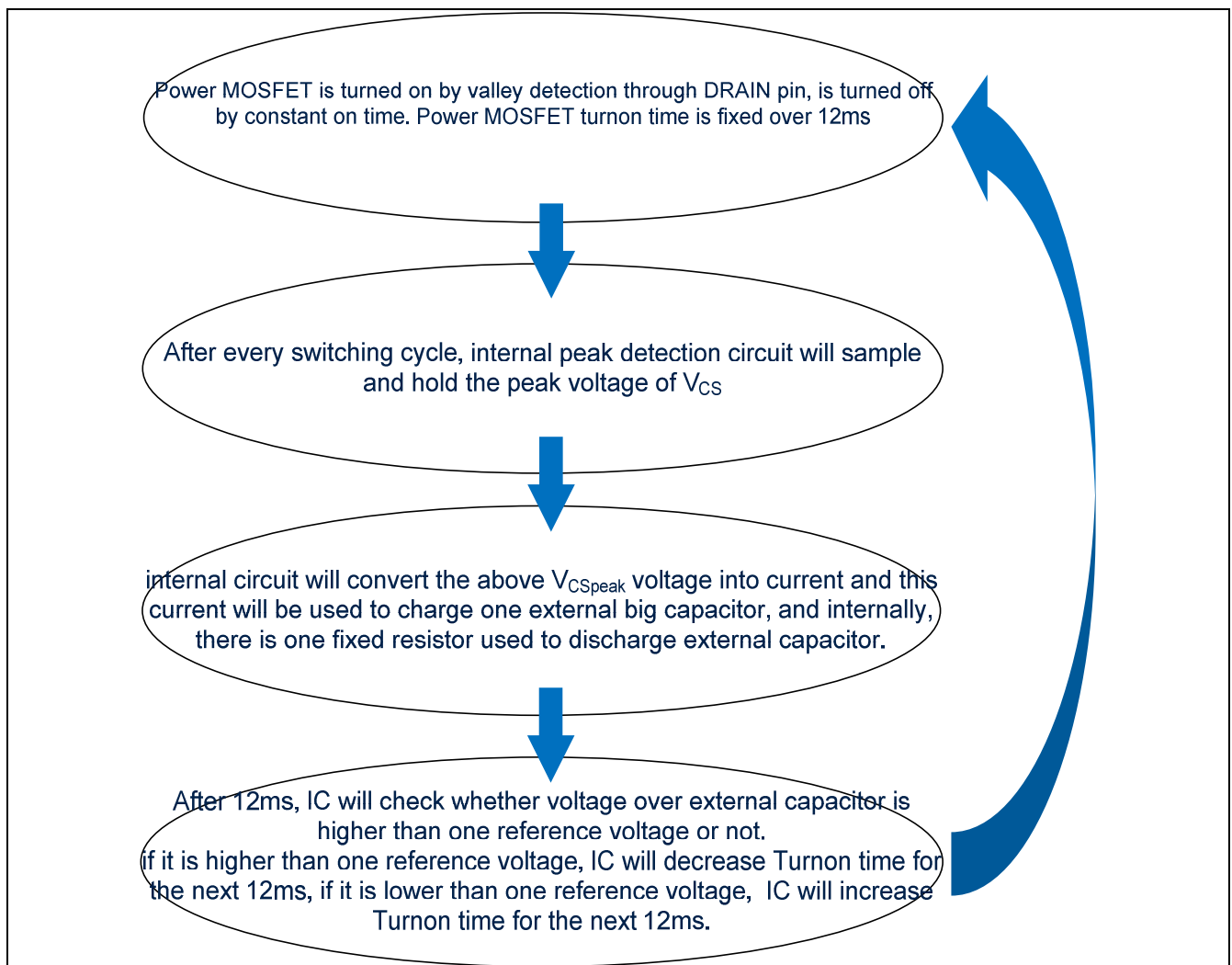


Figure 7 Normal regulation operation of ICL8201

4.2.4 Zero Current Detection

In the ICL8201 system, when power MOSFET is being turned on, current through choke inductor L_{BUCK} will linearly ramp up, when power MOSFET is being turned off, current through choke inductor will linearly ramp down until 0A.

Later when current through choke inductor reaches 0A, system will start to oscillate. In order to turn on power MOSFET when current through choke inductor reduce to 0A, it is necessary to do zero current detection for system.

As shown in Figure 9, zero current detection is achieved by the following circuit.

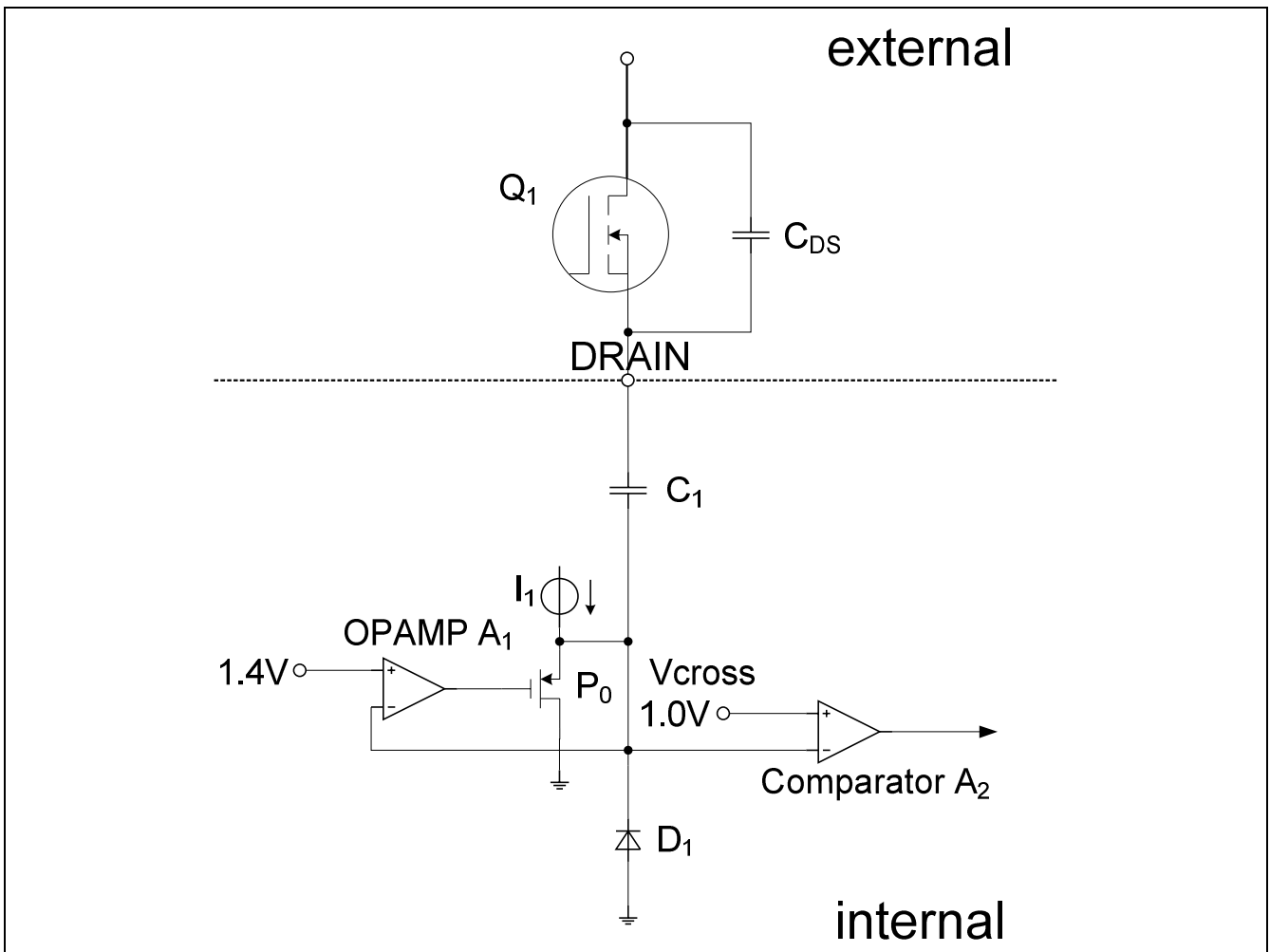


Figure 8 Zero current detection circuit implemented in ICL8201

The above block diagram shown in Figure 9, where capacitor C_{DS} is used to couple the high frequency signal to IC Drain and internally IC will accept the oscillation signal and do zero current detection. Internally, capacitor C_1 will be used to further couple oscillation signal at DRAIN pin into low voltage signal; current source I_1 and operational amplifier is used to ensure the maximum V_{cross} voltage to be 1.4V when there is no oscillation at the Drain pin; diode D_1 is used to clamp point V_{cross} voltage not lower than -0.7V when power MOSFET is being turned on; when there is some high frequency signal transferred to point V_{cross} , the V_{cross} will be pulled down, and there is one comparator which is used to detect if V_{cross} is lower than 1.0V. When V_{cross} is lower than 1.0V, zero current point is detected. The typical DRAIN voltage Slew Rate necessary for zero current detection is 50V/ μ s for a ΔV_{DRAIN} of 0.5V and 2.5V/ μ s for a ΔV_{DRAIN} of 0.8V.

As shown in Figure 10, upper side power MOSFET drain voltage and lower side power MOSFET drain & current through choke inductor with zero current detection used.

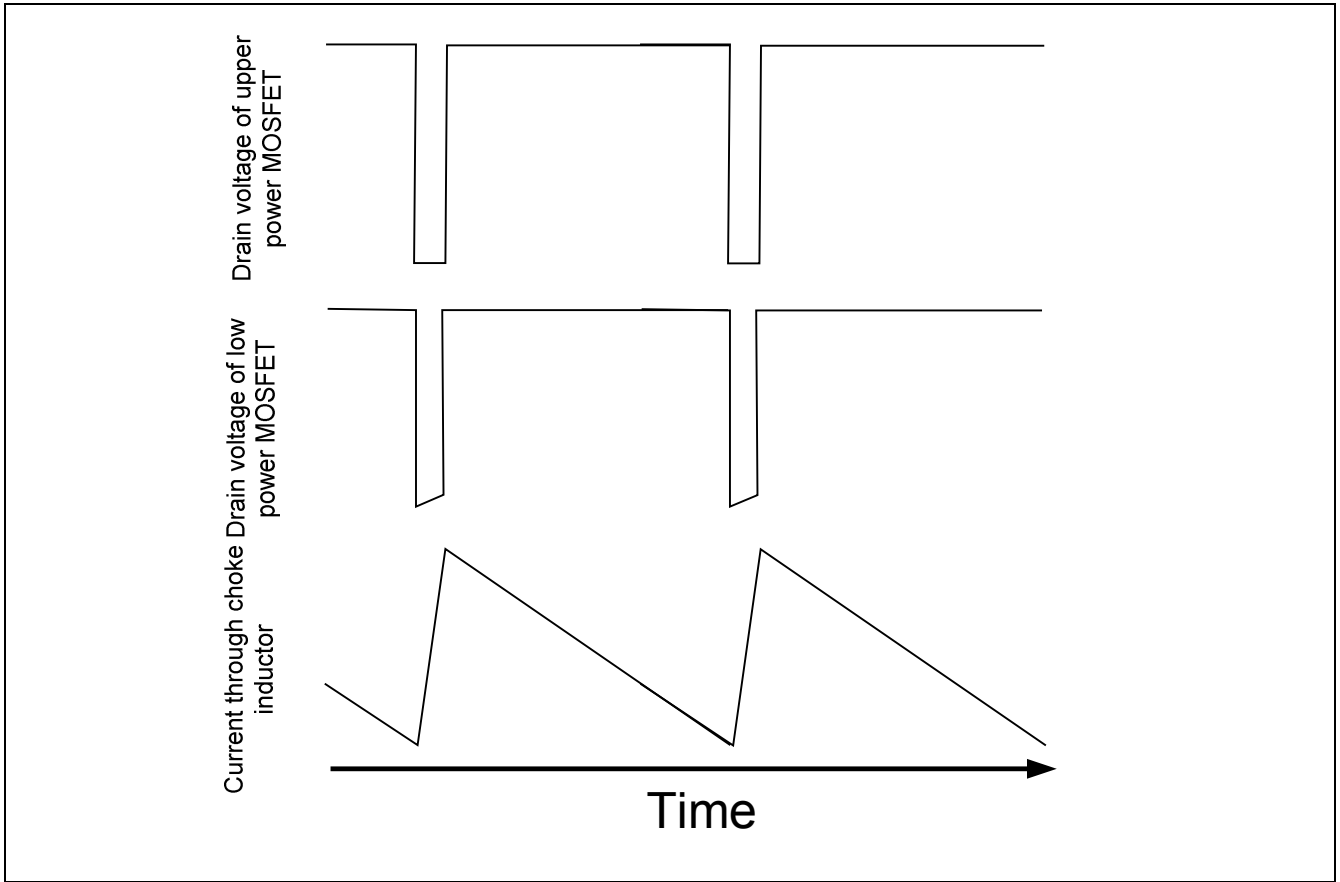


Figure 9 Waveform to show how is the drain voltage and current through choke inductor behave when zero current detection used

4.2.5 Peak Detection

In order to do output current measurement and regulation, it is necessary to do V_{CS} voltage peak detection. As shown in Figure 11, the peak voltage value of V_{CS} is sample and hold for output current regulation purpose.

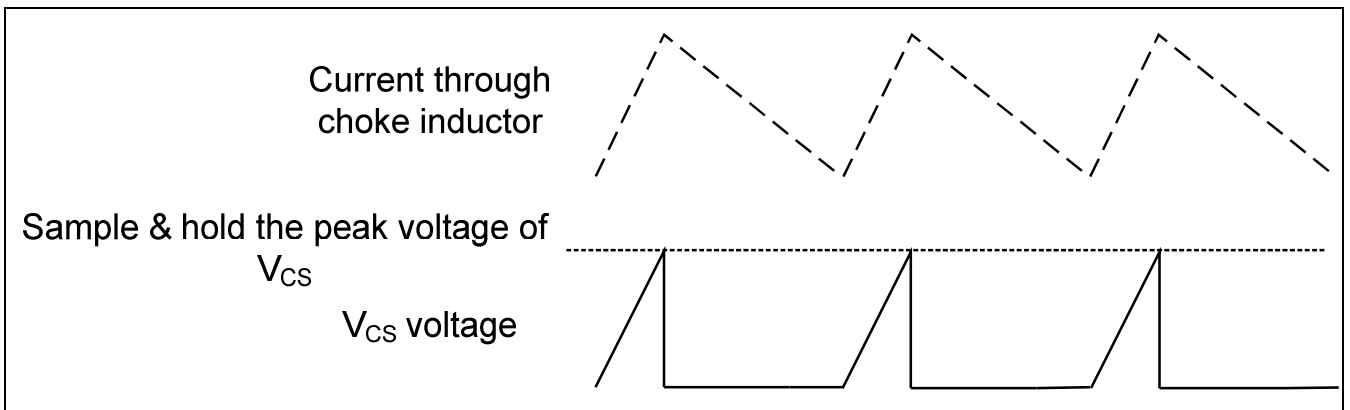


Figure 10 Waveform to show peak detection of V_{CS} signal

4.2.6 Voltage to Current Converter

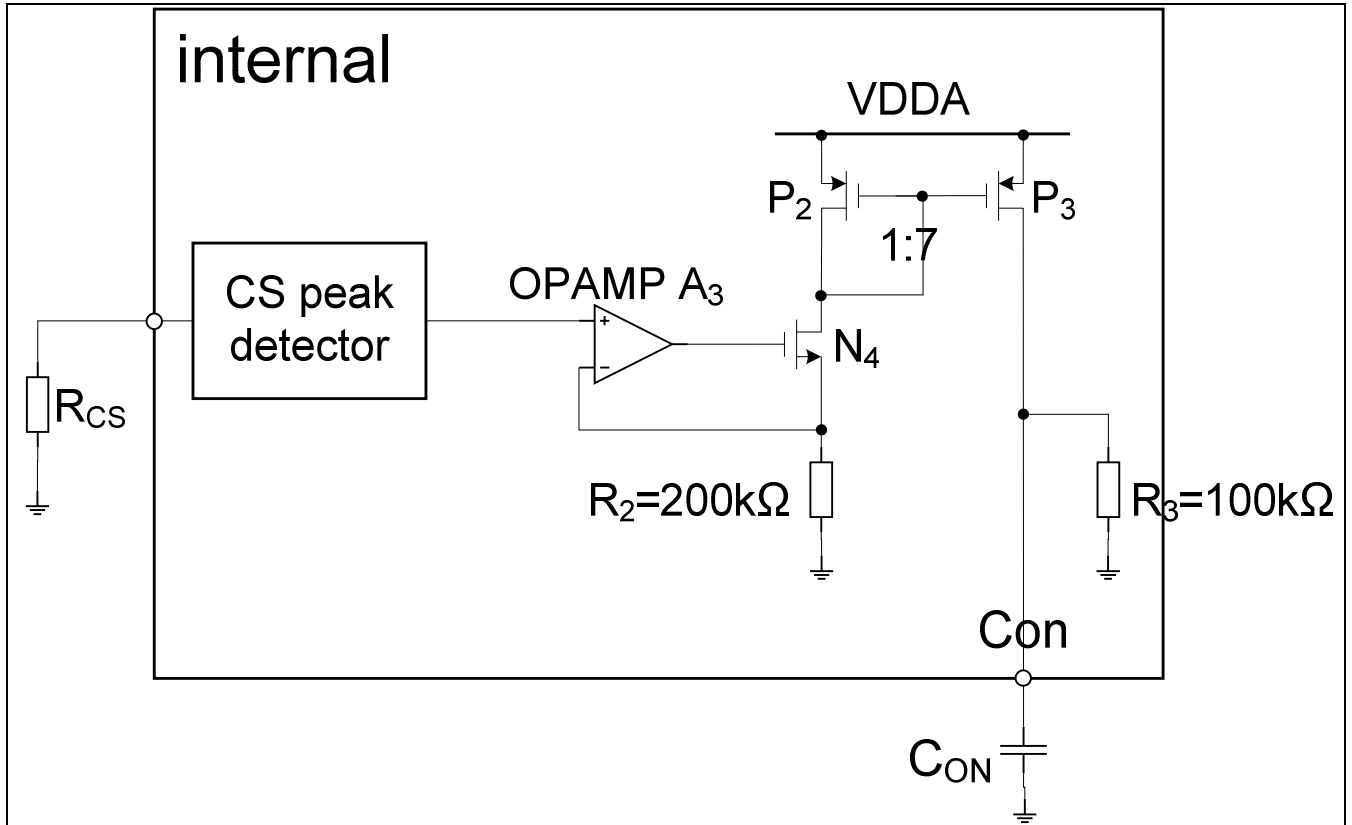


Figure 11 Block diagram to show peak detection & Voltage to Current block with current mirror circuit diagram

From the above block diagram, at first V_{CS} peak voltage is sample and hold, which will be applied to one Voltage to Current converter block, this voltage to Current converter block includes OPAMP A_3 , NMOS transistor N_4 and resistor R_2 .

The current I_{CSpeak} will be equal to V_{CSpeak} / R_2 . This I_{CSpeak} will be mirrored by P_2 and P_3 into 7-times current source to charge external capacitor C_{ON} . Also there is one resistor R_3 which is connected from Con to GND. The external C_{ON} works together with this internal resistor R_3 establish the C_{on} voltage which will be applied to the internal coarse and fine tuning block to determine the ON time, T_{ON} .

4.2.7 ON time generation

ICL8201 uses constant on time control method, it can accept universal input voltage with wide output voltage range. The On time range is between $0.8\mu\text{s}$ and $20\mu\text{s}$. The On Time is preset to 800ns during start up. The percentage of On time change is dependent on V_{Con} voltage. V_{Con} voltage is sensed every 12ms typically. The percentage of On time change with respect to V_{Con} voltage is shown in Table 2.

Table 6 Tuning mechanism used in ICL8201

V_{Con} voltage	On time
$V_{Con} > 1.8\text{V}$	Decrease by 50%
$1.8\text{V} > V_{Con} > 1.6\text{V}$	Decrease by 10%
$1.6\text{V} > V_{Con} > 1.5\text{V}$	Decrease by 0.2%
$1.4\text{V} < V_{Con} < 1.5\text{V}$	Increase by 0.2%
$1.2\text{V} < V_{Con} < 1.4\text{V}$	Increase by 10%
$V_{Con} < 1.2\text{V}$	Increase by 50%

4.2.8 How to calculate output average current

The average of the V_{CS} peak voltage divided by external sense resistor R_{CS} will be the 2 times of the average current through choke inductor. Output average current only depends on sense resistor value, in order to get target output average current, equation 5.1 can be followed

$$I_{output} = \frac{1}{2} \times \frac{1.5}{3.5 \times (R_{CS})} \quad (5.1)$$

Where R_{CS} is sense resistor value and 3.5 is Peak V_{CS} amplifier gain, 1.5V is C_{ON} threshold voltage.

4.2.9 Leading Edge Blanking

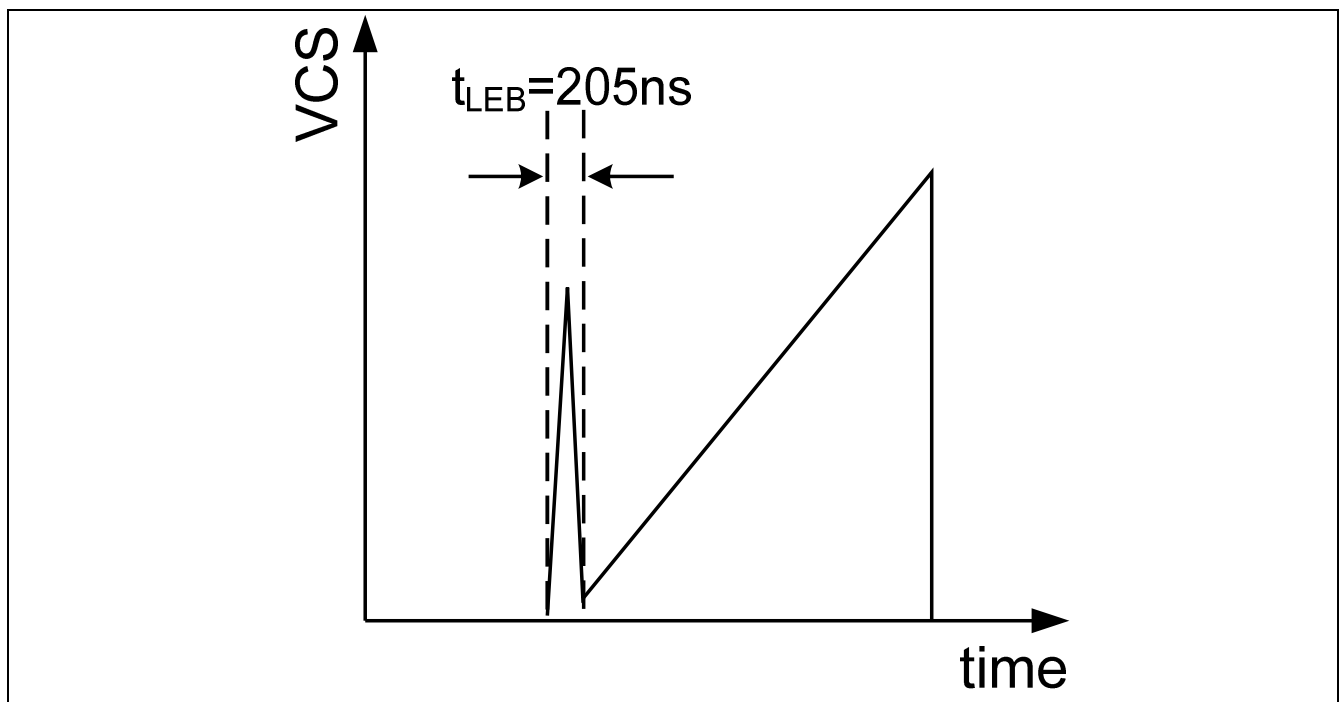


Figure 12 Leading Edge Blanking

Whenever the power MOSFET is switched on, a leading edge spike is generated due to parasitic capacitances. This spike can cause the gate drive to switch off unintentionally. In order to avoid a premature termination of the switching pulse, this spike is blanked out with a time constant of $t_{LEB}=205ns$.

4.2.10 Driver Stage

Cascode topology is adopted in ICL8201 system, one fixed voltage (for example: 12V) is applied to the Gate of the upper side power MOSFET, then if lower side power MOSFET is turned on, the whole current path will be turned on; if lower side power MOSFET is turned off, the whole current path will also be turned off.

4.3 System Functional description

4.3.1 Start-Up behaviour

4.3.1.1 Start-Up: Into Normal Operation

Start-up is executed in 3 phases: UVLO, power-up and soft start, as shown in figure 14. When the bus voltage is applied, the V_{CC} capacitor C_{VCC} is charged up until V_{CC} reaches the V_{CC} 'ON' threshold of $V_{CC,ON} = 7.5\text{ V}$. After exceeding this threshold, the IC powers up into the soft start. V_{CON} is charged up, the internal MOSFET starts switching.

There is one fast charge function which is used to charge Con pin quickly to 1.5V after IC start to work.

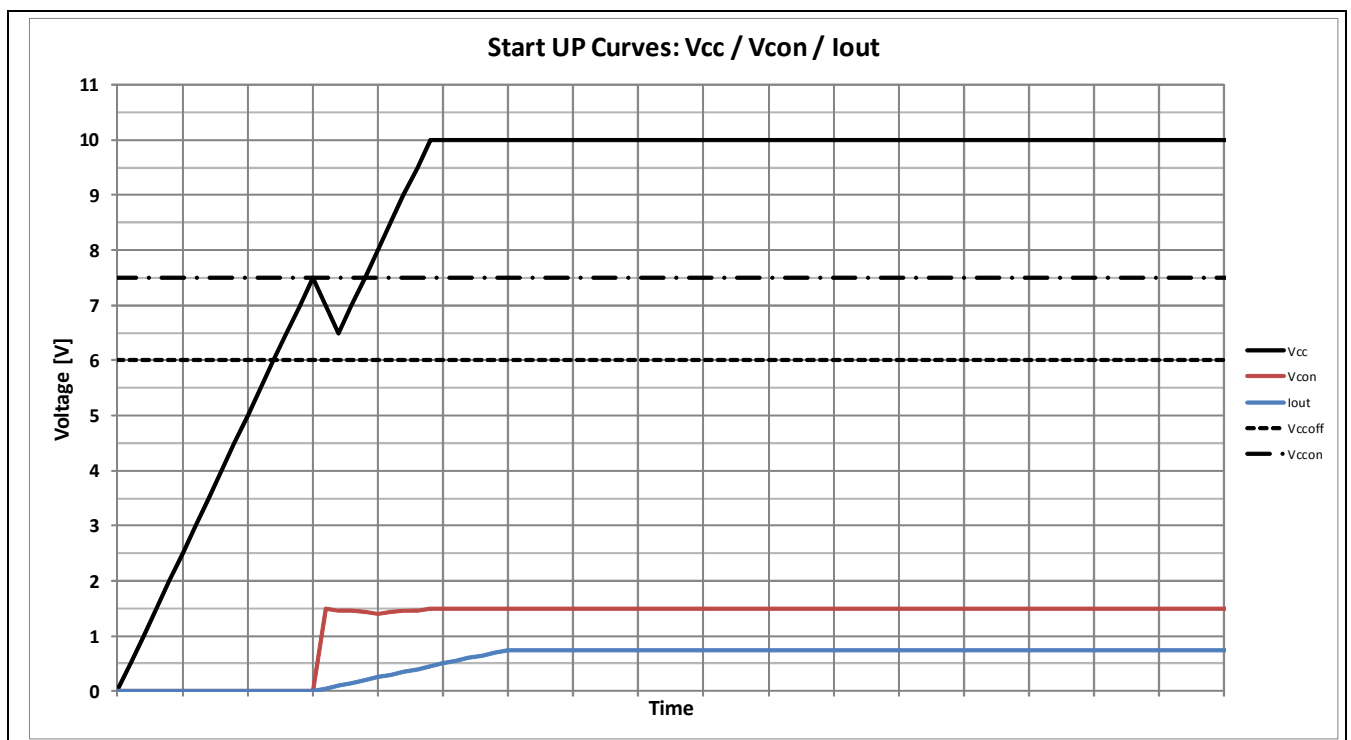


Figure 13 Start Up

4.3.1.2 Start-Up: Soft-Start Phase

During the digital Soft-Start phase, the current sensing voltage V_{CS} is limited from 0.1 V up to 0.4 V. After the soft start phase (24 ms), the peak current sensing voltage threshold is set to $V_{CS} = 0.9$ V for current limitation. Two additional thresholds are set in order to detect output short and short winding conditions. The first set to be $V_{CSthShort} = 0.6$ V with no zero current detection as protection against short OUTPUT and second set to be $V_{CSthShort} = 1.2$ V when a short winding at the BUCK choke, L_{BUCK} , happens. In figure 15, shows the voltage behavior during start-up into normal operation.

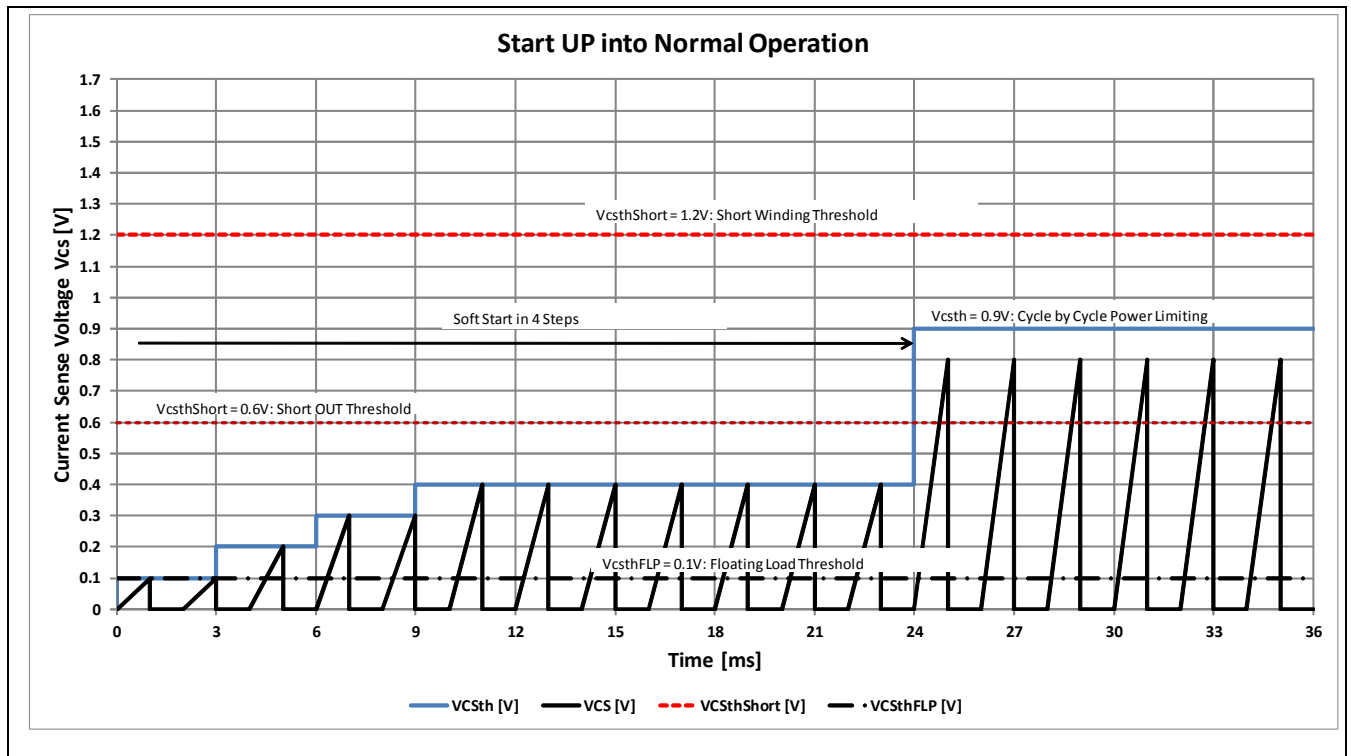


Figure 14 Soft-Start

4.3.1.3 Start-Up: Short Output

During the digital Soft-Start phase, a short output is detected when the current sensing voltage V_{CS} exceeds the $V_{CSthShort} = 0.6\text{ V}$ threshold and the internal zero current detection signal is missing. The controller stops working after a consecutive 126 switching cycles and enters into the LATCH OFF mode.

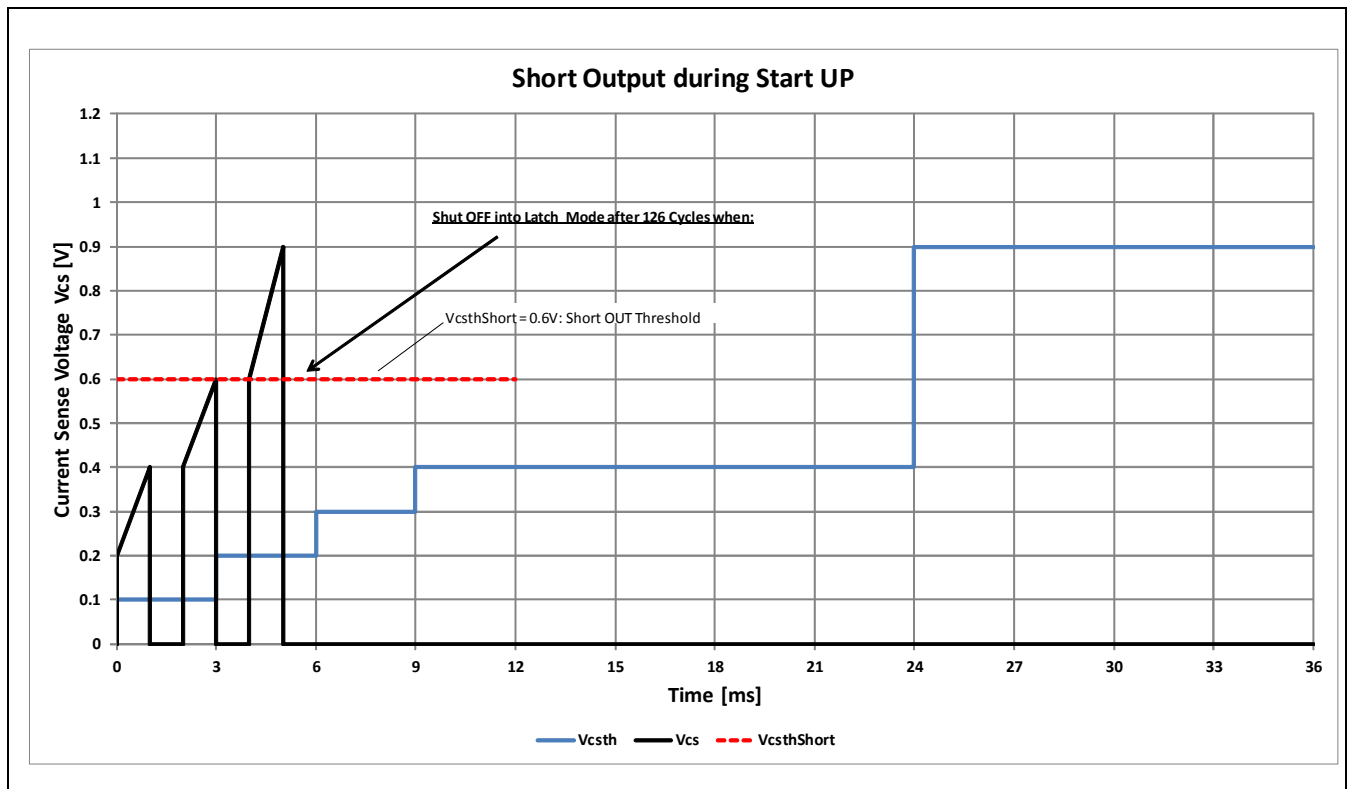


Figure 15 Short Output

4.3.1.4 Start-Up: Floating Load Protection

There is no effective floating load protection available. The risks during open or floating load are that the output voltage will be charged to the same voltage as input. If output capacitor, C_{OUT} , is not selected above the rated input voltage, it is recommended to include an output clamp circuit to prevent output capacitor, C_{OUT} , from operating above its rated voltage during open or floating load conditions.

An open output (floating load) is detected when the current sensing voltage V_{CS} stays below $V_{CsthFLP} = 0.12\text{ V}$ for 24 ms (soft start time) + 160 ms. After this blanking time, the controller stops working and enters into the LATCH OFF mode.

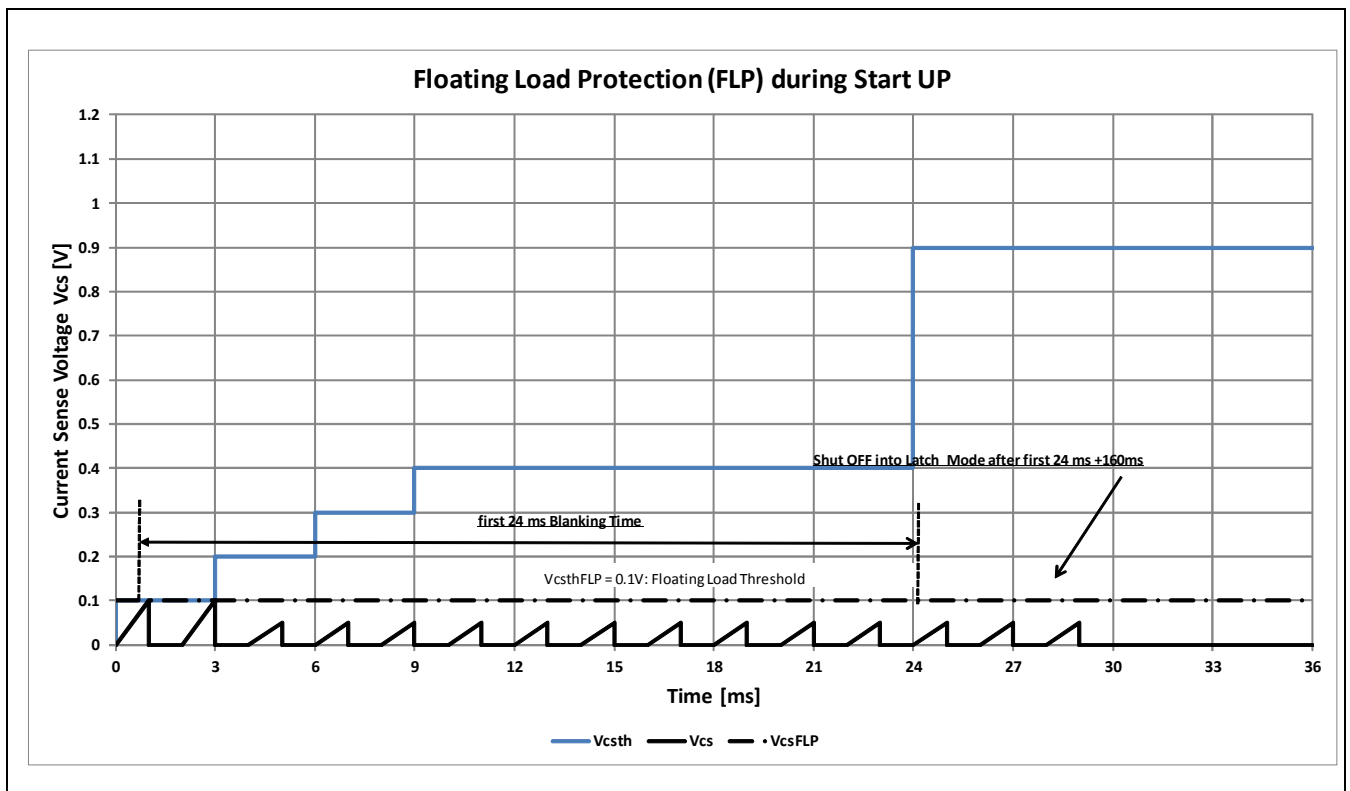


Figure 16 Floating Load Protection