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LED System Driver IC

ICLS8023Z

Off-Line LED Current Mode Controllers
with Integrated 800 V CoolMOS™ & Startup Cell

Data Sheet

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Current Mode Controller with Integrated 800 V Startup Cell/Depletion CoolMOS™

Product Highlights

- 800 V avalanche-rugged CoolMOS™ with startup cell
- Adjustable blanking window for high-load jumps to increase reliability
- Frequency jittering and soft driving for low EMI
- Auto Restart protection for overload, overtemperature, overvoltage and undervoltage
- Pb-free lead plating, RoHS-compilant

Features

- 800 V avalanche-rugged CoolMOS™ with startup cell
- 65 kHz internally-fixed switching frequency with jittering feature
- Auto Restart mode for overtemperature detection
- Auto Restart mode for overvoltage detection
- Auto Restart mode for overload and open loop
- Auto Restart mode for VCC undervoltage
- Floating Load Protection (FLP) mode in the case of open loads
- External auto-restart enable pin
- Overtemperature protection with 50 °C hysteresis
- Built-in 10 ms soft start
- Built-in 20 ms and extendable blanking time for short duration peak power
- Propagation delay compensation for both maximum load and burst mode
- Overall tolerance of current limiting < ± 5 %
- Internal leading edge blanking
- BiCMOS technology for low power consumption and wide VCC voltage range
- Soft gate drive with 50 Ω turn-on resistor

Description

controllers employ a fixed-frequency operation mode optimized for offline LED lighting. The integrated constant power function (patented by Infineon Techologies AG) and the frequency jitter enable high performance without investment of too much effort in stabilization of the system and filtering in terms of EMC.

A wide VCC range up to 26 V is provided by use of BiCMOS technology to cover changes in the auxiliary supply voltage if a CV/CC regulation is implemented on the secondary side.

Auto Restart Mode is entered in the case of overtemperature, VCC overvoltage, output open loop or overload and VCC undervoltage. If an open load event occurs, the device enters the so-called Floating Load Protection (FLP) mode to protect the LED against destruction. The dimensions of the transformer and the secondary diode can be reduced owing to the internal precise peak current limitation to yield greater cost efficiency.

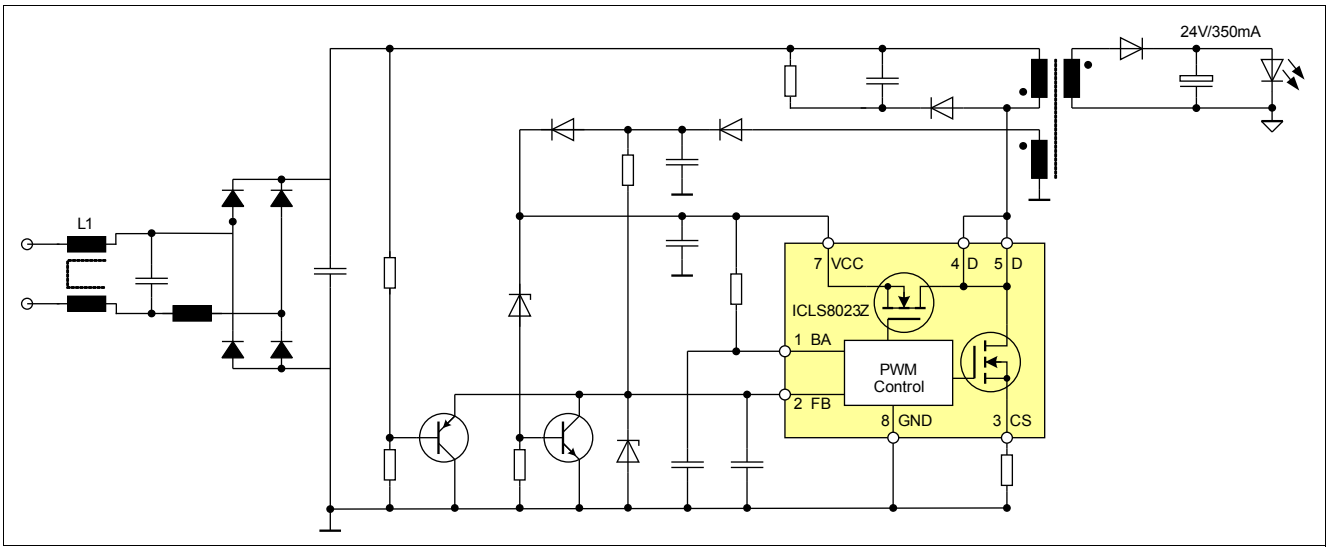

Figure 1 Typical application of ICLS8023Z controllers

Type	Package	Marking	V_{DS}	F_{OSC}	R_{DSon} [1]	230 VAC ± 15 % [2]	110 VAC ± 15 % [2]
ICLS8023Z	PG-DIP-7	ICLS8023Z	800 V	65 kHz	2.26 Ω	24 W	12 W

1) typ. @ T = 25 °C

2) Calculated maximum input power rating at T_a = 80 °C, T_j = 125 °C and without copper area as heat sink

1 Pin Configuration and Functionality

1.1 Pin Configuration for PG-DIP-7

Table 1 Pin Configuration for PG-DIP-7

Pin	Symbol	Function
1	BA	Extended blanking time & auto-restart enable
2	FB	Feedback
3	CS	Current Sense / 800 V[1)] depletion CoolMOS™ source
4	n.c.	Not connected
5	Drain	800 V[1)] CoolMOS™ drain
6	–	No pin
7	VCC	Controller supply voltage
8	GND	Controller ground

1) @ T_j = 110 °C

1.2 PG-DIP-7 Package

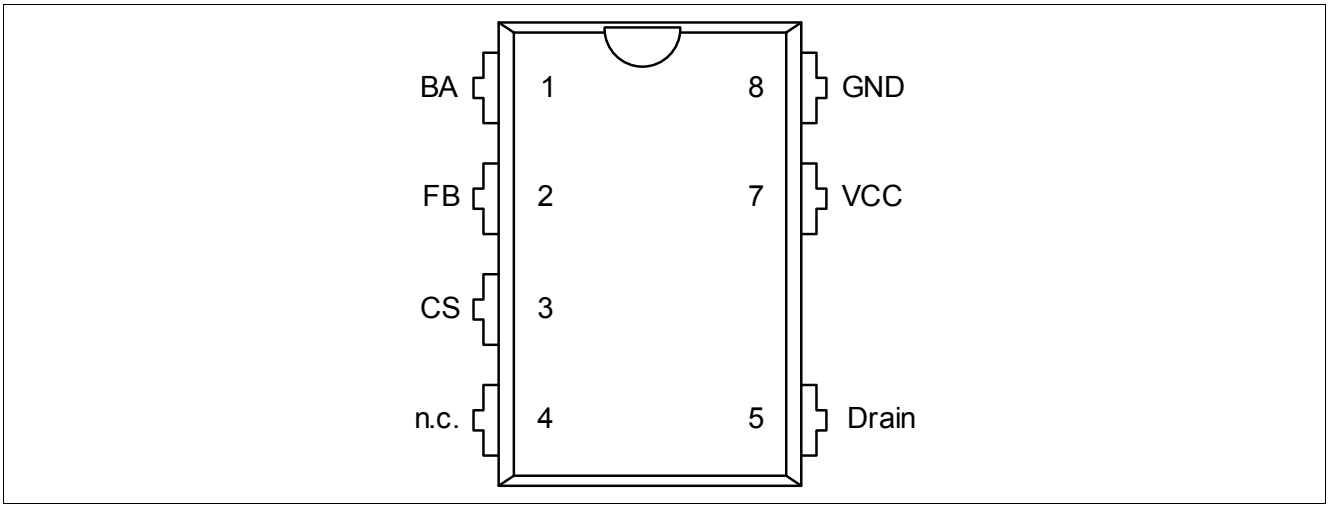

Figure 2 Pin configuration of PG-DIP-7 (top view)

1.3 Pin Functionality

BA (extended blanking time & auto-restart enable)

The BA pin combines the functions of extendable blanking time for overload protection and the external auto-restart enable. The extendable blanking time function is to extend the built-in 20 ms blanking time for overload protection by adding an external capacitor to ground. The external auto-restart enable function is an external access to stop the gate switching and force the IC to enter auto-restart mode. It is triggered by pulling the pin voltage to less than 0.4 V.

FB (feedback)

The information on the regulation is provided by the FB pin to the internal protection unit and to the internal PWM comparator to control the duty cycle. In the event of an open load event, the device enters the Floating Load Protection (FLP) mode.

CS (current sense)

The current sense pin senses the voltage developed on the series resistor inserted into the source of the integrated depletion CoolMOS™. If CS reaches the internal threshold of the current limit comparator, the driver output is immediately switched off. The current information is provided to the PWM comparator to realize the current mode.

Drain (drain of integrated depletion CoolMOS™)

The drain pin provides the connection to the drain of the internal depletion CoolMOS™.

VCC (power supply)

The VCC pin is the positive supply of the IC. The operating range of the supply is between 10.5 V and 25 V.

GND (ground)

The GND pin is the common ground of the controller.

2 Block Diagram

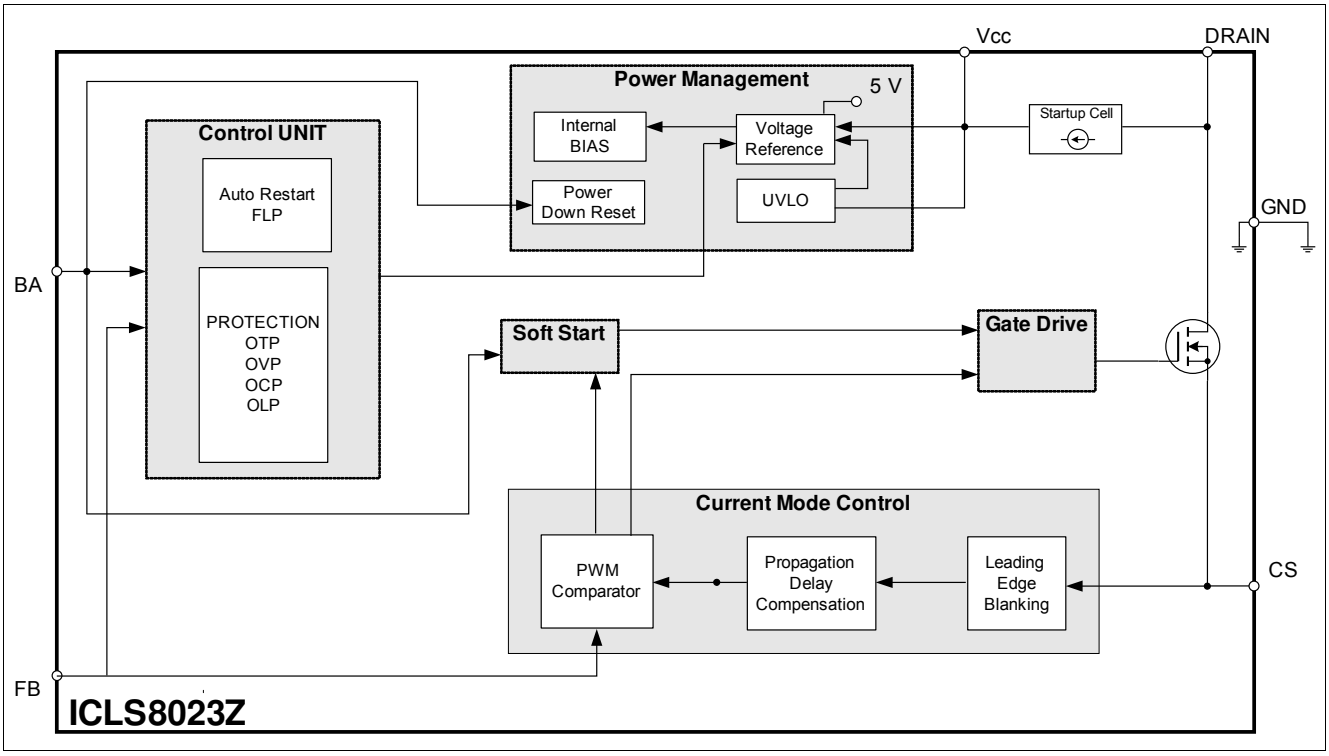

Figure 3 Block diagram of ICLS8023Z controllers

3 Functional Description

All values used in the functional description are typical values. When calculating the worst cases, the minimium/maximum values listed in **Electrical Characteristics** on page **32** have to be considered.

3.1 Introduction

For ICLS8023Z controllers, a high voltage startup cell is integrated into the system IC, which is switched off once the undervoltage lockout-on threshold of 17 V is exceeded. This startup cell is part of the integrated depletion CoolMOS™. The external startup resistor is no longer necessary as the startup cell is connected to the drain, resulting in reduced power losses. This increases the efficiency under light load conditions drastically.

The soft start capacitor is also used for providing an adjustable blanking window for high load jumps. The overload detection function is disabled during this window. With this concept, no further external components are necessary to adjust the blanking window.

An Auto Restart mode is implemented in the IC to reduce the average power conversion in the event of malfunction or unsafe operating conditions in the LED drives. This feature increases the system's robustness and safety, which would otherwise lead to a destruction of the LED drive. Once the malfunction is corrected, normal operation is automatically initiated after the next startup phase.

Together with the soft start capacitor, the feedback can also sense a missing load, which leads to rising output and auxiliary voltages. This triggers the Floating Load Protection (FLP) mode. When feedback falls below 1.35 V, the Soft Start voltage begins to rise up to a threshold of 4 V (depends on the C4 value) and the IC is switched into FLP mode.

The precise internal peak current limitation reduces the costs for the transformer and the secondary diode. The influence of the change in the input voltage on the power limitation can be avoided together with the integrated Propagation Delay Compensation circuit. Consequently, the maximum power is practically independent of the input voltage required for wide range LED drives. There is no need for additional oversizing of the LED drives – e.g., for the transformer or the secondary diode.

3.2 Power Management

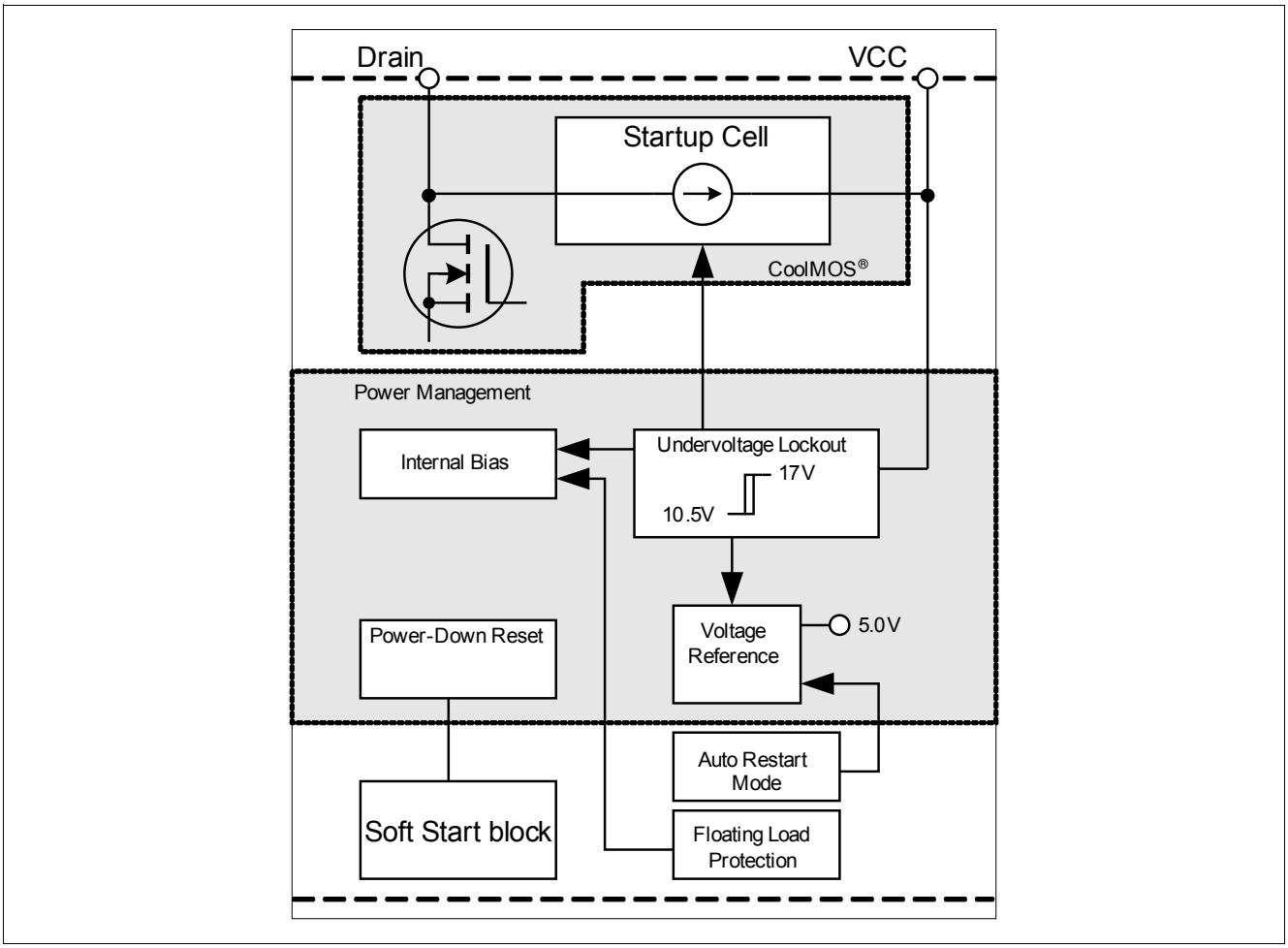

Figure 4 Power management of ICLS8023Z controllers

The undervoltage lockout function monitors the external supply voltage V_{VCC}. When the LED drive is connected to the main line, the internal startup cell is biased and starts to charge the external capacitor C_{VCC}, which is connected to the VCC pin. The VCC charge current that is provided by the startup cell from the drain pin is 0.9 mA. If V_{VCC} exceeds the on-threshold V_{CCon} (= 17 V), the bias circuit is switched on. Then the startup cell is switched off by the undervoltage lockout; therefore no power losses are present due to the connection of the startup cell to the drain voltage. An hysteresis loop is implemented to avoid uncontrolled ringing at switch-on. Switch-off of the controller can only take place after the active mode has been entered and V_{VCC} has fallen below 10.5 V.

The maximum current consumption before the controller is activated is about 200 µA.

If V_{VCC} falls below the off-threshold V_{CCoff} (= 10.5 V), the bias circuit is switched off and the soft start counter is reset. This ensures in every startup cycle that the soft start begins at zero.

The bias circuit is switched off if Auto Restart mode is entered. The current consumption is then reduced to 320 µA.

Once the malfunction condition is resolved, this block will then turn back on. The recovery from Auto Restart mode does not require disconnection of the LED drive from the AC line.

When Floating Load Protection (LFP) is entered, the internal bias is switched off most of the time but the voltage reference is kept alive in order to reduce the current consumption below 620 µA.

3.3 Improved Current Mode

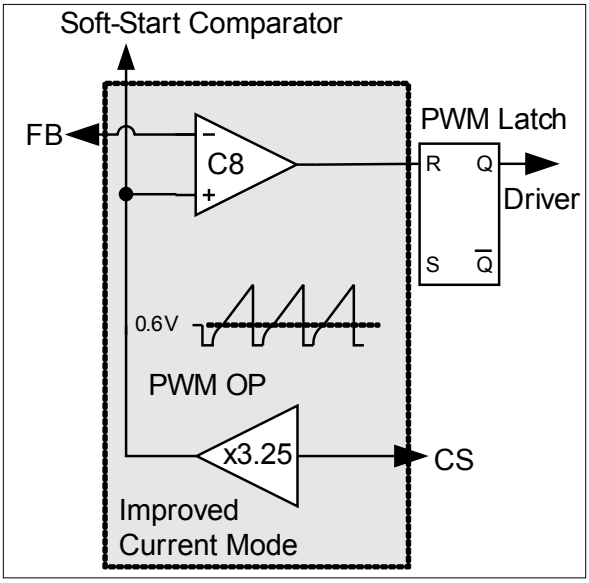

Figure 5 Current Mode

Current Mode means the duty cycle is controlled by the slope of the primary current. This is done by comparing the FB signal with the amplified current sense signal.

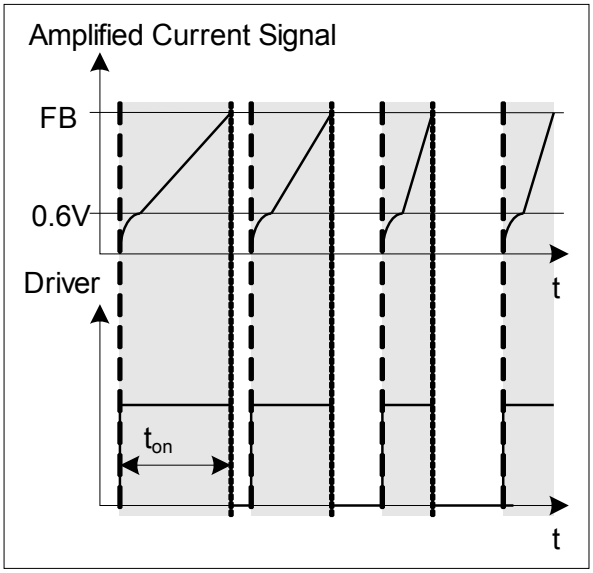

Figure 6 Pulse Width Modulation

If the amplified current sense signal exceeds the FB signal, the on-time t_{on} of the driver is finished by resetting the PWM latch (**Figure 6**).

The primary current is sensed by the external series resistor R_{Sense} inserted in the source of the integrated CoolMOS™. By means of current mode regulation, the secondary output voltage is insensitive to the line variations. The current waveform slope will change with the line variation, which controls the duty cycle.

The external R_{Sense} allows individual adjustment of the maximum source current of the integrated CoolMOS™.

To improve the current mode during light load conditions the amplified current ramp of the PWM-OP is superimposed on a voltage ramp, which is built by the switch T2, the voltage source V1 and a resistor R1 (see **Figure 7**). Every time the oscillator shuts down for maximum duty cycle limitation the switch T2 is closed by V_{OSC}. When the oscillator triggers the gate driver, T2 is opened so that the voltage ramp can start.

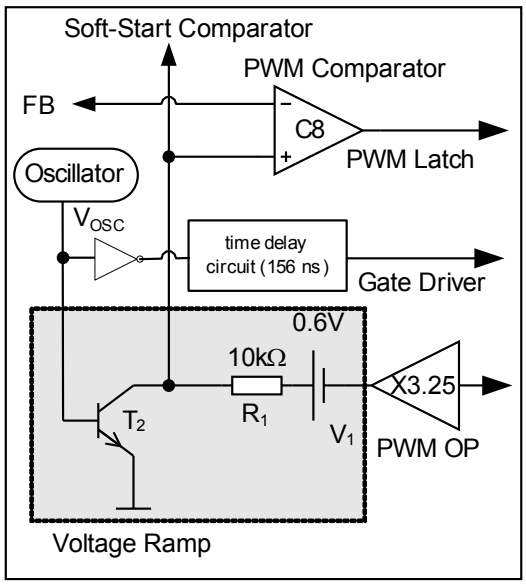

Figure 7 Improved Current Mode

In the case of light loads the amplified current ramp is too small to ensure stable regulation. In such cases the voltage ramp is a well-defined signal for the comparison with the FB signal. The duty cycle is then controlled by the slope of the voltage ramp.

By means of the time delay circuit which is triggered by the inverted V_{OSC} signal, the gate driver is switched off until it reaches approximately a 156 ns delay time (**Figure 8**). It allows the duty cycle to be reduced continuously to 0 % by decreasing V_{FB} below that threshold.

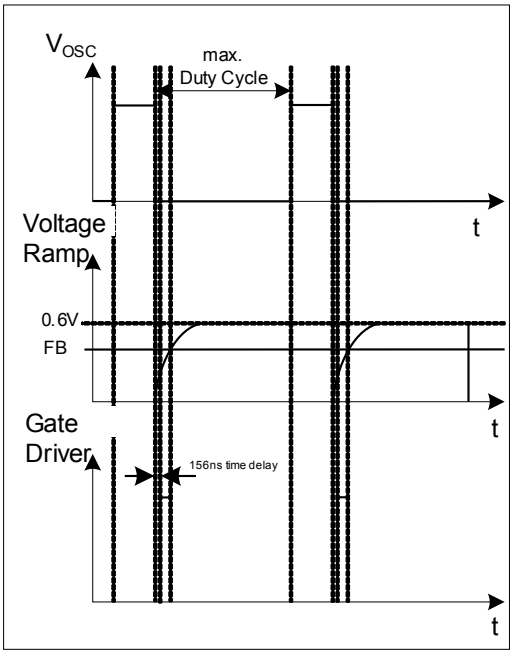

Figure 8 Light Load Conditions

3.3.1 PWM-OP

The input of the PWM-OP is applied over the internal leading edge blanking to the external sense resistor R_{Sense} connected to the CS pin. R_{Sense} converts the source current into a sense voltage. The sense voltage is amplified with a gain of 3.25 by the PWM-OP. The output of the PWM-OP is connected to the voltage source V1. The voltage ramp with the superimposed amplified current signal is fed into the positive inputs of the PWM comparator C8 and the soft start comparator (**Figure 9**).

3.3.2 PWM Comparator

The PWM comparator compares the sensed current signal of the integrated CoolMOS™ with the feedback signal V_{FB} (**Figure 9**). V_{FB} is created by an external optocoupler or external transistor in combination with the internal pull-up resistor R_{FB} and provides the load information of the feedback circuitry. When the amplified current signal of the integrated CoolMOS™ exceeds the signal V_{FB} the PWM comparator switches off the gate driver.

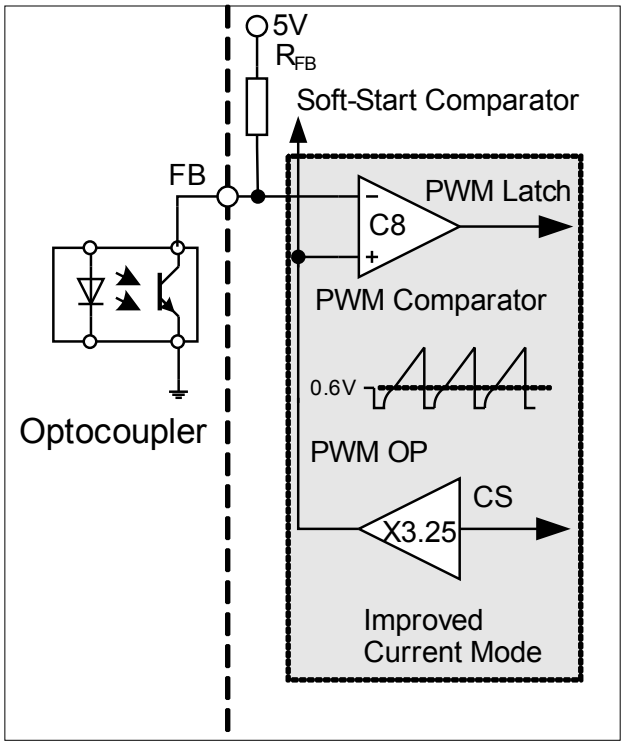

Figure 9 PWM Controlling

3.3.3 Startup Phase

In the startup phase, the IC provides a soft start period to control the primary current by means of a duty cycle limitation. The soft start function is a built-in function and it is controlled by an internal counter.

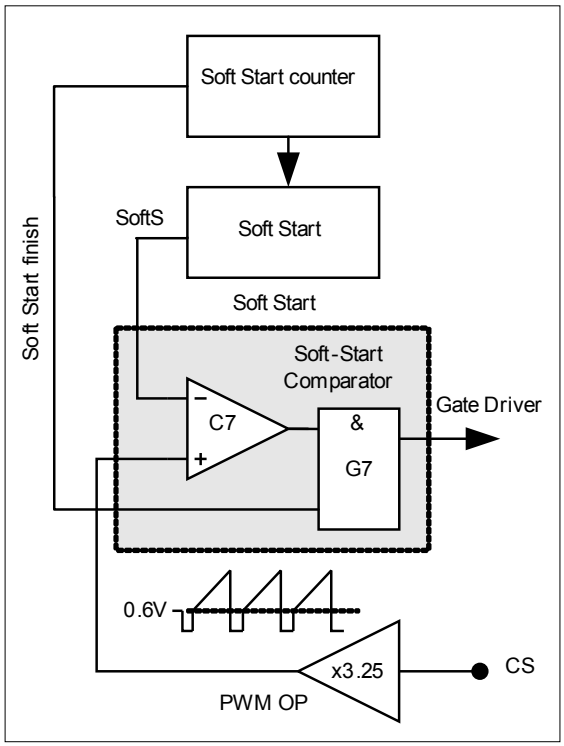

Figure 10 Soft Start

When the V_{CC} exceeds the on-threshold voltage, the IC starts the soft start mode (**Figure 11**).

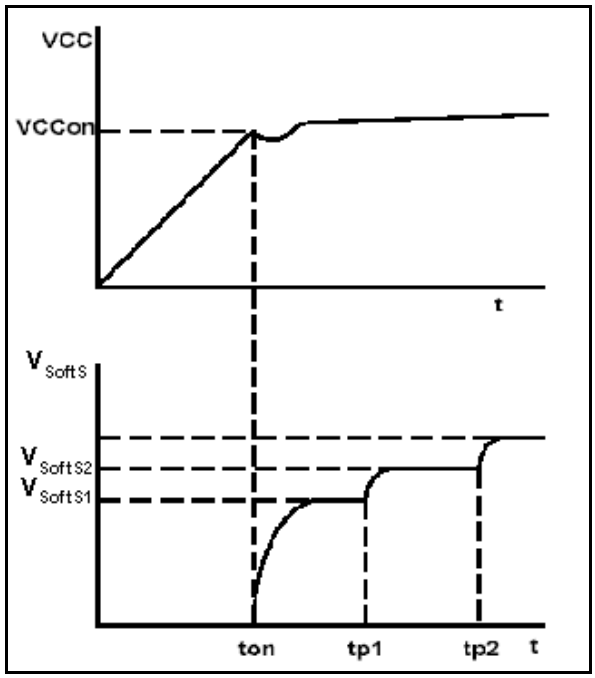

Figure 11 Soft Start Phase

The function is realized by an internal soft start resistor, a current sink and a counter. The amplitude of the current sink is controlled by the counter (**Figure 12**).

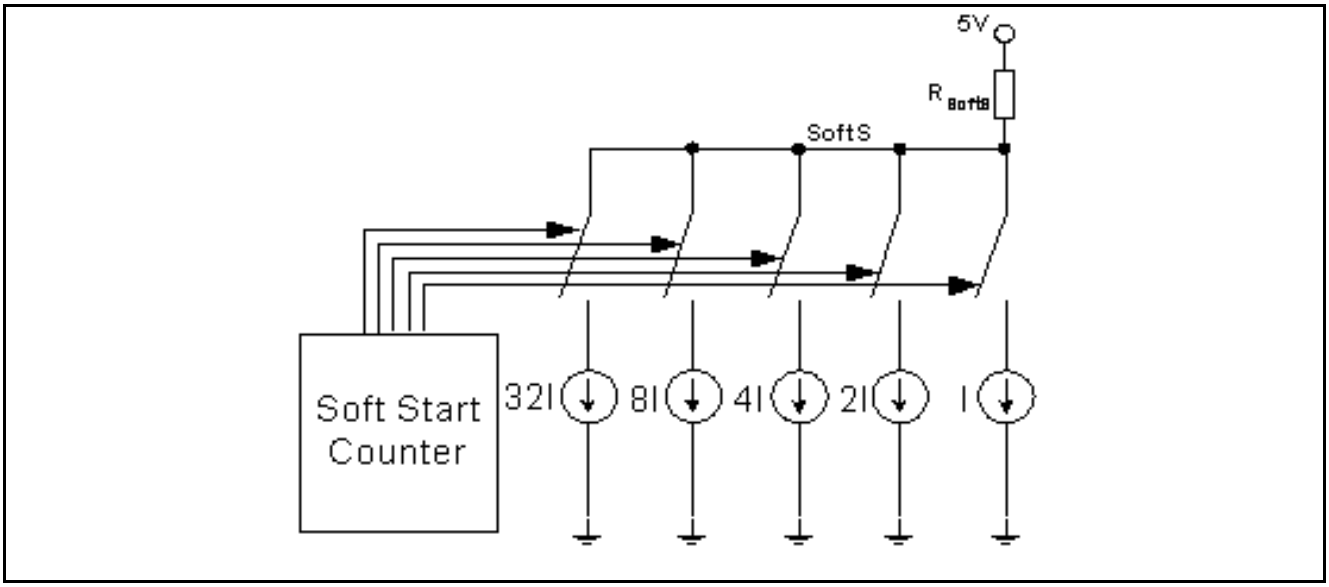

Figure 12 Soft Start Circuit

After the IC is switched on, the V_{SoftS} voltage is controlled such that the voltage is increased step-by-step (in 32 steps) with the increase of the counts. The soft start counter sends a signal to the current sink control every 300 μs so that the current sink decreases gradually and the duty ratio of the gate drive increases gradually. The soft start is finished in 10 ms ($t_{Soft\text{-}Start}$) after the IC is switched on. At the end of the soft start period, the current sink is switched off.

Within the soft start period, the duty cycle increases from zero to maximum gradually (see **Figure 13**).

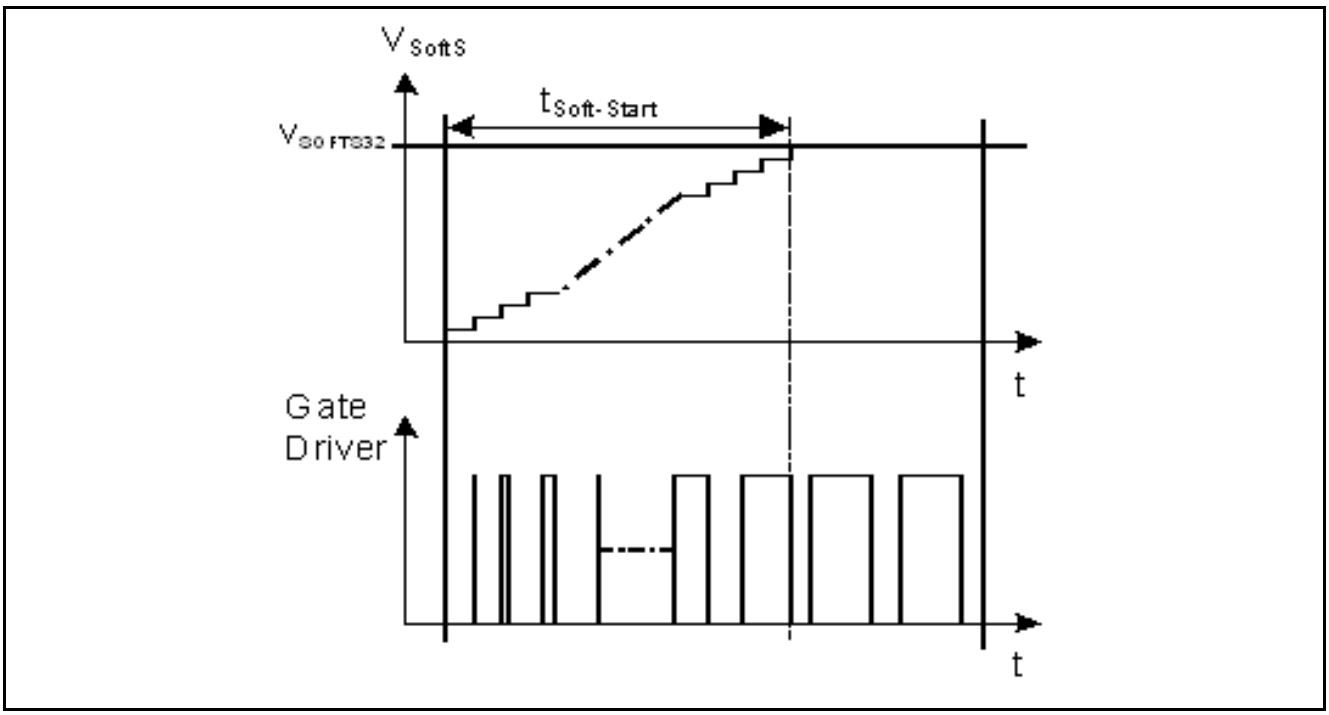

Figure 13 Gate Drive Signal in the Soft Start Phase

In addition to start-up, soft start is also activated at each restart attempt during auto restart.

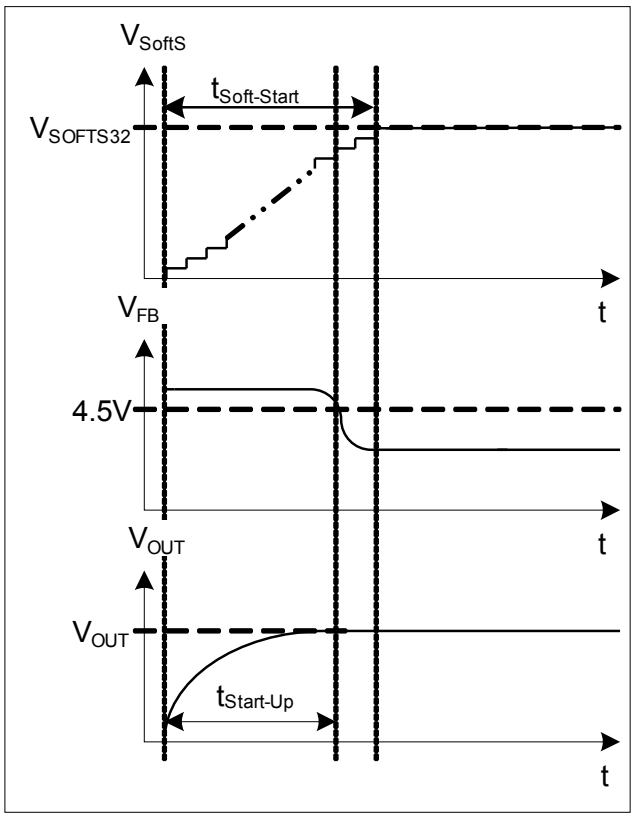

Figure 14 Start-Up Phase

The start-up time $t_{Start-Up}$ before the converter output voltage V_{OUT} is settled must be shorter than the soft start phase $t_{Soft-Start}$ (**Figure 14**). Soft start allows effective minimization of current and voltage stresses on the integrated CoolMOS™, the clamp circuit and the output rectifier and it helps to prevent saturation of the transformer during start-up.

3.4 PWM Section

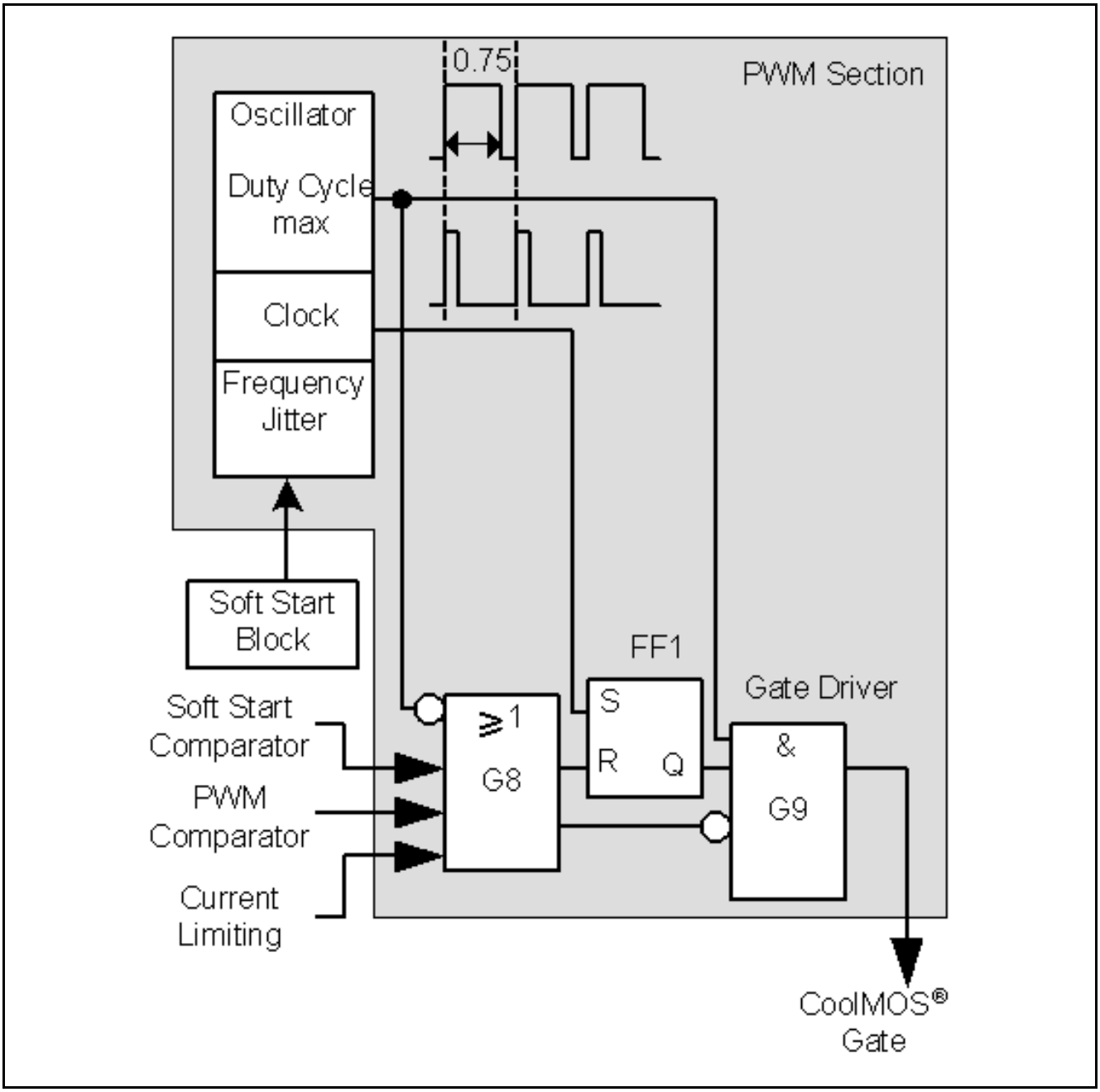

Figure 15 PWM Section Block

3.4.1 Oscillator

The oscillator generates a fixed frequency of 65 kHz with frequency jittering of ± 4 % (which is ± 2.6 kHz) at a jittering period of 4 ms.

A capacitor, a current source and current sink which determine the frequency are integrated. The charging and discharging current of the implemented oscillator capacitor are internally trimmed in order to achieve a very accurate switching frequency. The ratio of controlled charge to discharge current is adjusted to reach a maximum duty cycle limitation of D_{max} = 0.75.

Once the soft start period is over and when the IC goes into normal operating mode, the switching frequency of the clock is varied by the control signal from the soft start block. Then the switching frequency is varied in the range of 65 kHz ± 2.6 kHz at period of 4 ms.

3.4.2 PWM Latch FF1

The output of the oscillator block provides continuous pulses to the PWM latch, which turns on/off the integrated CoolMOS™. After the PWM latch is set, it is reset by the PWM comparator, the soft start comparator or the current limit comparator. When it is in reset mode, the output of the driver is shut down immediately.

3.4.3 Gate Driver

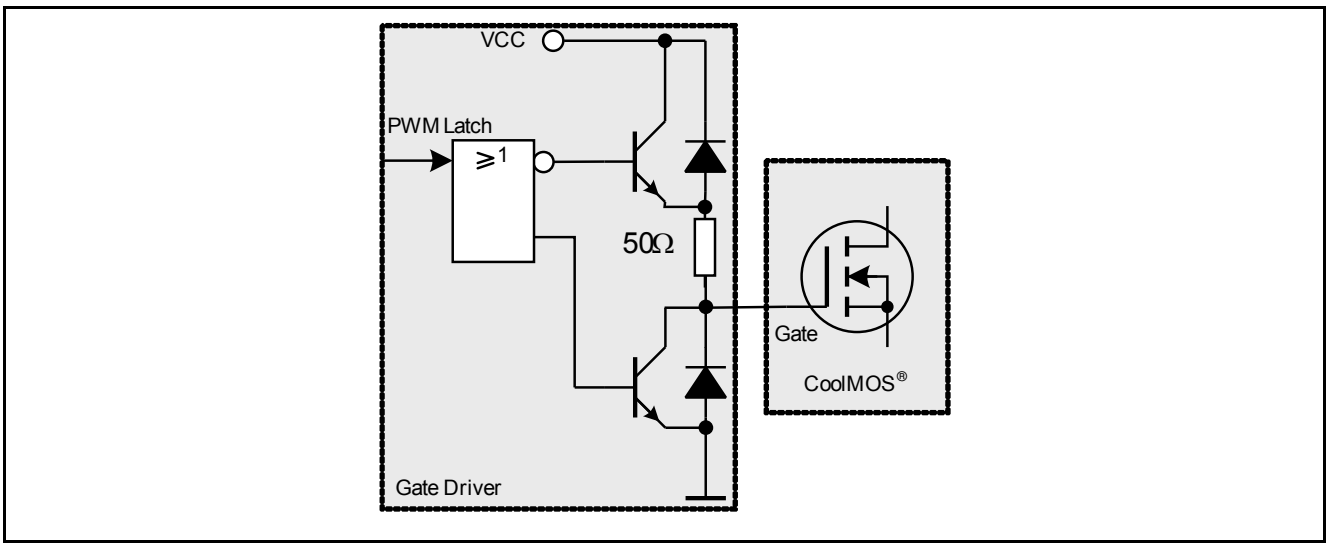

Figure 16 Gate Driver

The driver stage is optimized to minimize EMI and to provide high circuit efficiency. This is done by reducing the switch-on slope when exceeding the integrated CoolMOS™ threshold. This is achieved by a slope control of the rising edge at the driver's output (**Figure 17**) and adding a 50 Ω gate turn-on resistor (**Figure 16**). Thus the leading switch-on spike is minimized.

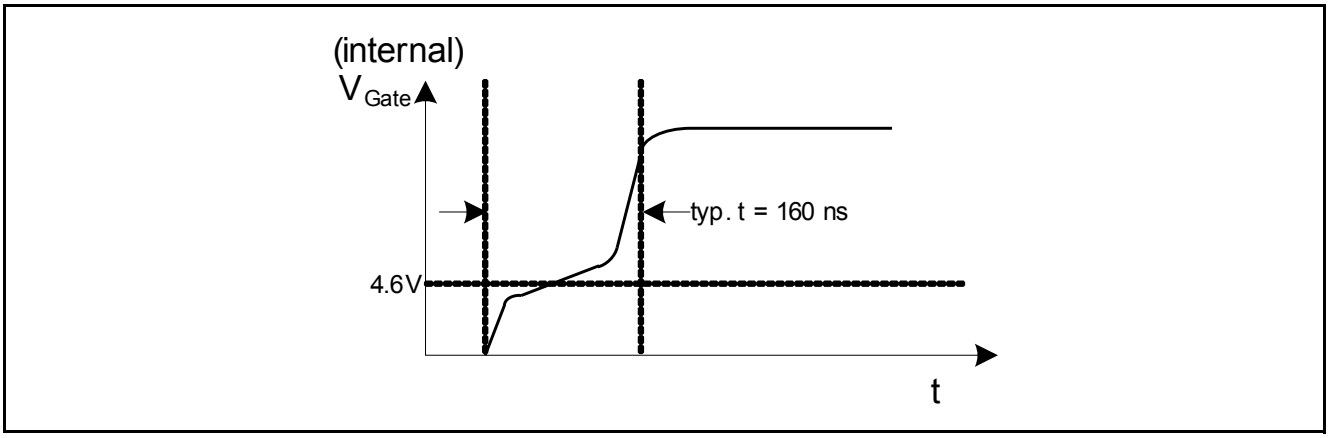

Figure 17 Gate Rising Slope

Furthermore the driver circuit is designed to eliminate cross conduction of the output stage.

During power-up, when V_{CC} is below the undervoltage lockout threshold V_{VCCoff}, the output of the gate driver is set to low in order to disable power transfer to the secondary side.

3.5 Current Limiting

A cycle-by-cycle peak current limiting operation is realized by the current limit comparator C10. The source current of the integrated CoolMOS™ is sensed via an external sense resistor R_{Sense}. By means of R_{Sense} the source current is transformed to a sense voltage V_{Sense}, which is fed to the pin CS. If the voltage V_{Sense} exceeds the internal threshold voltage V_{csth}, the comparator C10 immediately turns off the gate drive by resetting the PWM latch FF1.

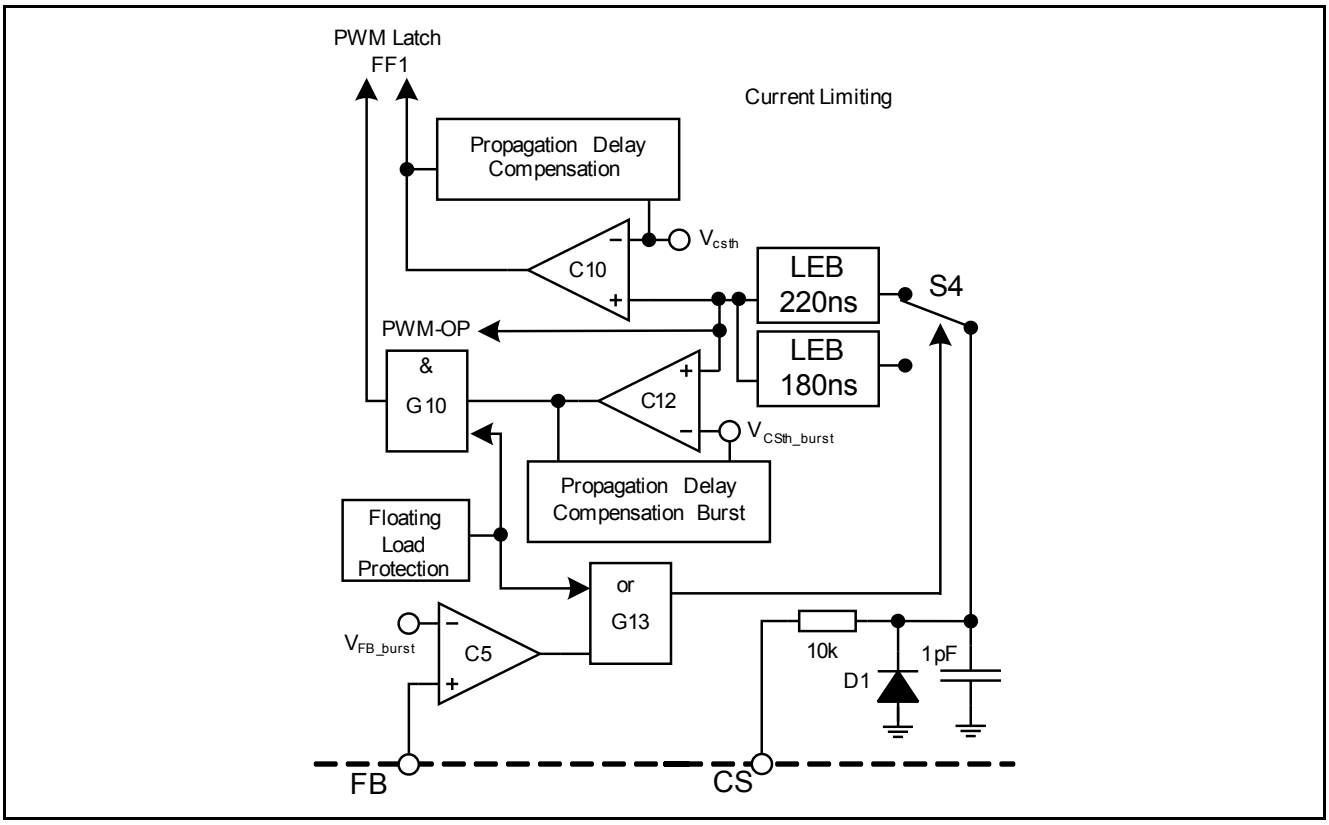

Figure 18 Current Limiting Block

Propagation delay compensation is added to support the immediate shutdown of the integrated CoolMOS™ with very short propagation delay. Thus the influence of the AC input voltage on the maximum output power can be reduced to a minimu. This compensation applies to both the peak load and burst mode.

In order to prevent the current limit from distortions caused by leading edge spikes, Leading Edge Blanking (LEB) is integrated into the current sense path for the comparators C10, C12 and the PWM-OP.

The output of comparator C12 is activated by the gate G10 if the FLP is entered. When it is activated, the current limiting is reduced to V_{csth_FLP}. This voltage level determines the maximum power level in Floating Load Protection mode.

3.5.1 Leading Edge Blanking

Whenever the integrated CoolMOS™ is switched on, a leading edge spike is generated due to the primary-side capacitances and reverse recovery time of the secondary-side rectifier. This spike can cause the gate drive to switch off unintentionally. In order to avoid premature termination of the switching pulse, this spike is blanked out with a time constant of t_{LEB} = 220 ns for normal load and t_{LEB} = 180 ns for FLP mode.

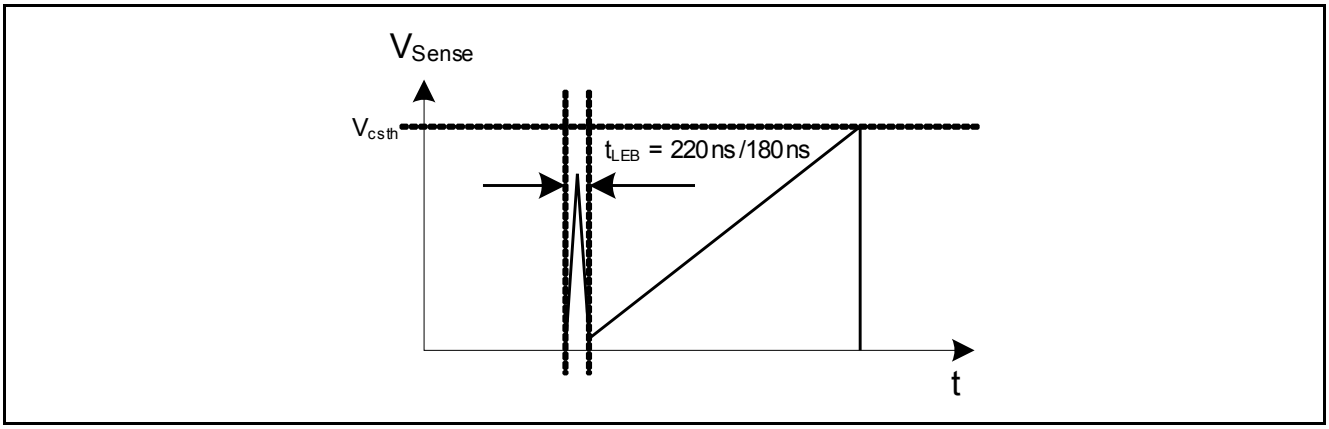

Figure 19 Leading Edge Blanking

3.5.2 Propagation Delay Compensation (patented)

In the case of overcurrent detection, there is always propagation delay to switch off the integrated CoolMOS™. An overshoot of the peak current I_{peak} is induced to the delay, which depends on the ratio of dI/dt of the peak current (**Figure 20**).

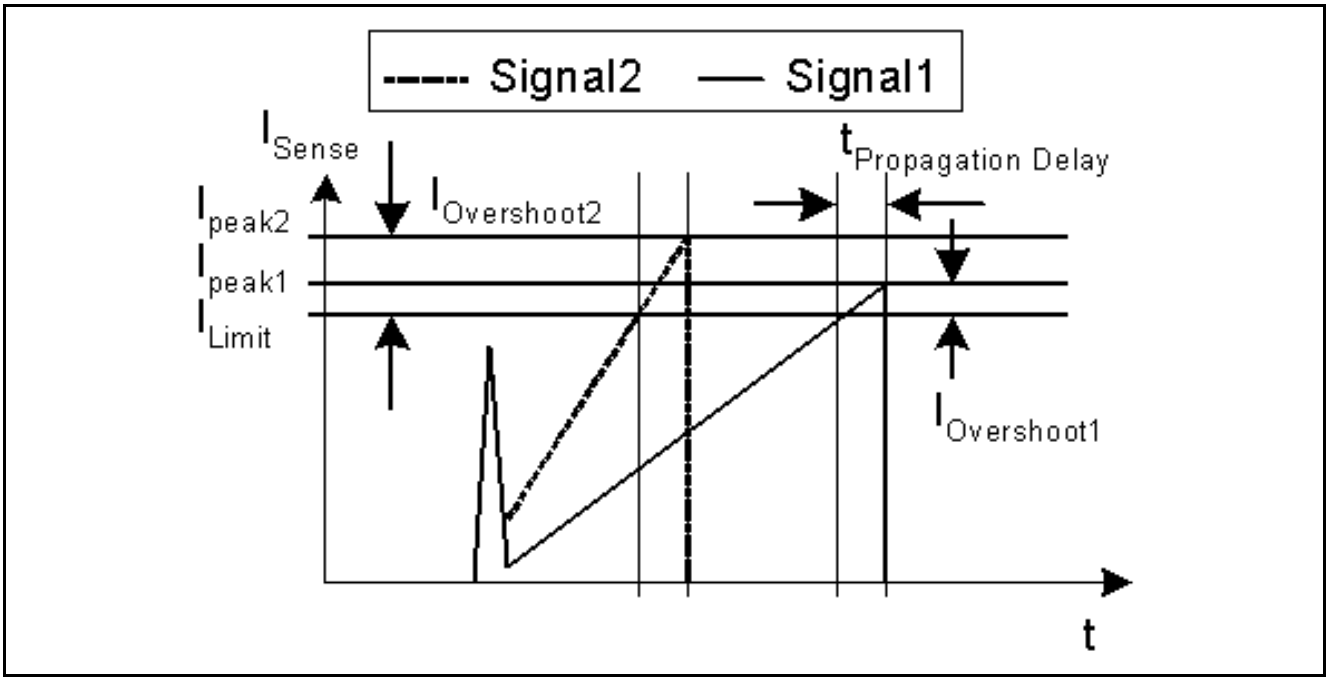

Figure 20 Current Limiting

The overshoot of Signal2 is larger than of Signal1 due to the steeper rising waveform. This change in the slope depends on the AC input voltage. Propagation Delay Compensation is integrated to reduce the overshoot due to dI/dt of the rising primary current. Thus the propagation delay time between exceeding the current sense threshold V_{csth} and the switching-off of the integrated CoolMOS™ is compensated over temperature within a wide input range. Current limiting is then very accurate.

For example, I_{peak} = 0.5 A with R_{Sense} = 2. The current sense threshold is set to a static voltage level V_{csth} = 1 V without Propagation Delay Compensation. A current ramp of dI/dt = 0.4 A/µs, or dV_{Sense}/dt = 0.8 V/µs, and a propagation delay time of $t_{Propagation\ Delay}$ = 180 ns leads to an I_{peak} overshoot of 14.4 %. With the propagation delay compensation, the overshoot is only around 2 % (**Figure 21**).

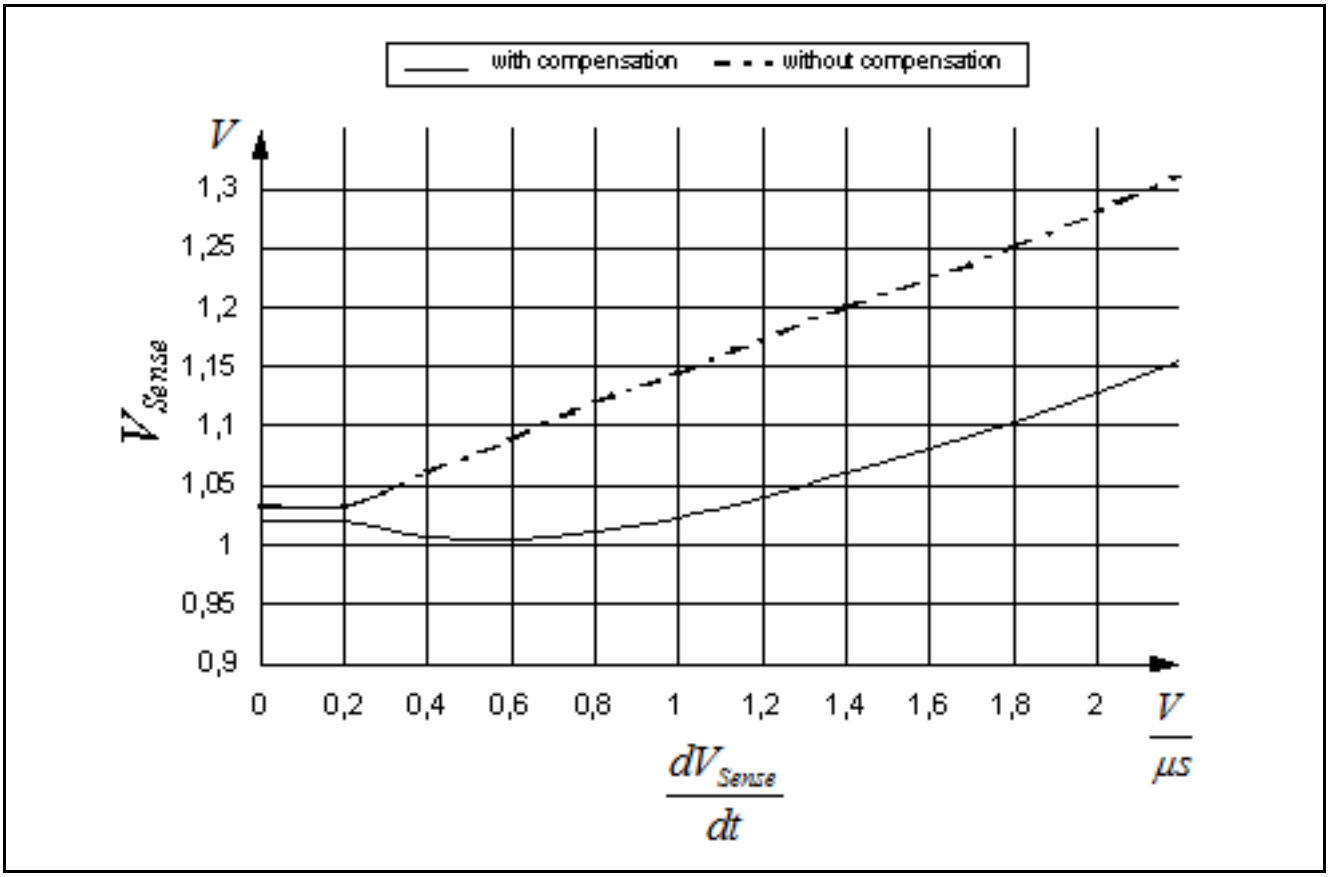

Figure 21 Overcurrent Shutdown

The Propagation Delay Compensation is realized by means of a dynamic threshold voltage V_{csth} (**Figure 22**). In case of a steeper slope the switch-off of the driver is earlier to compensate the delay.

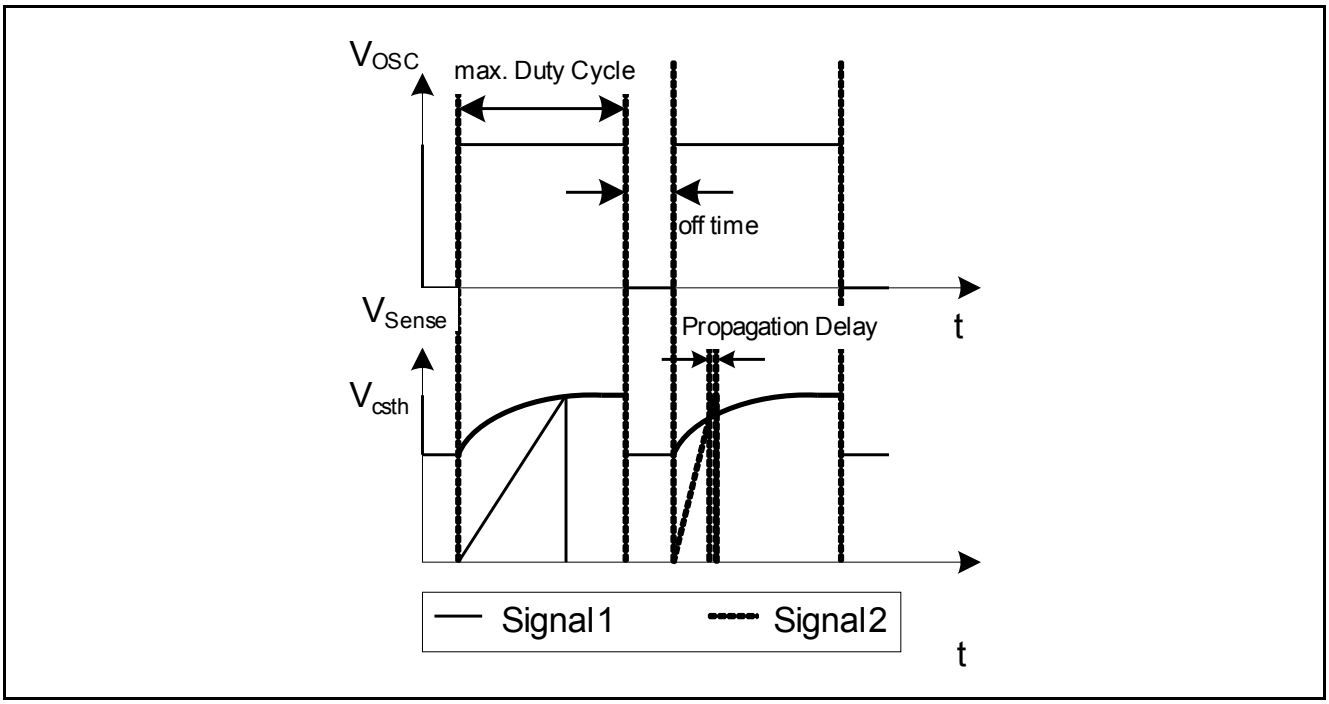

Figure 22 Dynamic Voltage Threshold V_{csth}

Similarly, the same concept of propagation delay compensation is also implemented in FLP mode with a reduced level, V_{csth_FLP} (**Figure 18**). With this implementation, the entry and exit FLP mode power can be very close between low line and high line input voltage.

3.6 Control Unit

The Control Unit contains the functions for Floating Load Protection (FLP) mode and Auto Restart mode. The FLP mode and the Auto Restart mode both have 20 ms internal blanking times. For the overload Auto Restart mode, the 20 ms blanking time can be further extended by adding an external capacitor at the BA pin. With the blanking time, the IC avoids entering into those two modes accidentally. This buffer time is very useful for the application, which works in short durations of peak power occasionally.

3.6.1 Basic and Extendable Blanking Mode

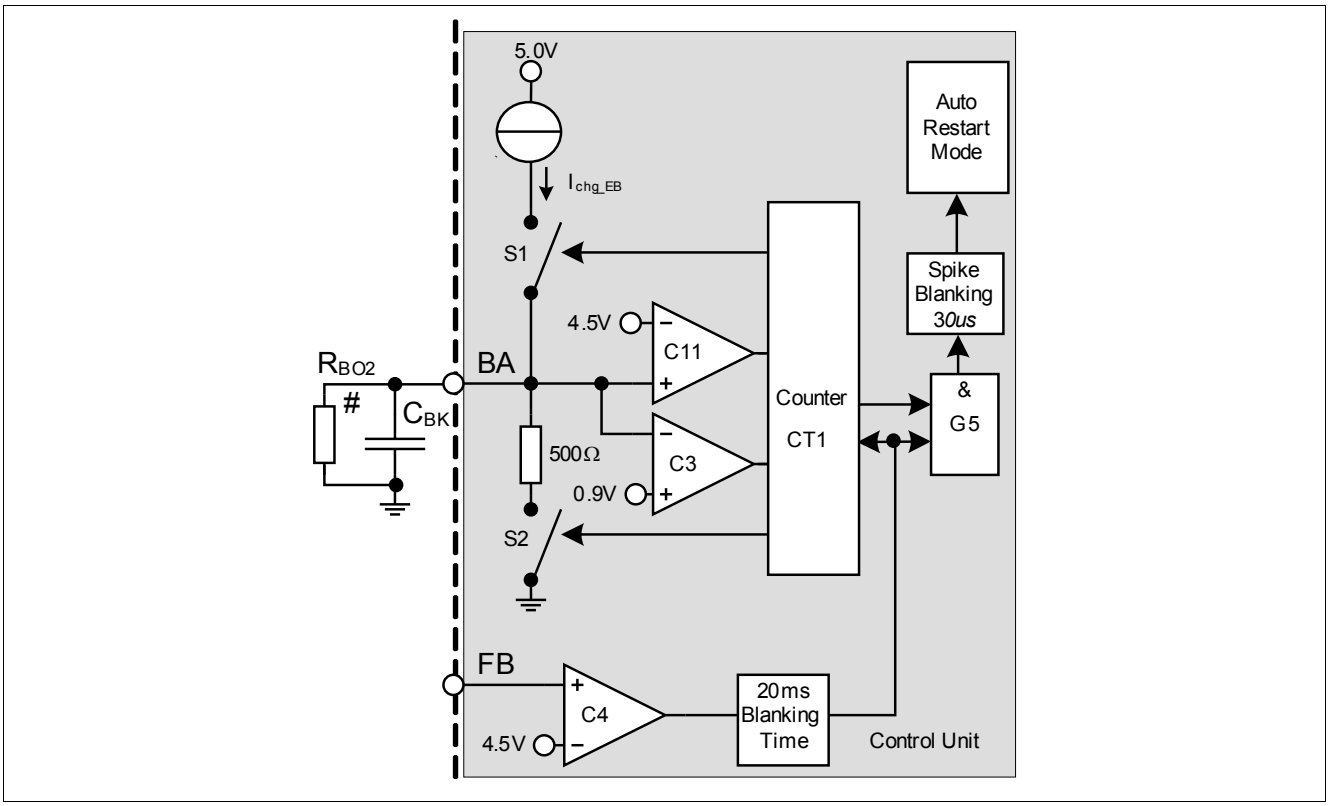

Figure 23 Basic and Extendable Blanking Mode

There are 2 kinds of blanking mode: basic mode and the extendable mode. The basic mode is a built-in 20 ms blanking time while the extendable mode can extend this blanking time by connecting an external capacitor to the BA pin. For the extendable mode, the gate G5 remains blocked even though the 20 ms blanking time is reached. After reaching the 20 ms blanking time the counter is activated and the switch S1 is turned on to charge the voltage of the BA pin by the constant current source, I_{chg_EB}. When the voltage of the BA pin hits 4.5 V, which is sensed by the comparator C11, the counter will increase the counter by 1. Then it switches off the switch S1 and turns on the switch S2. The voltage at the BA pin will be discharged through a 500 Ω resistor. When the voltage drops to 0.9 V, which is sensed by the comparator C3, the switch S2 will be turned off and the switch S1 will be turned on. Then the constant current I_{chg_EB} will charge the C_{BK} capacitor again. When the voltage at BA hits 4.5 V, which is sensed by comparator C11, the counter will increase the count to 2. The process repeats until it reaches a total count of 256 (**Figure 23**). Then the counter will release a high output signal. When the AND gate G5 detects both