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High Performance 6-Axis MEMS MotionTracking™ Device in 2.5x3x0.91mm Package

GENERAL DESCRIPTION

The ICM-20600 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, 3-axis accelerometer, in a small 2.5 mm x 3 mm x 0.91 mm (14-pin LGA) package.

- High performance specs
 - Gyroscope sensitivity error: $\pm 1\%$
 - Gyroscope noise: ± 4 mdps/ $\sqrt{\text{Hz}}$
 - Accelerometer noise: $100 \mu\text{g}/\sqrt{\text{Hz}}$
- Includes 1 KB FIFO to reduce traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode
- EIS FSYNC support

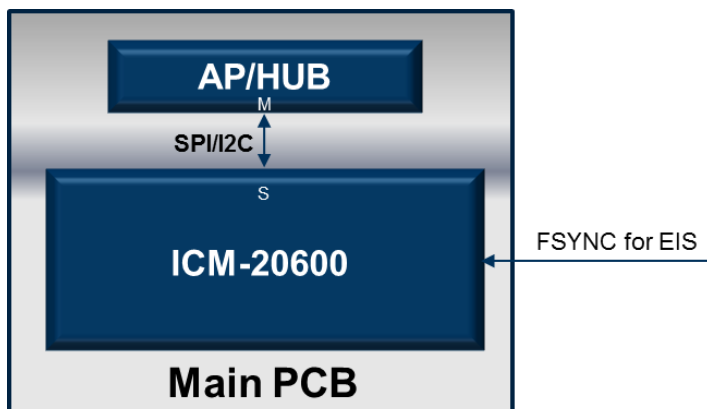
ICM-20600 includes on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features an operating voltage range down to 1.71V. Communication ports include I²C and high speed SPI at 10 MHz.

ORDERING INFORMATION

PART	TEMP RANGE	PACKAGE
ICM-20600†	-40°C to +85°C	14-Pin LGA

†Denotes RoHS and Green-Compliant Package

BLOCK DIAGRAM



APPLICATIONS

- Smartphones and Tablets
- Wearable Sensors
- IoT Applications
- Motion-based game controllers
- 3D remote controls for Internet connected DTVs and set top boxes, 3D mice

FEATURES

- 3-Axis Gyroscope with Programmable FSR of ± 250 dps, ± 500 dps, ± 1000 dps, and ± 2000 dps
- 3-Axis Accelerometer with Programmable FSR of $\pm 2g$, $\pm 4g$, $\pm 8g$, and $\pm 16g$
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- 1 KB FIFO buffer enables the applications processor to read the data in bursts
- On-Chip 16-bit ADCs and Programmable Filters
- Host interface: 10 MHz SPI or 400 kHz Fast Mode I²C
- Digital-output temperature sensor
- VDD operating range of 1.71 to 3.45V
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

TYPICAL OPERATING CIRCUIT

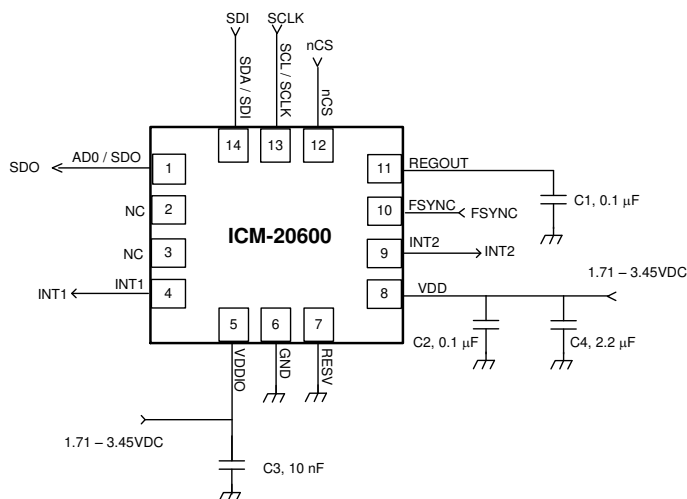


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1 INTRODUCTION

1.1 PURPOSE AND SCOPE

This document is a product specification, providing a description, specifications, and design related information on the ICM-20600™ MotionTracking device. The device is housed in a small 2.5x3x0.91mm 14-pin LGA package.

1.2 PRODUCT OVERVIEW

The ICM-20600 is a 6-axis MotionTracking device that combines a 3-axis gyroscope, and a 3-axis accelerometer in a small 2.5x3x0.91mm (14-pin LGA) package. It also features a 1K-byte FIFO that can lower the traffic on the serial bus interface, and reduce power consumption by allowing the system processor to burst read sensor data and then go into a low-power mode. ICM-20600, with its 6-axis integration, enables manufacturers to eliminate the costly and complex selection, qualification, and system level integration of discrete devices, guaranteeing optimal motion performance for consumers.

The gyroscope has a programmable full-scale range of ± 250 , ± 500 , ± 1000 , and ± 2000 degrees/sec. The accelerometer has a user-programmable accelerometer full-scale range of $\pm 2g$, $\pm 4g$, $\pm 8g$, and $\pm 16g$. Factory-calibrated initial sensitivity of both sensors reduces production-line calibration requirements.

Other industry-leading features include on-chip 16-bit ADCs, programmable digital filters, an embedded temperature sensor, and programmable interrupts. The device features I²C and SPI serial interfaces, a VDD operating range of 1.71 to 3.45V, and a separate digital IO supply, VDDIO from 1.71V to 3.45V.

Communication with all registers of the device is performed using either I²C at 400kHz or SPI at 10MHz.

By leveraging its patented and volume-proven CMOS-MEMS fabrication platform, which integrates MEMS wafers with companion CMOS electronics through wafer-level bonding, InvenSense has driven the package size down to a footprint and thickness of 2.5x3x0.91mm (14-pin LGA), to provide a very small yet high performance low cost package. The device provides high robustness by supporting 20,000g shock reliability.

1.3 APPLICATIONS

- Smartphones and Tablets
- Wearable Sensors

2 FEATURES

2.1 GYROSCOPE FEATURES

The triple-axis MEMS gyroscope in the ICM-20600 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis angular rate sensors (gyroscopes) with a user-programmable full-scale range of ± 250 , ± 500 , ± 1000 , and $\pm 2000^\circ/\text{sec}$ and integrated 16-bit ADCs
- Digitally-programmable low-pass filter
- Low-power gyroscope operation
- Factory calibrated sensitivity scale factor
- Self-test

2.2 ACCELEROMETER FEATURES

The triple-axis MEMS accelerometer in ICM-20600 includes a wide range of features:

- Digital-output X-, Y-, and Z-axis accelerometer with a programmable full scale range of $\pm 2g$, $\pm 4g$, $\pm 8g$ and $\pm 16g$ and integrated 16-bit ADCs
- User-programmable interrupts
- Wake-on-motion interrupt for low power operation of applications processor
- Self-test

2.3 ADDITIONAL FEATURES

The ICM-20600 includes the following additional features:

- Smallest and thinnest LGA package for portable devices: 2.5 mm x 3 mm x 0.91 mm (14-pin LGA)
- Minimal cross-axis sensitivity between the accelerometer and gyroscope axes
- 1 KB FIFO buffer enables the applications processor to read the data in bursts
- Digital-output temperature sensor
- User-programmable digital filters for gyroscope, accelerometer, and temp sensor
- 20,000 g shock tolerant
- 400 kHz Fast Mode I²C for communicating with all registers
- 10 MHz SPI serial interface for communicating with all registers
- MEMS structure hermetically sealed and bonded at wafer level
- RoHS and Green compliant

3 ELECTRICAL CHARACTERISTICS

3.1 GYROSCOPE SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
GYROSCOPE SENSITIVITY						
Full-Scale Range	FS_SEL=0		±250		dps	3
	FS_SEL=1		±500		dps	3
	FS_SEL=2		±1000		dps	3
	FS_SEL=3		±2000		dps	3
Gyroscope ADC Word Length			16		bits	3
Sensitivity Scale Factor	FS_SEL=0		131		LSB/(dps)	3
	FS_SEL=1		65.5		LSB/(dps)	3
	FS_SEL=2		32.8		LSB/(dps)	3
	FS_SEL=3		16.4		LSB/(dps)	3
Sensitivity Scale Factor Initial Tolerance	25°C		±1		%	1
Sensitivity Scale Factor Variation Over Temperature	-40°C to +85°C		±2		%	1
Nonlinearity	Best fit straight line; 25°C		±0.1		%	1
Cross-Axis Sensitivity			±1		%	1
ZERO-RATE OUTPUT (ZRO)						
Initial ZRO Tolerance	25°C		±1		dps	1
ZRO Variation vs. Temperature	-40°C to +85°C		±0.01		dps/°C	1
GYROSCOPE NOISE PERFORMANCE (FS_SEL=0)						
Rate Noise Spectral Density	@10 Hz		0.004		dps/VHz	1, 4
Total RMS Noise	Bandwidth = 100 Hz		0.04		kHz	1, 4
Gyroscope Mechanical Frequencies		25	27	29	Hz	2
Low Pass Filter Response	Programmable Range	5		250	ms	3
Gyroscope Start-Up Time	Time from gyro enable to gyro drive ready		35	100	Hz	1
Output Data Rate	Low-Noise mode	3.91		8000	Hz	3
	Low Power Mode	3.91		333.33	Hz	3

Table 1. Gyroscope Specifications

Notes:

1. Target spec. Subject to update.
2. Tested in production.
3. Guaranteed by design.
4. Noise specifications shown are for low-noise mode.

3.2 ACCELEROMETER SPECIFICATIONS

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
ACCELEROMETER SENSITIVITY						
Full-Scale Range	AFS_SEL=0		±2		g	2
	AFS_SEL=1		±4		g	2
	AFS_SEL=2		±8		g	2
	AFS_SEL=3		±16		g	2
ADC Word Length	Output in two's complement format		16		bits	2
Sensitivity Scale Factor	AFS_SEL=0		16,384		LSB/g	2
	AFS_SEL=1		8,192		LSB/g	2
	AFS_SEL=2		4,096		LSB/g	2
	AFS_SEL=3		2,048		LSB/g	2
Sensitivity Scale Factor Initial Tolerance	Component-level		±1		%	1
Sensitivity Change vs. Temperature	-40°C to +85°C		±1.5		%	1
Nonlinearity	Best Fit Straight Line		±0.3		%	1
Cross-Axis Sensitivity			±1		%	1
ZERO-G OUTPUT						
Initial Tolerance	Component-level, all axes		±25			1
	Board-level, all axes		±40		mg	1
Zero-G Level Change vs. Temperature	X & Y-axis (-40°C to +85°C)		±0.5		mg/°C	1
	Z-axis (-40°C to +85°C)		±1		mg/°C	1
NOISE PERFORMANCE						
Power Spectral Density	@ 10 Hz		100		µg/√Hz	1, 3
RMS Noise	Bandwidth = 100 Hz		1.0		mg-rms	1, 3
Low-Pass Filter Response	Programmable Range	5		218	Hz	2
Accelerometer Startup Time	From sleep mode to valid data		10	20	ms	2
Output Data Rate	Low Noise mode	3.91		4000	Hz	2
	Low Power Mode	3.91		500	Hz	

Table 2. Accelerometer Specifications

Notes:

1. Target spec. Subject to update.
2. Guaranteed by design.
3. Noise specifications shown are for low-noise mode.

3.3 ELECTRICAL SPECIFICATIONS

D.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLY VOLTAGES						
VDD		1.71	1.8	3.45	V	1
VDDIO		1.71	1.8	3.45	V	1
SUPPLY CURRENTS & BOOT TIME						
Low-Noise Mode	6-Axis Gyroscope + Accelerometer		2.79		mA	1
	3-Axis Accelerometer		321		μA	1
	3-Axis Gyroscope		2.55		mA	1
Accelerometer Low -Power Mode (Gyroscope disabled)	100 Hz ODR, 1x averaging		40		μA	1
Gyroscope Low-Power Mode (Accelerometer disabled)	100 Hz ODR, 1x averaging		1.08		mA	1
6-Axis Low-Power Mode (Gyroscope Low-Power Mode; Accelerometer Low-Noise Mode)	100 Hz ODR, 1x averaging		1.33		mA	1
Full-Chip Sleep Mode	At 25°C		6		μA	1
TEMPERATURE RANGE						
Specified Temperature Range	Performance parameters are not applicable beyond Specified Temperature Range	-40		85	°C	1

Table 3. D.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.

A.C. Electrical Characteristics

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SUPPLIES						
Supply Ramp Time	Monotonic ramp. Ramp rate is 10% to 90% of the final value	0.01		3	ms	1
Power Supply Noise				10	mV peak-peak	1
Power Supply Sequencing Requirement Between VDD and VDDIO		None				2
TEMPERATURE SENSOR						
Operating Range	Ambient	-40		85	°C	1
25°C Output			0		LSB	3
ADC Resolution			16		bits	2
ODR	Without Filter		8000		Hz	2
	With Filter	3.91		1000	Hz	2
Room Temperature Offset	25°C	-15		15	°C	3
Stabilization Time				14000	µs	2
Sensitivity	Untrimmed		326.8		LSB/°C	1
Sensitivity Error		-2.5		+2.5	%	1
POWER-ON RESET						
Start-up time for register read/write	From power-up			2	ms	1
I²C ADDRESS	AD0 = 0		1101000			
	AD0 = 1		1101001			
DIGITAL INPUTS (FSYNC, AD0, SCLK, SDI, CS)						
V _{IH} , High Level Input Voltage		0.7*VDDIO			V	1
V _{IL} , Low Level Input Voltage				0.3*VDDIO	V	
C _I , Input Capacitance			< 10		pF	
DIGITAL OUTPUT (SDO, INT)						
V _{OH} , High Level Output Voltage	R _{LOAD} =1 MΩ;	0.9*VDDIO			V	1
V _{OL} , LOW-Level Output Voltage	R _{LOAD} =1 MΩ;			0.1*VDDIO	V	
V _{OL,INT} , INT Low-Level Output Voltage	OPEN=1, 0.3 mA sink Current			0.1	V	
Output Leakage Current	OPEN=1		100		nA	
t _{INT} , INT Pulse Width	LATCH_INT_EN=0		50		µs	
I²C I/O (SCL, SDA)						
V _{IL} , LOW Level Input Voltage		-0.5V		0.3*VDDIO	V	1
V _{IH} , HIGH-Level Input Voltage		0.7*VDDIO		VDDIO + 0.5V	V	
V _{hys} , Hysteresis			0.1*VDDIO		V	
V _{OL} , LOW-Level Output Voltage	3 mA sink current	0		0.4	V	
I _{OL} , LOW-Level Output Current	V _{OL} =0.4V		3		mA	
	V _{OL} =0.6V		6		mA	
Output Leakage Current			100		nA	
t _{of} , Output Fall Time from V _{IHmax} to V _{ILmax}	C _b bus capacitance in pf	20+0.1C _b		300	ns	
INTERNAL CLOCK SOURCE						
Sample Rate	FCHOICE_B=1,2,3; SMPLRT_DIV=0		32		kHz	2

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
	FCHOICE_B=0; DLPFCFG=0 or 7 SMPLRT_DIV=0		8		kHz	2
	FCHOICE_B=0; DLPFCFG=1,2,3,4,5,6; SMPLRT_DIV=0		1		kHz	2
Clock Frequency Initial Tolerance	CLK_SEL=0, 6 or gyro inactive; 25°C	-3		+3	%	1
	CLK_SEL=1,2,3,4,5 and gyro active; 25°C	-1		+1	%	1
Frequency Variation over Temperature	CLK_SEL=0,6 or gyro inactive. (-40°C to +85°C)			±2	%	1
	CLK_SEL=1,2,3,4,5 and gyro active			±2	%	1

Table 4. A.C. Electrical Characteristics

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. Guaranteed by design.
3. Production tested.

Other Electrical Specifications

Typical Operating Circuit of section **Error! Reference source not found.**, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
SERIAL INTERFACE						
SPI Operating Frequency, All Registers Read/Write	Low Speed Characterization	100	100 ±10%		kHz	1,3
	High Speed Characterization	0.2	1	10	MHz	1, 2, 3
SPI Modes			0 and 3			
I ² C Operating Frequency	All registers, Fast-mode	100		400	kHz	1
	All registers, Standard-mode			100	kHz	1

Table 5. Other Electrical Specifications

Notes:

1. Derived from validation or characterization of parts, not guaranteed in production.
2. SPI clock duty cycle between 45% and 55% should be used for 10 MHz operation.
3. Minimum SPI/I²C clock rate is dependent on ODR. If ODR is below 4 kHz, minimum clock rate is 100 kHz. If ODR is greater than 4 kHz, minimum clock rate is 200 kHz.

3.4 I²C TIMING CHARACTERIZATION

Typical Operating Circuit of section 4.2, VDD = 1.8V, VDDIO = 1.8V, T_A=25°C, unless otherwise noted.

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
I²C TIMING		I²C FAST-MODE				
f _{SCL} , SCL Clock Frequency		100		400	kHz	1
t _{HD,STA} , (Repeated) START Condition Hold Time		0.6			μs	1
t _{LOW} , SCL Low Period		1.3			μs	1
t _{HIGH} , SCL High Period		0.6			μs	1
t _{SU,STA} , Repeated START Condition Setup Time		0.6			μs	1
t _{HD,DAT} , SDA Data Hold Time		0			μs	1
t _{SU,DAT} , SDA Data Setup Time		100			ns	1
t _r , SDA and SCL Rise Time	C _b bus cap. from 10 to 400 pF	20+0.1C _b		300	ns	1
t _f , SDA and SCL Fall Time	C _b bus cap. from 10 to 400 pF	20+0.1C _b		300	ns	1
t _{SU,STO} , STOP Condition Setup Time		0.6			μs	1
t _{BUF} , Bus Free Time Between STOP and START Condition		1.3			μs	1
C _b , Capacitive Load for each Bus Line			< 400		pF	1
t _{VD,DAT} , Data Valid Time				0.9	μs	1
t _{VD,ACK} , Data Valid Acknowledge Time				0.9	μs	1

Table 6. I²C Timing Characteristics

Notes:

- Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets

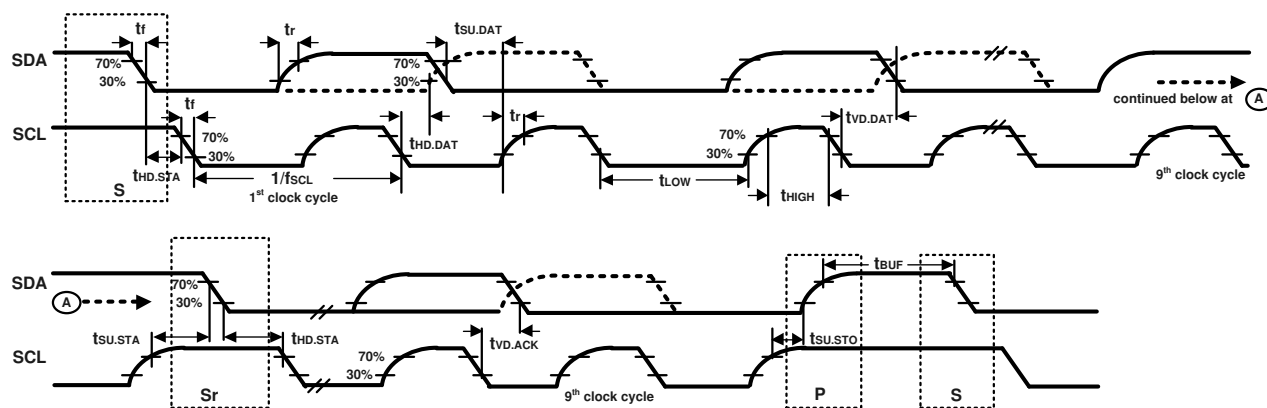


Figure 1. I²C Bus Timing Diagram

3.5 SPI TIMING CHARACTERIZATION

Typical Operating Circuit of section **Error! Reference source not found.**, VDD = 1.8V, VDDIO = 1.8V, TA=25°C, unless otherwise noted.

Parameters	Conditions	Min	Typical	Max	Units	Notes
SPI TIMING						
f _{SPC} , SPC Clock Frequency				10	MHz	1
t _{LOW} , SPC Low Period		45			ns	1
t _{HIGH} , SPC High Period		45			ns	1
t _{SU,CS} , CS Setup Time		2			ns	1
t _{HD,CS} , CS Hold Time		63			ns	1
t _{SU,SDI} , SDI Setup Time		3			ns	1
t _{HD,SDI} , SDI Hold Time		7			ns	1
t _{VD,SDO} , SDO Valid Time	C _{load} = 20 pF			40	ns	1
t _{DIS,SDO} , SDO Output Disable Time				20	ns	1

Table 7. SPI Timing Characteristics (7 MHz)

Notes:

1. Based on characterization of 5 parts over temperature and voltage as mounted on evaluation board or in sockets
2. Based on other parameter values

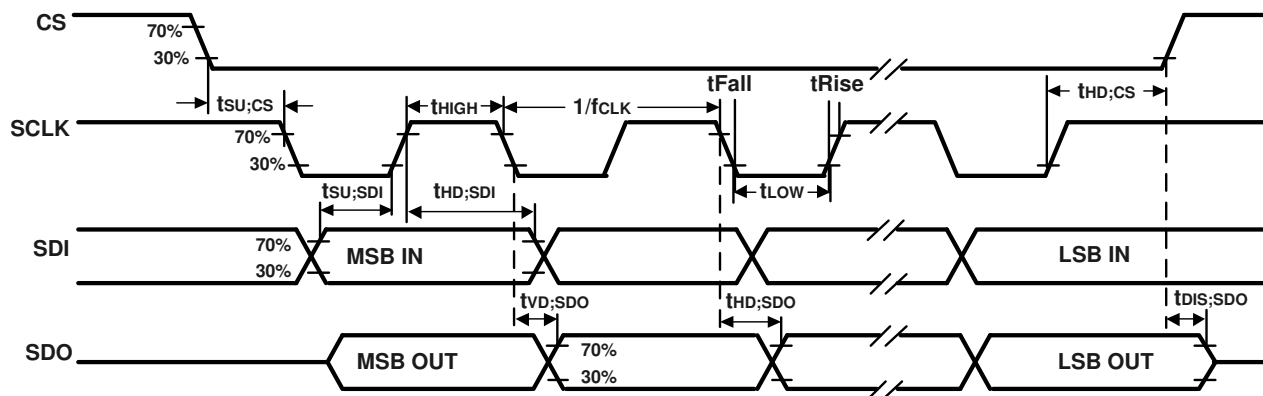


Figure 2. SPI Bus Timing Diagram

3.6 ABSOLUTE MAXIMUM RATINGS

Stress above those listed as “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to the absolute maximum ratings conditions for extended periods may affect device reliability.

PARAMETER	RATING
Supply Voltage, VDD	-0.5V to +4V
Supply Voltage, VDDIO	-0.5V to +4V
REGOUT	-0.5V to 2V
Input Voltage Level (AD0, FSYNC, SCL, SDA)	-0.5V to VDDIO + 0.5V
Acceleration (Any Axis, unpowered)	20,000g for 0.2 ms
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Electrostatic Discharge (ESD) Protection	2 kV (HBM); 250V (MM)
Latch-up	JEDEC Class II (2), 125°C ±100 mA

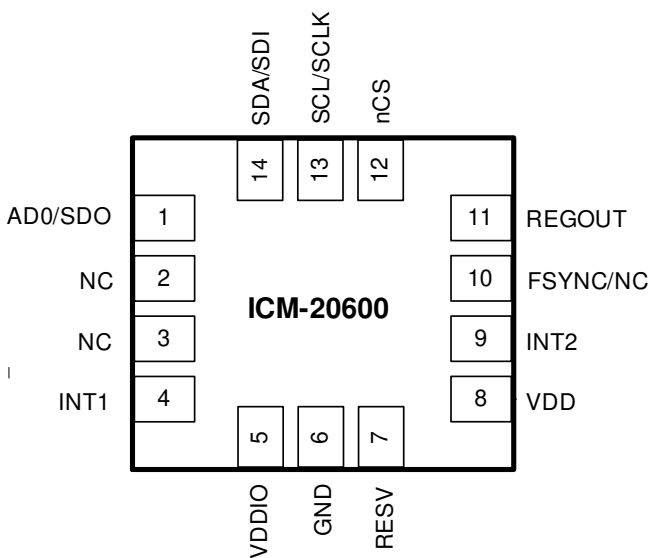
Table 8. Absolute Maximum Ratings

4 APPLICATIONS INFORMATION

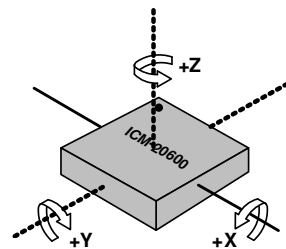
4.1 PIN OUT DIAGRAM AND SIGNAL DESCRIPTION

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	AD0 / SDO	I ² C slave address LSB (AD0); SPI serial data output (SDO)
2	NC	No Connect
3	NC	No Connect
4	INT1	Interrupt digital output (totem pole or open-drain)
5	VDDIO	Digital I/O supply voltage
6	GND	Power supply ground
7	RESV	Reserved, connect to ground
8	VDD	Power supply voltage
9	INT2	Interrupt digital output (totem pole or open-drain)
10	FSYNC / NC	Frame synchronization digital input or No Connect
11	REGOUT	Regulator filter capacitor connection
12	nCS	Chip select (SPI mode only)
13	SCL / SCLK	I ² C serial clock (SCL); SPI serial clock (SCLK)
14	SDA / SDI	I ² C serial data (SDA); SPI serial data input (SDI)

Table 9. Signal Descriptions



LGA Package (Top view)



Orientation of Axes of Sensitivity and Polarity of Rotation

Figure 3. Pin out Diagram for ICM-20600 2.5 mm x 3.0 mm x 0.91 mm LGA

4.2 TYPICAL OPERATING CIRCUIT

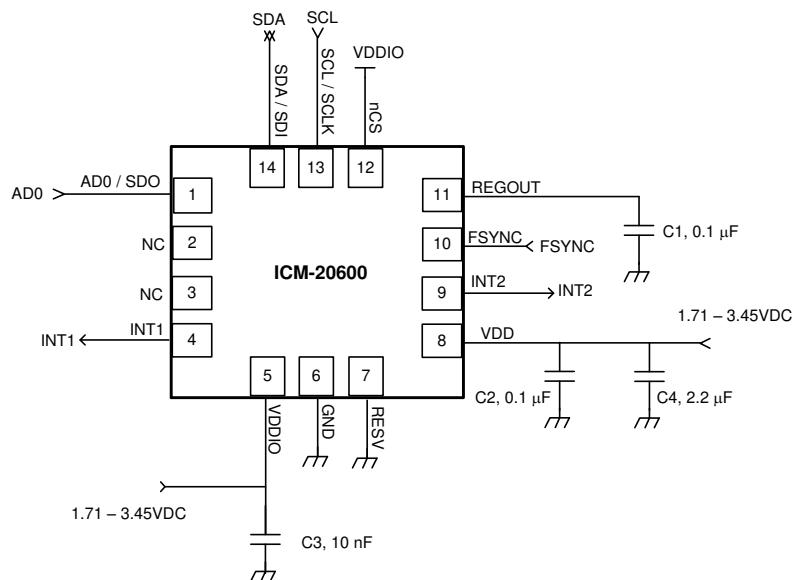


Figure 4. ICM-20600 LGA Application Schematic (I²C Operation)

Note: I²C lines are open drain and pullup resistors (e.g. 10kΩ) are required.

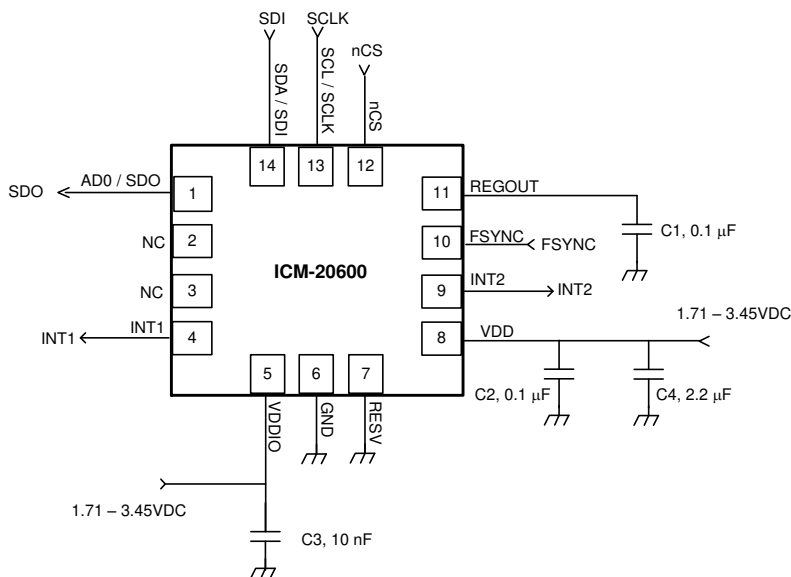


Figure 5. ICM-20600 LGA Application Schematic (SPI Operation)

4.3 BILL OF MATERIALS FOR EXTERNAL COMPONENTS

COMPONENT	LABEL	SPECIFICATION	QUANTITY
REGOUT Capacitor	C1	X7R, 0.1 μF ±10%	1
VDD Bypass Capacitors	C2	X7R, 0.1 μF ±10%	1
	C4	X7R, 2.2 μF ±10%	1
VDDIO Bypass Capacitor	C3	X7R, 10 nF ±10%	1

Table 10. Bill of Materials

4.4 BLOCK DIAGRAM

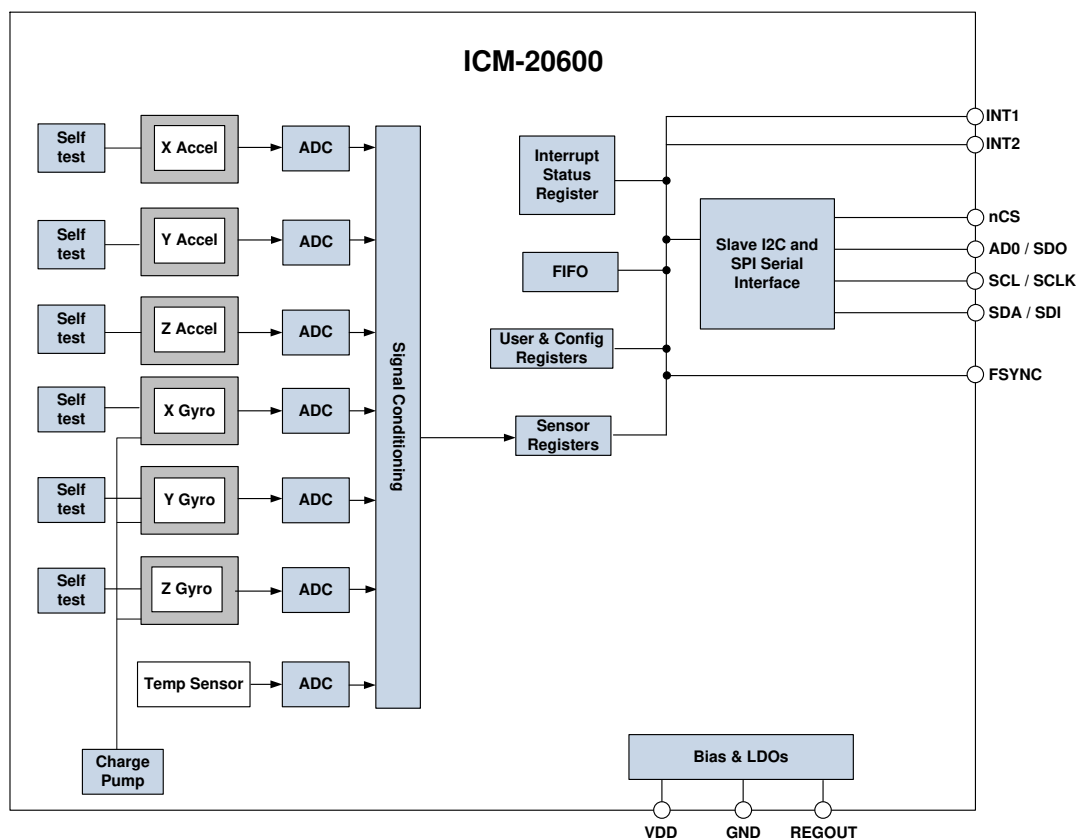


Figure 6. ICM-20600 Block Diagram

4.5 OVERVIEW

The ICM-20600 is comprised of the following key blocks and functions:

- Three-axis MEMS rate gyroscope sensor with 16-bit ADCs and signal conditioning
- Three-axis MEMS accelerometer sensor with 16-bit ADCs and signal conditioning
- Primary I²C and SPI serial communications interfaces
- Self-Test
- Clocking
- Sensor Data Registers
- FIFO
- Interrupts
- Digital-Output Temperature Sensor
- Bias and LDOs
- Charge Pump
- Standard Power Modes

4.6 THREE-AXIS MEMS GYROSCOPE WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20600 consists of three independent vibratory MEMS rate gyroscopes, which detect rotation about the X-, Y-, and Z- Axes. When the gyros are rotated about any of the sense axes, the Coriolis Effect causes a vibration that is detected by a capacitive pickoff. The resulting signal is amplified, demodulated, and filtered to produce a voltage that is proportional to the angular rate. This voltage is digitized using individual on-chip 16-bit Analog-to-Digital Converters (ADCs) to sample each axis. The full-scale range of the gyro sensors may be digitally programmed to ± 250 , ± 500 , ± 1000 , or ± 2000 degrees per second (dps). The ADC sample rate is programmable from 8,000 samples per second, down to 3.9 samples per second, and user-selectable low-pass filters enable a wide range of cut-off frequencies.

4.7 THREE-AXIS MEMS ACCELEROMETER WITH 16-BIT ADCS AND SIGNAL CONDITIONING

The ICM-20600’s 3-Axis accelerometer uses separate proof masses for each axis. Acceleration along a particular axis induces displacement on the corresponding proof mass, and capacitive sensors detect the displacement differentially. The ICM-20600’s architecture reduces the accelerometers’ susceptibility to fabrication variations as well as to thermal drift. When the device is placed on a flat surface, it will measure 0g on the X- and Y-axes and +1g on the Z-axis. The accelerometers’ scale factor is calibrated at the factory and is nominally independent of supply voltage. Each sensor has a dedicated sigma-delta ADC for providing digital outputs. The full scale range of the digital output can be adjusted to $\pm 2g$, $\pm 4g$, $\pm 8g$, or $\pm 16g$.

4.8 I²C AND SPI SERIAL COMMUNICATIONS INTERFACES

The ICM-20600 communicates to a system processor using either a SPI or an I²C serial interface. The ICM-20600 always acts as a slave when communicating to the system processor. The LSB of the I²C slave address is set by pin 1 (AD0).

ICM-20600 Solution Using I²C Interface

In Figure 7, the system processor is an I²C master to the ICM-20600.

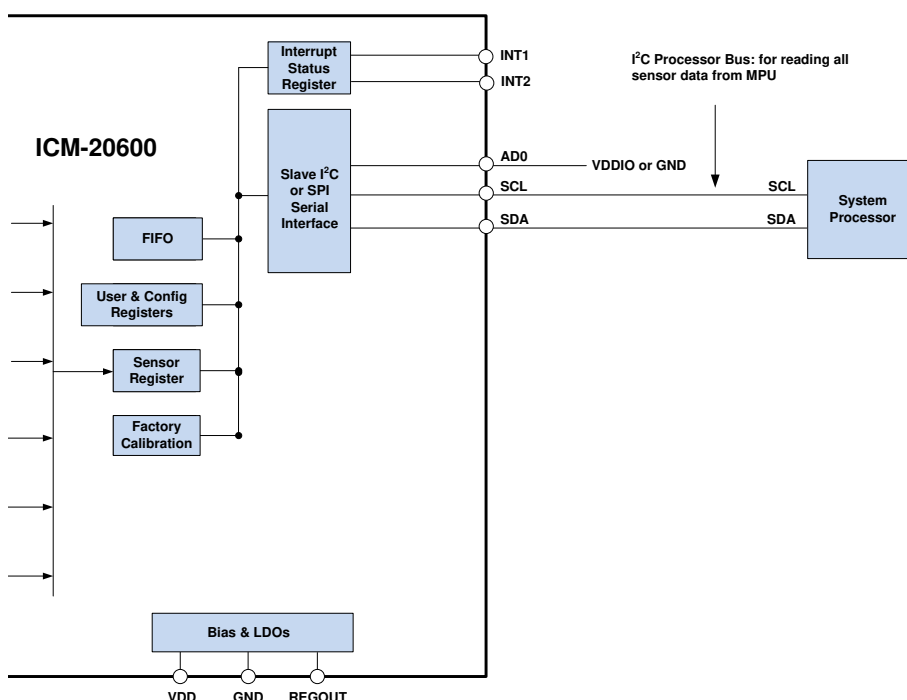


Figure 7. ICM-20600 Solution Using I²C Interface

ICM-20600 Solution Using SPI Interface

In Figure 8 below, the system processor is an SPI master to the ICM-20600. Pins 1, 12, 13, and 14 are used to support the SDO, nCS, SCLK, and SDI signals for SPI communications.

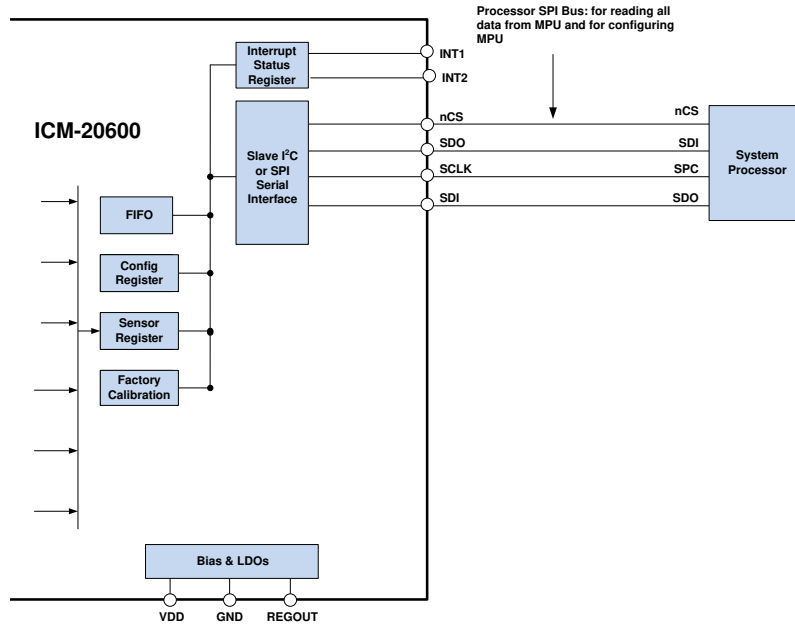


Figure 8. ICM-20600 Solution Using SPI Interface

4.9 SELF-TEST

Self-test allows for the testing of the mechanical and electrical portions of the sensors. The self-test for each measurement axis can be activated by means of the gyroscope and accelerometer self-test registers.

When the self-test is activated, the electronics cause the sensors to be actuated and produce an output signal. The output signal is used to observe the self-test response.

The self-test response is defined as follows:

$$\text{SELF-TEST RESPONSE} = \text{SENSOR OUTPUT WITH SELF-TEST ENABLED} - \text{SENSOR OUTPUT WITH SELF-TEST DISABLED}$$

The self-test response for each gyroscope axis is defined in the gyroscope specification table, while that for each accelerometer axis is defined in the accelerometer specification table.

When the value of the self-test response is within the specified min/max limits of the product specification, the part has passed self-test. When the self-test response exceeds the min/max values, the part is deemed to have failed self-test.

4.10 CLOCKING

The ICM-20600 has a flexible clocking scheme, allowing a variety of internal clock sources to be used for the internal synchronous circuitry. This synchronous circuitry includes the signal conditioning and ADCs, and various control circuits and registers. An on-chip PLL provides flexibility in the allowable inputs for generating this clock.

Allowable internal sources for generating the internal clock are:

- a) An internal relaxation oscillator
- b) Auto-select between internal relaxation oscillator and gyroscope MEMS oscillator to use the best available source

The only setting supporting specified performance in all modes is option b). It is recommended that option b) be used.

4.11 SENSOR DATA REGISTERS

The sensor data registers contain the latest gyroscope, accelerometer, and temperature measurement data. They are read-only registers, and are accessed via the serial interface. Data from these registers may be read anytime.

4.12 FIFO

The ICM-20600 contains a 1 KB FIFO (FIFO depth 1008 bytes) register that is accessible via the Serial Interface. The FIFO configuration register determines which data is written into the FIFO. Possible choices include gyro data, accelerometer data, temperature readings, and FSYNC input. A FIFO counter keeps track of how many bytes of valid data are contained in the FIFO. The FIFO register supports burst reads. The interrupt function may be used to determine when new data is available.

The ICM-20600 allows FIFO read in low-power accelerometer mode. A programmable FIFO watermark is included, with data-ready interrupt triggered when the watermark is reached.

4.13 INTERRUPTS

Interrupt functionality is configured via the Interrupt Configuration register. Items that are configurable include the INT1 and INT2 pins configuration, the interrupt latching and clearing method, and triggers for the interrupt. Items that can trigger an interrupt are (1) Clock generator locked to new reference oscillator (used when switching clock sources); (2) new data is available to be read (from the FIFO and Data registers); (3) accelerometer event interrupts; (4) FIFO overflow. The interrupt status can be read from the Interrupt Status register.

4.14 DIGITAL-OUTPUT TEMPERATURE SENSOR

An on-chip temperature sensor and ADC are used to measure the ICM-20600 die temperature. The readings from the ADC can be read from the FIFO or the Sensor Data registers.

4.15 BIAS AND LDOS

The bias and LDO section generates the internal supply and the reference voltages and currents required by the ICM-20600. Its two inputs are an unregulated VDD and a VDDIO logic reference supply voltage. The LDO output is bypassed by a capacitor at REGOUT. For further details on the capacitor, please refer to the Bill of Materials for External Components.

4.16 CHARGE PUMP

An on-chip charge pump generates the high voltage required for the MEMS oscillator.

4.17 STANDARD POWER MODES

The following table lists the user-accessible power modes for ICM-20600.

MODE	NAME	GYRO	ACCEL
1	Sleep Mode	Off	Off
2	Standby Mode	Drive On	Off
3	Accelerometer Low-Power Mode	Off	Duty-Cycled
4	Accelerometer Low-Noise Mode	Off	On
5	Gyroscope Low-Power Mode	Duty-Cycled	Off
6	Gyroscope Low-Noise Mode	On	Off
7	6-Axis Low-Noise Mode	On	On
8	6-Axis Low-Power Mode	Duty-Cycled	On

Table 11. Standard Power Modes for ICM-20600

Notes:

1. Power consumption for individual modes can be found in the D.C. Electrical Characteristics section.

5 PROGRAMMABLE INTERRUPTS

The ICM-20600 has a programmable interrupt system that can generate an interrupt signal on the INT pins. Status flags indicate the source of an interrupt. Interrupt sources may be enabled and disabled individually. Interrupts carried on INT1 and INT2 pins are shown in the table below. If INT2 is not enabled, all interrupts are mapped to INT1.

INTERRUPT NAME	MODULE
Motion Detection	INT2
FIFO Overflow	INT2
FIFO Watermark	INT1
Data Ready	INT1
FSYNC	INT2

Table 12. Table of Interrupt Sources

5.1 WAKE-ON-MOTION INTERRUPT

The ICM-20600 provides motion detection capability. A qualifying motion sample is one where the high passed sample from any axis has an absolute value exceeding a user-programmable threshold. The following steps explain how to configure the Wake-on-Motion Interrupt.

Step 1: Ensure that Accelerometer is running

- In PWR_MGMT_1 register (0x6B) set CYCLE = 0, SLEEP = 0, and GYRO_STANDBY = 0
- In PWR_MGMT_2 register (0x6C) set STBY_XA = STBY_YA = STBY_ZA = 0, and STBY_XG = STBY_YG = STBY_ZG = 1

Step 2: Accelerometer Configuration

- In ACCEL_CONFIG2 register (0x1D) set ACCEL_FCHOICE_B = 1 and A_DLPF_CFG[2:0] = 1 (b001)

Step 3: Enable Motion Interrupt

- In INT_ENABLE register (0x38) set WOM_X_INT_EN = WOM_Y_INT_EN = WOM_Z_INT_EN = 1 to enable motion interrupt for X, Y, and Z axis

Step 4: Set Motion Threshold

- Set the motion threshold for X-axis in ACCEL_WOM_X_THR register (0x20)
- Set the motion threshold for Y-axis in ACCEL_WOM_Y_THR register (0x21)
- Set the motion threshold for Z-axis in ACCEL_WOM_Z_THR register (0x22)

Step 5: Set Interrupt Mode

- In ACCEL_INTEL_CTRL register (0x69) clear bit 0 (WOM_TH_MODE) to select the motion interrupt as an OR of the enabled interrupts for X, Y, Z-axes and set bit 0 to make the interrupt an AND of the enabled interrupts for X, Y, Z axes

Step 6: Enable Accelerometer Hardware Intelligence

- In ACCEL_INTEL_CTRL register (0x69) set ACCEL_INTEL_EN = ACCEL_INTEL_MODE = 1

Step 7: Set Frequency of Wake-Up

- In SMPLRT_DIV register (0x19) set SMPLRT_DIV[7:0] = 3.9Hz – 500Hz

Step 8: Enable Cycle Mode (Accelerometer Low-Power Mode)

- In PWR_MGMT_1 register (0x6B) set CYCLE = 1

6 DIGITAL INTERFACE

6.1 I²C AND SPI SERIAL INTERFACES

The internal registers and memory of the ICM-20600 can be accessed using either I²C at 400 kHz or SPI at 10 MHz. SPI operates in four-wire mode.

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	AD0 / SDO	I ² C Slave Address LSB (AD0); SPI serial data output (SDO)
12	nCS	Chip select (SPI mode only)
13	SCL / SCLK	I ² C serial clock (SCL); SPI serial clock (SCLK)
14	SDA / SDI	I ² C serial data (SDA); SPI serial data input (SDI)

Table 13. Serial Interface

Note:
To prevent switching into I²C mode when using SPI, the I²C interface should be disabled by setting the *I2C_IF_DIS* configuration bit. Setting this bit should be performed immediately after waiting for the time specified by the “Start-Up Time for Register Read/Write” in Section 0.
For further information regarding the *I2C_IF_DIS* bit, please refer to sections 7 and **Error! Reference source not found.** of this document.

6.2 I²C INTERFACE

I²C is a two-wire interface comprised of the signals serial data (SDA) and serial clock (SCL). In general, the lines are open-drain and bi-directional. In a generalized I²C interface implementation, attached devices can be a master or a slave. The master device puts the slave address on the bus, and the slave device with the matching address acknowledges the master.

The ICM-20600 always operates as a slave device when communicating to the system processor, which thus acts as the master. SDA and SCL lines typically need pull-up resistors to VDD. The maximum bus speed is 400 kHz.

The slave address of the ICM-20600 is b110100X which is 7 bits long. The LSB bit of the 7-bit address is determined by the logic level on pin AD0. This allows two ICM-20600s to be connected to the same I²C bus. When used in this configuration, the address of one of the devices should be b1101000 (pin AD0 is logic low) and the address of the other should be b1101001 (pin AD0 is logic high).

6.3 I²C COMMUNICATIONS PROTOCOL

START (S) and STOP (P) Conditions

Communication on the I²C bus starts when the master puts the START condition (S) on the bus, which is defined as a HIGH-to-LOW transition of the SDA line while SCL line is HIGH (see figure below). The bus is considered to be busy until the master puts a STOP condition (P) on the bus, which is defined as a LOW to HIGH transition on the SDA line while SCL is HIGH (see figure below).

Additionally, the bus remains busy if a repeated START (Sr) is generated instead of a STOP condition.

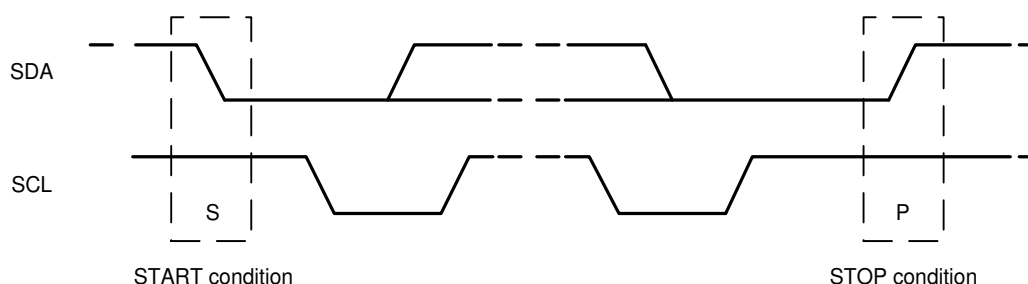


Figure 9. START and STOP Conditions

Data Format / Acknowledge

I²C data bytes are defined to be 8-bits long. There is no restriction to the number of bytes transmitted per data transfer. Each byte transferred must be followed by an acknowledge (ACK) signal. The clock for the acknowledge signal is generated by the master, while the receiver generates the actual acknowledge signal by pulling down SDA and holding it low during the HIGH portion of the acknowledge clock pulse.

If a slave is busy and cannot transmit or receive another byte of data until some other task has been performed, it can hold SCL LOW, thus forcing the master into a wait state. Normal data transfer resumes when the slave is ready, and releases the clock line (refer to the following figure).

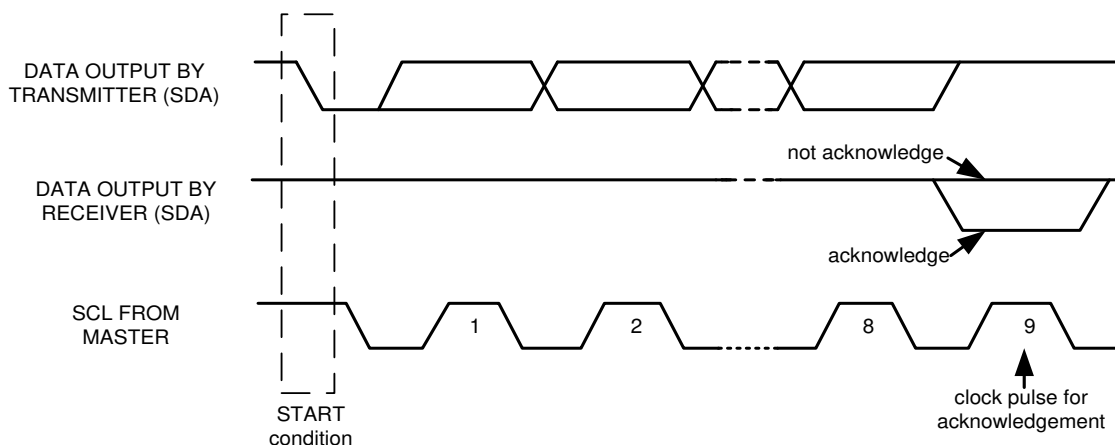


Figure 10. Acknowledge on the I²C Bus

Communications

After beginning communications with the START condition (S), the master sends a 7-bit slave address followed by an 8th bit, the read/write bit. The read/write bit indicates whether the master is receiving data from or is writing to the slave device. Then, the master releases the SDA line and waits for the acknowledge signal (ACK) from the slave device. Each byte transferred must be followed by an acknowledge bit. To acknowledge, the slave device pulls the SDA line LOW and keeps it LOW for the high period of the SCL line. Data transmission is always terminated by the master with a STOP condition (P), thus freeing the communications line. However, the master can generate a repeated START condition (Sr), and address another slave without first generating a STOP condition (P). A LOW to HIGH transition on the SDA line while SCL is HIGH defines the stop condition. All SDA changes should take place when SCL is low, with the exception of start and stop conditions.

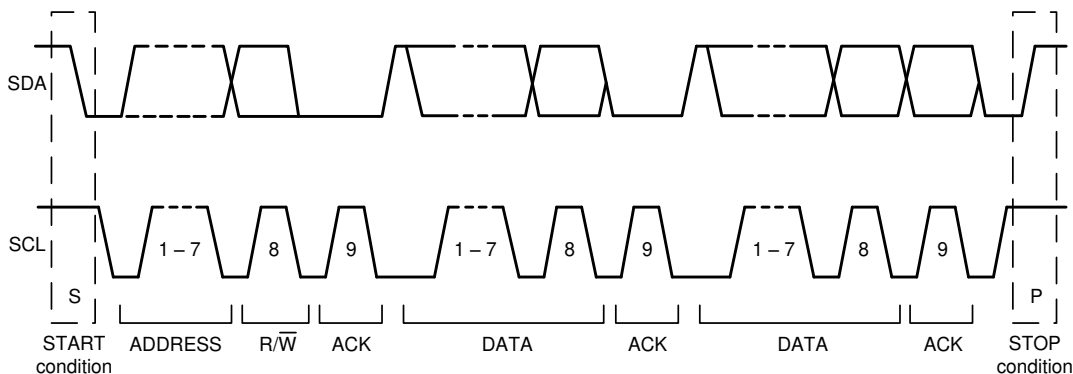


Figure 11. Complete I²C Data Transfer