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3.3-V 10Base-T/100Base-TX Integrated PHYceiver™

General

The ICS1893AF is a lower cost, re-packaged version of the ICS1893Y-10. The ICS1893AF is a fully integrated, Physical Layer device (PHY) that is compliant with both the 10Base-T and 100Base-TX CSMA/CD Ethernet Standard, ISO/IEC 8802-3. The ICS1893AF uses the same proven silicon as the ICS1893Y-10 but offers a lower cost solution by using a lower cost 300 mil. 48-lead SSOP package.

The ICS1893AF uses the same twisted-pair transmit and receive circuits as the ICS1893Y-10, and the same recommended board layout techniques apply to the ICS1893AF.

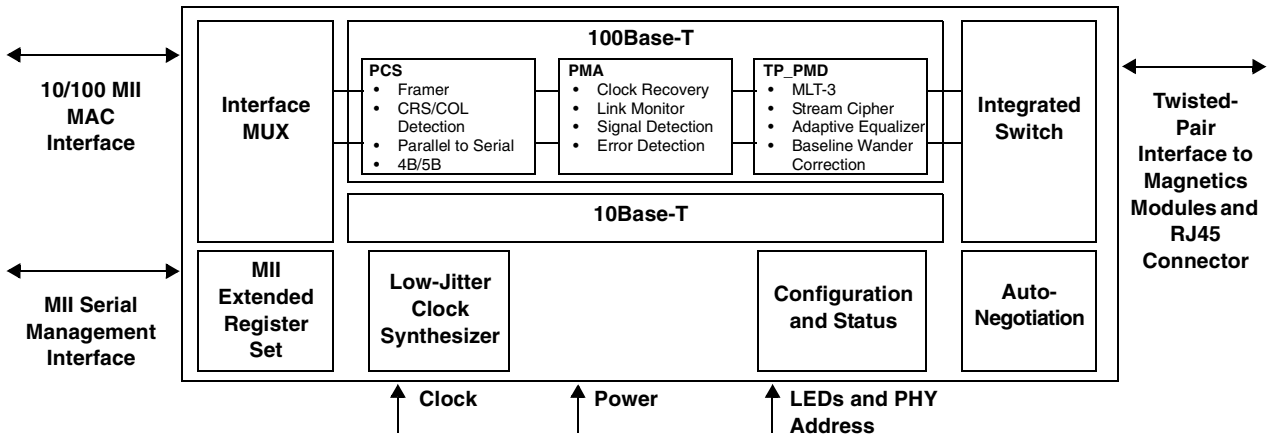
The ICS1893AF is intended for Node applications using the standard MII interface to the MAC.

All differences in the ICS1893AF / ICS1893Y-10 Feature Set are listed in the Comparison Table on page 2.

Features

- Single 3.3V power supply
- Supports category 5 cables with attenuation in excess of 24dB at 100 MHz.
- DSP-based baseline wander correction to virtually eliminate killer packets
- Low-power, 0.35-micron CMOS (typically 400 mW)
- Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sublayers of IEEE standard
- 10Base-T and 100Base-TX IEEE 802.3 compliant
- Clock or crystal supported
- Media Independent Interface (MII) supported
- Managed or Unmanaged Applications
- 10M or 100M Half and Full Duplex Modes
- Auto-Negotiation with Parallel detection for Legacy products
- Fully integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline wander correction
  - Transmit wave shaping and stream cipher scrambler
  - MLT-3 encoder and NRZ/NRZI encoder
- Loopback mode for Diagnostic Functions
- Small footprint 48-pin 300 mil SSOP package

ICS1893AF, Rev. C Block



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Revision History

- The initial release of this document was dated 5 April 2002.
- This release of this document, Rev B, is dated 6 March 2003. The following list indicates where changes occur.
  - Table of Contents reflect page renumbering.
  - Figure 6-3, “Crystal or Oscillator Operation”, corrected 33 pF to 33 Ohm in Oscillator operation.
  - Section 7.5.5. “When the 10Base-T link is:, Invalid / Valid Smart Squelch function”. Changed each “logic” number from zero to one, or the reverse.
  - Table 8-10, changed “Decimal” revision number from 0 to 1.
  - Table 8-11, deleted “Note 1” at foot of table. On bits 4.5 through 4.8, replaced “Note 1” notation in “Access” column with R/W.
  - Section 8.14. Deleted two paragraphs made redundant by change made to Table 8-21.
  - Table 8-21, Bit 19.5, changed “Force LEDs On” to ”ICS Reserved”.
  - Table 9-6, revised P3TD Pin 6 and P4RD Pin 8 Pin Description.
  - Table 10-3, “Note” paragraph deleted.
  - Figure 10-1, deleted capacitors across resistors 10TCSR and 100TCSR.
  - Table 10-4, changed “Supply Current Power-Down” IDD from 40 to 4 (Typ) and from 50 to 5 (Max). In addition, changed “Supply Current Reset” IDD from 50 to 10 (Typ) and from 60 to 11 (Max).
  - Figure 12-1, “Package Type” added AFI = 48 Lead 300 mil. SSOP Industrial Temp.

Chapter 1 Abbreviations and Acronyms

Table 1-1 lists and interprets the abbreviations and acronyms used throughout this data sheet.

Table 1-1. Abbreviations and Acronyms

Abbreviation / Acronym	Interpretation
4B/5B	4-Bit / 5-Bit Encoding/Decoding
ANSI	American National Standards Institute
CMOS	complimentary metal-oxide semiconductor
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
CW	Command Override Write
DSP	digital signal processing
ESD	End-of-Stream Delimiter
FDDI	Fiber Distributed Data Interface
FLL	frequency-locked loop
FLP	Fast Link Pulse
IDL	A ‘dead’ time on the link following a 10Base-T packet, not to be confused with idle
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
ISO	International Standards Organization
LH	Latching High
LL	Latching Low
LMX	Latching Maximum
MAC	Media Access Control
Max.	maximum
Mbps	Megabits per second
MDI	Media Dependent Interface
MF	Management Frame
MII	Media Independent Interface
Min.	minimum
MLT-3	Multi-Level Transition Encoding (3 Levels)
N/A	Not Applicable
NLP	Normal Link Pulse
No.	Number
NRZ	Not Return to Zero
NRZI	Not Return to Zero, Invert on one
OSI	Open Systems Interconnection

Table 1-1. Abbreviations and Acronyms (*Continued*)

Abbreviation / Acronym	Interpretation
OUI	Organizationally Unique Identifier
PCS	Physical Coding sublayer
PHY	physical-layer device The ICS1893AF, Rev. C is a physical-layer device, also referred to as a 'PHY' or 'PHYceiver'. (The ICS1890 is also a physical-layer device.)
PLL	phase-locked loop
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
ppm	parts per million
QFP	quad flat pack
RO	read only
R/W	read/write
R/W0	read/write zero
SC	self-clearing
SF	Special Functions
SFD	Start-of-Frame Delimiter
SI	Stream Interface, Serial Interface, or Symbol Interface. With reference to the MII/SI pin, the acronym 'SI' has multiple meanings. • Generically, SI means 'Stream Interface', and is documented as such in this data sheet. • However, when the MAC/Repeater Interface is configured for: – 10M operations, SI is an acronym for 'Serial Interface'. – 100M operations, SI is an acronym for 'Symbol Interface'.
SQE	Signal Quality Error
SSD	Start-of-Stream Delimiter
STA	Station Management Entity
STP	shielded twisted pair
TAF	Technology Ability Field
TP-PMD	Twisted-Pair Physical Layer Medium Dependent
Typ.	typical
UTP	unshielded twisted pair

Chapter 2 Conventions and Nomenclature

Table 2-1 lists and explains the conventions and nomenclature used throughout this data sheet.

Table 2-1. Conventions and Nomenclature

Item	Convention / Nomenclature
Bits	• A bit in a register is identified using the format 'register.bit'. For example, bit 0.15 is bit 15 of register 0. • When a colon is used with bits, it indicates the range of bits. For example, bits 1.15:11 are bits 15, 14, 13, 12, and 11 of register 1. • For a range of bits, the order is always from the most-significant bit to the least-significant bit.
Code groups	Within this table, see the item 'Symbols'
Colon (:)	Within this table, see these items: • 'Bits' • 'Pin (or signal) names'
Numbers	• As a default, all numbers use the decimal system (that is, base 10) unless followed by a lowercase letter. A string of numbers followed by a lowercase letter: – A 'b' represents a binary (base 2) number – An 'h' represents a hexadecimal (base 16) number – An 'o' represents an octal (base 8) number • All numerical references to registers use decimal notation (and not hexadecimal).
Pin (or signal) names	• All pin or signal names are provided in capital letters. • A pin name that includes a forward slash '/' is a multi-function, configuration pin. These pins provide the ability to select between two ICS1893AF, Rev. C functions. The name provided: – Before the '/' indicates the pin name and function when the signal level on the pin is logic zero. – After the '/' indicates the pin name and function when the signal level on the pin is logic one. For example, the HW/SW pin selects between Hardware (HW) mode and Software (SW) mode. When the signal level on the HW/SW pin is logic: – Zero, the ICS1893AF, Rev. C Hardware mode is selected. – One, the ICS1893AF, Rev. C Software mode is selected. • An 'n' appended to the end of a pin name or signal name (such as RESETn) indicates an active-low operation. • When a colon is used with pin or signal names, it indicates a range. For example, TXD[3:0] represents pins/signals TXD3, TXD2, TXD1, and TXD0. • When pin name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the pin name abbreviation.
Registers	• A bit in a register is identified using the format 'register.bit'. For example, bit 0.15 is bit 15 of register 0. • All numerical references to registers use decimal notation (and not hexadecimal). • When register name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the register name abbreviation.

Table 2-1. Conventions and Nomenclature (*Continued*)

Item	Convention / Nomenclature
Signal references	• When referring to signals, the terms: – 'FALSE', 'low', or 'zero' represent signals that are logic zero. – 'TRUE', 'high', or 'one' represent signals that are logic one. • Chapter 10, "DC and AC Operating Conditions" defines the electrical specifications for 'logic zero' and 'logic one' signals.
Symbols	• In this data sheet, code group names are referred to as 'symbols' and they are shown between '/' (slashes). For example, the symbol /J/ represents the first half of the Start-of-Stream Delimiter (SSD1). • Symbol sequences are shown in succession. For example, /I/J/K/ represents an IDLE followed by the SSD.
Terms: 'set', 'active', 'asserted',	The terms 'set', 'active', and 'asserted' are synonymous. They do not necessarily infer logic one. (For example, an active-low signal can be set to logic zero.)
Terms: 'cleared', 'de-asserted', 'inactive'	The terms 'cleared', 'inactive', and 'de-asserted' are synonymous. They do not necessarily infer logic zero.
Terms: 'twisted-pair receiver'	In reference to the ICS1893AF, Rev. C, the term 'Twisted-Pair Receiver' refers to the set of Twisted-Pair Receive output pins (TP_RXP and TP_RXN).
Terms: 'twisted-pair transmitter'	In reference to the ICS1893AF, Rev. C, the term 'Twisted-Pair Transmitter' refers to the set of Twisted-Pair Transmit output pins (TP_TXP and TP_TXN).

Chapter 3 Typical ICS1893AF Applications

The ICS1893AF is configured for the majority of single Phy Ethernet applications. These applications include Network Interface Cards, PC Motherboards, Printers, ACR Riser cards, Set top Boxes, and Game machines.

Virtually any single Phy application utilizing the standard IEEE MII interface can use the ICS1893AF. The ICS1893AF offers the same high performance at a lower cost.

Table 3-1. ICS1893AF / ICS1893Y-10 Feature Set Comparison Table

Feature	ICS1893AF	ICS1893Y-10	Comment
Package Type	**SSOP 300mil**	**TQFP 10x10x1.0**	
Pin Count	**48**	**64**	
NOD/REP	NOD/REP pin removed tied internally to VSS	NOD/REP	ICS1893AF configured in NODE mode only.
HW/SW	MII/SI pin removed tied internally to VDD	MII/SI	ICS1893AF configured in software mode only.
MII/SI	SI/MII pin removed tied internally to VSS	SI/MII	ICS1893AF supports only MII interface to MAC.
10/100	10/100 pin is output only	10/100	The 10/100 pin in software mode is an output indicating 100M operation when high.
DPXSEL	DPXSEL pin removed	DPXSEL	FD/HD information is available in the Quick Poll Status Register Reg 17.
ANSEL	DPXSEL pin removed	ANSEL	ANSEL in software mode is an output. This information is available in control Reg 0, Default setting is A-N enabled.
LSTA	LSTA pin removed	LSTA	Link status available on P2LI led
LOCK	LOCK pin removed	LOCK	Link status available on P2LI led
TXER	TXER pin removed tied internally to VSS	TXER	TXER function is still available by using control Reg

3.1 The following bullet items describe ICS1893AF pin differences and how they affect the application:

- The ICS1893AF is hardwired for the predominate board application used in the vast majority of single Phy applications:

  - Hardwired for Node configuration (NOD/REP pin removed, tied internally to VSS). Node configuration enables the 10M SQE test default setting and causes CRS to be asserted for either transmit or receive activity in half duplex, or for just receive activity when in full duplex.
  - Hardwired for Software mode (HW/SW pin removed, tied internally to VDD).
  - Hardwired for MII interface only. (MII/SI pin removed, tied internally to VSS). In this configuration the 10baseT serial and 100baseTX 5 bit symbol interfaces are NOT supported. Applications requiring these interfaces should use ICS1893Y-10.
- In the software control configuration the 10/100, DPXSEL and ANSEL pins are outputs.
  - DPXEL pin is not brought out.
  - ANSEL pin is not brought out.
  - 10/100 pin is brought out to indicate 100M operation. Some applications use this output to drive an LED indicating 100M operation.
- Pins LSTA (link status) and LOCK (rec. PLL locked) are not brought out.
  - LSTA and LOCK provided redundant information already available with the P2LI pin. P2LI indicates the Link is valid.
- Input pin TXER is removed and tied low inside the package. The TXER function is still available by using the Extended Control Register Reg 16 Bit 2. Most applications tied the TXER pin to VSS.

3.2 ISC1893AF Shared Features

- The same silicon die is used in the ICS1893AF and ICS1893Y-10
  - Only the package type is different.
- The ICS1893AF offers the same.35µ 3.3V low power operation.
- Parametric specifications and timing diagrams are the same as ICS1893Y-10.
- Both the ICS1893Y-10 and the ICS1893AF incorporate Digital Signal Processing in their PMD Sub layer, thereby allowing them to transmit and receive data with Unshielded Twisted Pair (UTP) Category 5 cables up to 150 meters in length. In addition, this ICS-patented technology enables the ICS1893Y-10 ICS1893AF to address the effects of Baseline Wander correction.
- Both ICS1893AF and ICS1893Y-10 have improved 10Base-T Squelch operation.
- The ICS1893AF uses the same twisted pair transmitter and receive circuits and therefore the same recommended board layout techniques apply.
- Both share improved transmit circuits resulting in a decrease in the magnitude of the 10Base-T harmonic content generated during transmission (reference ISO/IEC 8802-3: 1993 Clause 8.3.1.3).
- Both use digital PLL technology resulting in lower jitter and improved stability.
- The MDIO Maintenance interface with the MDIO and MDC pins along with all internal registers are preserved in the ICS1893AF. This enables software configuring for FD/HD, 10Base-T, 100Base-TX and Auto-Negotiation to be configurable by the MDIO maintenance interface. Default setting is Auto-Negotiation Enable. All register settings are the same as in the ICS1893AF datasheet.
- The ICS1893AF preserves the dual-purpose LED/Phy Address control pins as in the ICS1893Y-10. The captured address seeds the scrambler for lower EMI in for multiple Phy applications.
- All Auto-Negotiation features are preserved in the ICS1893AF. The reset default mode is A_N enabled. The A_N parallel detect feature is preserved for legacy interoperability.
- Both support Management Frame (MF) Preamble Suppression.
- Both support backward compatibility with the ICS1890 Management Registers.

Chapter 4 Overview of the ICS1893AF, Rev. C

The ICS1893AF is a stream processor. During data transmission, it accepts sequential nibbles from its MAC (Media Access Control) converts them into a serial bit stream, encodes them, and transmits them over the medium through an external isolation transformer. When receiving data, the ICS1893AF converts and decodes a serial bit stream (acquired from an isolation transformer that interfaces with the medium) into sequential nibbles. It subsequently presents these nibbles to its MAC Interface.

The ICS1893AF implements the OSI model's physical layer, consisting of the following, as defined by the ISO/IEC 8802-3 standard:

- Physical Coding sublayer (PCS)
- Physical Medium Attachment sublayer (PMA)
- Physical Medium Dependent sublayer (PMD)
- Auto-Negotiation sublayer

The ICS1893AF is transparent to the next layer of the OSI model, the link layer. The link layer has two sublayers: the Logical Link Control sublayer and the MAC sublayer. The ICS1893AF can interface directly to the MAC.

The ICS1893AF transmits framed packets acquired from its MAC Interface and receives encapsulated packets from another PHY, which it translates and presents to its MAC Interface.

Note: As per the ISO/IEC standard, the ICS1893AF does not affect, nor is it affected by, the underlying structure of the MAC/repeater frame it is conveying.

4.1 100Base-TX Operation

During 100Base-TX data transmission, the ICS1893AF accepts packets from a MAC and inserts Start-of-Stream Delimiters (SSDs) and End-of-Stream Delimiters (ESDs) into the data stream. The ICS1893AF, Rev. C encapsulates each MAC/repeater frame, including the preamble, with an SSD and an ESD. As per the ISO/IEC Standard, the ICS1893AF, Rev. C replaces the first octet of each MAC preamble with an SSD and appends an ESD to the end of each MAC/repeater frame.

When receiving data from the medium, the ICS1893AF, Rev. C removes each SSD and replaces it with the pre-defined preamble pattern before presenting the nibbles to its MAC Interface. When the ICS1893AF, Rev. C encounters an ESD in the received data stream, signifying the end of the frame, it ends the presentation of nibbles to its MAC Interface. Therefore, the local MAC receives an unaltered copy of the transmitted frame sent by the remote MAC/repeater.

During periods when MAC frames are being neither transmitted nor received, the ICS1893AF, Rev. C signals and detects the IDLE condition on the Link Segment. In the 100Base-TX mode, the ICS1893AF, Rev. C transmit channel sends a continuous stream of scrambled ones to signify the IDLE condition. Similarly, the ICS1893AF, Rev. C receive channel continually monitors its data stream and looks for a pattern of scrambled ones. The results of this signaling and monitoring provide the ICS1893AF, Rev. C with the means to establish the integrity of the Link Segment between itself and its remote link partner and inform its Station Management Entity (STA) of the link status.

For 100M data transmission, the ICS1893AF, Rev. C MAC Interface is configured to provide a 100M Media Independent Interface (MII).

4.2 10Base-T Operation

During 10Base-T data transmission, the ICS1893AF, Rev. C inserts only the IDL delimiter into the data stream. The ICS1893AF, Rev. C appends the IDL delimiter to the end of each MAC frame. However, since the 10Base-T preamble already has a Start-of-Frame delimiter (SFD), it is not required that the ICS1893AF insert an SSD-like delimiter.

When receiving data from the medium (such as a twisted-pair cable), the ICS1893AF, Rev. C uses the preamble to synchronize its receive clock. When the ICS1893AF, Rev. C receive clock establishes lock, it presents the preamble nibbles to its MAC Interface. The 10M MAC Interface can be configured as either a 10M MII Interface.

In 10M operations, during periods when MAC frames are being neither transmitted nor received, the ICS1893AF, Rev. C signals and detects Normal Link Pulses. This action allows the integrity of the Link Segment with the remote link partner to be established and then reported to the ICS1893AF, Rev. C's STA.

Chapter 5 Operating Modes Overview

The ICS1893AF, Rev. C operating modes are typically controlled from software.

The ICS1893AF register bits are accessible through a standard MII (Media Independent Interface) Serial Management Port.

The ICS1893AF, Rev. C is configured to support the MAC Interface as a 10M MII or a 100M MII. The protocol on the Medium Dependent Interface (MDI) can be configured to support either 10M or 100M operations in either half-duplex or full-duplex modes.

The ICS1893AF, Rev. C is fully compliant with the ISO/IEC 8802-3 standard, as it pertains to both 10Base-T and 100Base-TX operations. The feature-rich ICS1893AF, Rev. C allows easy migration from 10-Mbps to 100-Mbps operations as well as from systems that require support of both 10M and 100M links.

This chapter is an overview of the following ICS1893AF, Rev. C modes of operation:

- Section 5.1, “Reset Operations”
- Section 5.2, “Power-Down Operations”
- Section 5.3, “Automatic Power-Saving Operations”
- Section 5.4, “Auto-Negotiation Operations”
- Section 5.5, “100Base-TX Operations”
- Section 5.6, “10Base-T Operations”
- Section 5.7, “Half-Duplex and Full-Duplex Operations”

5.1 Reset Operations

This section first discusses reset operations in general and then specific ways in which the ICS1893AF, Rev. C can be configured for various reset options.

5.1.1 General Reset Operations

The following reset operations apply to all the specific ways in which the ICS1893AF, Rev. C can be reset, which are discussed in Section 5.1.2, “Specific Reset Operations”.

5.1.1.1 Entering Reset

When the ICS1893AF, Rev. C enters a reset condition (either through hardware, power-on reset, or software), it does the following:

1. Isolates the MAC/Repeater Interface input pins
2. Drives all MAC/Repeater Interface output pins low
3. Tri-states the signals on its Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
4. Initializes all its internal modules and state machines to their default states
5. Enters the power-down state
6. Initializes all internal latching low (LL), latching high (LH), and latching maximum (LMX) Management Register bits to their default values

5.1.1.2 Exiting Reset

When the ICS1893AF, Rev. C exits a reset condition, it does the following:

1. Exits the power-down state
2. Latches the Serial Management Port Address of the ICS1893AF, Rev. C into the Extended Control Register, bits 16.10:6. [See Section 8.11.3, “PHY Address (bits 16.10:6)”.]
3. Enables all its internal modules and state machines
4. Sets all Management Register bits to either (1) their default values or (2) the values specified by their associated ICS1893AF, Rev. C input pins, as determined by the HW/SW pin
5. Enables the Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
6. Resynchronizes both its Transmit and Receive Phase-Locked Loops, which provide its transmit clock (TXCLK) and receive clock (RXCLK)
7. Releases all MAC/Repeater Interface pins, which takes a maximum of 640 ns after the reset condition is removed

5.1.1.3 Hot Insertion

As with the ICS189X products, the ICS1893AF, Rev. C reset design supports ‘hot insertion’ of its MII. (That is, the ICS1893AF, Rev. C can connect its MAC/Repeater Interface to a MAC/repeater while power is already applied to the MAC/repeater.)

5.1.2 Specific Reset Operations

This section discusses the following specific ways that the ICS1893AF, Rev. C can be reset:

- Hardware reset (using the RESETn pin)
- Power-on reset (applying power to the ICS1893AF, Rev. C)
- Software reset (using Control Register bit 0.15)

Note: At the completion of a reset (either hardware, power-on, or software), the ICS1893AF, Rev. C sets all registers to their default values.

5.1.2.1 Hardware Reset

Entering Hardware Reset

Holding the active-low RESETn pin low for a minimum of five REF_IN clock cycles initiates a hardware reset (that is, the ICS1893AF, Rev. C enters the reset state). During reset, the ICS1893AF, Rev. C executes the steps listed in Section 5.1.1.1, “Entering Reset”.

Exiting Hardware Reset

After the signal on the RESETn pin transitions from a low to a high state, the ICS1893AF, Rev. C completes in 640 ns (that is, in 16 REF_IN clocks) steps 1 through 5, listed in Section 5.1.1.2, “Exiting Reset”. After the first five steps are completed, the Serial Management Port is ready for normal operations, but this action does not signify the end of the reset cycle. The reset cycle completes when the transmit clock (TXCLK) and receive clock (RXCLK) are available, which is typically 53 ms after the RESETn pin goes high. [For details on this transition, see Section 10.5.16, “Reset: Hardware Reset and Power-Down”.]

Note:

1. The MAC/Repeater Interface is not available for use until the TXCLK and RXCLK are valid.
2. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset.

5.1.2.2 Power-On Reset

Entering Power-On Reset

When power is applied to the ICS1893AF, Rev. C, it waits until the potential between VDD and VSS achieves a minimum voltage before entering reset and executing the steps listed in Section 5.1.1.1, “Entering Reset”. After entering reset from a power-on condition, the ICS1893AF, Rev. C remains in reset for approximately 20 µs. (For details on this transition, see Section 10.5.15, “Reset: Power-On Reset”.)

Exiting Power-On Reset

The ICS1893AF, Rev. C automatically exits reset and performs the same steps as for a hardware reset. (See Section 5.1.1.2, “Exiting Reset”.)

Note: The only difference between a hardware reset and a power-on reset is that during a power-on reset, the ICS1893AF, Rev. C isolates its RESETn input pin. All other functionality is the same. As with a hardware reset, Control Register bit 0.15 does not represent the status of a power-on reset.

5.1.2.3 Software Reset

Entering Software Reset

Initiation of a software reset occurs when a management entity writes a logic one to Control Register bit 0.15. When this write occurs, the ICS1893AF, Rev. C enters the reset state for two REF_IN clock cycles.

Note: Entering a software reset is nearly identical to entering a hardware reset or a power-on reset, except that during a software-initiated reset, the ICS1893AF, Rev. C does not enter the power-down state.

Exiting Software Reset

At the completion of a reset (either hardware, power-on, or software), the ICS1893AF, Rev. C sets all registers to their default values. This action automatically clears (that is, sets equal to logic zero) Control Register bit 0.15, the software reset bit. Therefore, for a software reset (only), bit 0.15 is a self-clearing bit that indicates the completion of the reset process.

Note:

1. The RESETn pin is active low but Control Register bit 0.15 is active high.
2. Exiting a software reset is nearly identical to exiting a hardware reset or a power-on reset, except that upon exiting a software-initiated reset, the ICS1893AF, Rev. C does not re-latch its Serial Management Port Address into the Extended Control Register. [For information on the Serial Management Port Address, see Section 8.11.3, “PHY Address (bits 16.10:6)”.]
3. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset. During a hardware or power-on reset, Control Register bit 0.15 does not get set to logic one. As a result, this bit 0.15 cannot be used to indicate the completion of the reset process for hardware or power-on resets.

5.2 Power-Down Operations

The ICS1893AF, Rev. C enters the power-down state whenever either (1) the RESETn pin is low or (2) Control Register bit 0.11 (the Power-Down bit) is logic one. In the power-down state, the ICS1893AF, Rev. C disables all internal functions and drives all MAC/Repeater Interface output pins to logic zero except for those that support the MII Serial Management Port. In addition, the ICS1893AF, Rev. C tri-states its Twisted-Pair Transmit pins (TP_TXP and TP_TXN) to achieve an additional reduction in power.

There is one significant difference between entering the power-down state by setting Control Register bit 0.11 as opposed to entering the power-down state during a reset. When the ICS1893AF, Rev. C enters the power-down state:

- By setting Control Register bit 0.11, the ICS1893AF, Rev. C maintains the value of all Management Register bits except for the latching low (LL), latching high (LH), and latching maximum (LMX) status bits. Instead, these LL, LH, and LMX Management Register bits are re-initialized to their default values.
- During a reset, the ICS1893AF, Rev. C sets all of its Management Register bits to their default values. It does not maintain the state of any Management Register bit.

For more information on power-down operations, see the following:

- Section 8.14, “Register 19: Extended Control Register 2”
- Section 10.4, “DC Operating Characteristics”, which has tables that specify the ICS1893AF, Rev. C power consumption while in the power-down state

5.3 Automatic Power-Saving Operations

The ICS1893AF, Rev. C has power-saving features that automatically minimize its total power consumption while it is operating. Table 5-1 lists the ICS1893AF, Rev. C automatic power-saving features for the various modes.

Table 5-1. Automatic Power-Saving Features, 10Base-T and 100Base-TX Modes

Power-Saving Feature	Mode for ICS1893AF, Rev. C	
	10Base-T Mode	**100Base-TX Mode**
Disable Internal Modules	In 10Base-T mode, the ICS1893AF, Rev. C disables all its internal 100Base-TX modules.	In 100Base-TX mode, the ICS1893AF, Rev. C disables all its internal 10Base-T modules.
STA Control of Automatic Power-Saving Features	When an STA sets the state of the ICS1893AF, Rev. C Extended Control Register 2, bit 19.0 to logic: • Zero, the 100Base-TX modules always remain enabled, even during 10Base-T operations. • One, the ICS1893AF, Rev. C automatically disables 100Base-TX modules while the ICS1893AF, Rev. C is operating in 10Base-T mode.	When an STA sets the state of the ICS1893AF, Rev. C Extended Control Register 2, bit 19.1 to logic: • Zero, the 10Base-T modules always remain enabled, even during 100Base-TX operations. • One, the ICS1893AF, Rev. C automatically disables 10Base-T modules while the ICS1893AF, Rev. C is operating in 100Base-TX mode.

5.4 Auto-Negotiation Operations

The ICS1893AF, Rev. C has an Auto-Negotiation sublayer and provides a Control Register bit (bit 0.12) to determine whether its Auto-Negotiation sublayer is enabled or disabled.

When enabled, the ICS1893AF, Rev. C Auto-Negotiation sublayer exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode it has in common with its remote link partner. For example, if the ICS1893AF, Rev. C supports 100Base-TX and 10Base-T modes – but its link partner supports 100Base-TX and 100Base-T4 modes – the two devices automatically select 100Base-TX as the highest-performance common operating mode. For details regarding initialization and control of the auto-negotiation process, see Section 7.2, “Functional Block: Auto-Negotiation”.

5.5 100Base-TX Operations

The ICS1893AF, Rev. C 100Base-TX mode provides 100Base-TX physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 100Base-TX mode, the ICS1893AF, Rev. C is a 100M translator between a MAC and the physical transmission medium. As such, the ICS1893AF, Rev. C has two interfaces, both of which are fully configurable: one to the MAC/repeater and one to the Link Segment. In 100Base-TX mode, the ICS1893AF, Rev. C provides the following functions:

- Data conversion from both parallel-to-serial and serial-to-parallel formats
- Data encoding/decoding (4B/5B, NRZ/NRZI, and MLT-3)
- Data scrambling/descrambling
- Data transmission/reception over a twisted-pair medium

To accurately transmit and receive data, the ICS1893AF, Rev. C employs DSP-based wave shaping, adaptive equalization, and baseline wander correction. In addition, in 100Base-TX mode, the ICS1893AF, Rev. C provides a variety of control and status means to assist with Link Segment management. For more information on 100Base-TX, see Section 7.4, “Functional Block: 100Base-TX TP-PMD Operations”.

5.6 10Base-T Operations

The ICS1893AF, Rev. C 10Base-T mode provides 10Base-T physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 10Base-T mode, the ICS1893AF, Rev. C is a 10M translator between a MAC/repeater and the physical transmission medium. In 10Base-T mode, the ICS1893AF, Rev. C provides the following functions:

- Data conversion from both parallel-to-serial and serial-to-parallel formats
- Manchester data encoding/decoding
- Data transmission/reception over a twisted-pair medium

5.7 Half-Duplex and Full-Duplex Operations

The ICS1893AF, Rev. C supports half-duplex and full-duplex operations for both 10Base-T and 100Base-TX applications. Full-duplex operation allows simultaneous transmission and reception of data, which effectively doubles the Link Segment throughput to either 20 Mbps (for 10Base-T operations) or 200 Mbps (for 100Base-TX operations).

As per the ISO/IEC standard, full-duplex operations differ slightly from half-duplex operations. These differences are necessary, as during full-duplex operations a PHY actively uses both its transmit and receive data paths simultaneously.

- In 10Base-T full-duplex operations, the ICS1893AF, Rev. C disables its loopback function (that is, it does not automatically loop back data from its transmitter to its receiver) and disables its SQE Test function.
- In both 10Base-T and 100Base-TX full-duplex operations, the ICS1893AF, Rev. C asserts its CRS signal only in response to receive activity while its COL signal always remains inactive.

For more information on half-duplex and full-duplex operations, see the following sections:

- Section 8.2, “Register 0: Control Register”
- Section 8.2.8, “Duplex Mode (bit 0.8)”
- Section 8.3, “Register 1: Status Register”
- Section 8.6, “Register 4: Auto-Negotiation Register”

Chapter 6 Interface Overviews

The ICS1893AF, Rev. C MAC/Repeater Interface is fully configurable, thereby allowing it to accommodate many different applications.

This chapter includes overviews of the following MAC/repeater-to-PHY interfaces:

- Section 6.1, “MII Data Interface”
- Section 6.2, “Serial Management Interface”
- Section 6.3, “Twisted-Pair Interface”
- Section 6.4, “Clock Reference Interface”
- Section 6.5, “Status Interface”

6.1 MII Data Interface

The ICS1893AF's MAC Interface is the Medium Independent Interface (MII) operating at either 10 Mbps or 100 Mbps. The ICS1893AF MAC/Repeater Interface is configured for the MII Data Interface mode, data is transferred between the PHY and the MAC as framed, 4-bit parallel nibbles. In addition, the interface also provides status and control signals to synchronize the transfers.

The ICS1893AF provides a full complement of the ISO/IEC-specified MII signals. Its MII has both a transmit and a receive data path to synchronously exchange 4 bits of data (that is, nibbles).

- The ICS1893AF's MII transmit data path includes the following:
  - A data nibble, TXD[3:0]
  - A transmit data clock to synchronize transfers, TXCLK
  - A transmit enable signal, TXEN
  - A transmit error signal, TXER
- The ICS1893AF's MII receive data path includes the following:
  - A separate data nibble, RXD[3:0]
  - A receive data clock to synchronize transfers, RXCLK
  - A receive data valid signal, RXDV
  - A receive error signal, RXER

Both the MII transmit clock and the MII receive clock are provided to the MAC/Reconciliation sublayer by the ICS1893AF (that is, the ICS1893AF sources the TXCLK and RXCLK signals to the MAC/repeater).

Clause 22 also defines as part of the MII a Carrier Sense signal (CRS) and a Collision Detect signal (COL). The ICS1893AF is fully compliant with these definitions and sources both of these signals to the MAC/repeater. When operating in:

- Half-duplex mode, the ICS1893AF asserts the Carrier Sense signal when data is being either transmitted or received. While operating in half-duplex mode, the ICS1893AF also asserts its Collision Detect signal to indicate that data is being received while a transmission is in progress.
- Full-duplex mode, the ICS1893AF asserts the Carrier Sense signal only when receiving data and forces the Collision Detect signal to remain inactive.

As mentioned in Section 5.1.1.3, "Hot Insertion", the ICS1893AF design allows hot insertion of its MII. That is, it is possible to connect its MII to a MAC when power is already applied to the MAC. To support this functionality, the ICS1893AF isolates its MII signals and tri-states the signals on all Twisted-Pair Transmit pins (TP_TXP and TP_TXN) during a power-on reset. Upon completion of the reset process, the ICS1893AF enables its MII and enables its Twisted-Pair Transmit signals.