Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of "Quality Parts,Customers Priority,Honest Operation,and Considerate Service",our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

3.3-V 10Base-T/100Base-TX Integrated PHYceiver™

General

The ICS1893CF is a low-power, physical-layer device (PHY) that supports the ISO/IEC 10Base-T and 100Base-TX Carrier-Sense Multiple Access/Collision Detection (CSMA/CD) Ethernet standards, ISO/IEC 8802-3.

The ICS1893CF is intended for MII, Node applications that require the Auto-MDIX feature that automatically corrects crossover errors in plant wiring.

The ICS1893CF incorporates Digital-Signal Processing (DSP) control in its Physical-Medium Dependent (PMD) sub layer. As a result, it can transmit and receive data on unshielded twisted-pair (UTP) category 5 cables with attenuation in excess of 24 dB at 100MHz. With this ICS-patented technology, the ICS1893CF can virtually eliminate errors from killer packets.

The ICS1893CF provides a Serial-Management Interface for exchanging command and status information with a Station-Management (STA) entity. The ICS1893CF Media-Dependent Interface (MDI) can be configured to provide either half- or full-duplex operation at data rates of 10 Mb/s or 100Mb/s.

The ICS1893CF is available in a 300-mil 48-lead SSOP package. The ICS1893CF shares the same proven performance circuitry with the ICS1893BF and is a pin-for-pin replacement of the 1893BF.

Applications: NIC cards, PC motherboards, switches, routers, DSL and cable modems, game machines, printers, network connected appliances, and industrial equipment.

Features

- Supports category 5 cables with attenuation in excess of 24dB at 100 MHz.
- Single-chip, fully integrated PHY provides PCS, PMA, PMD, and AUTONEG sub layers functions of IEEE standard.
- 10Base-T and 100Base-TX IEEE 8802.3 compliant
- Single 3.3V power supply
- Highly configurable, supports:
  - Media Independent Interface (MII)
  - Auto-Negotiation with Parallel detection
  - Node applications, managed or unmanaged
  - 10M or 100M full and half-duplex modes
  - Loopback mode for Diagnostic Functions
  - Auto-MDI/MDIX crossover correction
- Low-power CMOS (typically 400 mW)
- Power-Down mode typically 21mW
- Clock and crystal supported
- Fully integrated, DSP-based PMD includes:
  - Adaptive equalization and baseline-wander correction
  - Transmit wave shaping and stream cipher scrambler
  - MLT-3 encoder and NRZ/NRZI encoder
- Small footprint 48-pin 300 mil. SSOP package
- Also available in small footprint 56-pin 8x8 MLF2 package
- Available in Industrial Temp and Lead Free

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

ICS1893CF Block Diagram
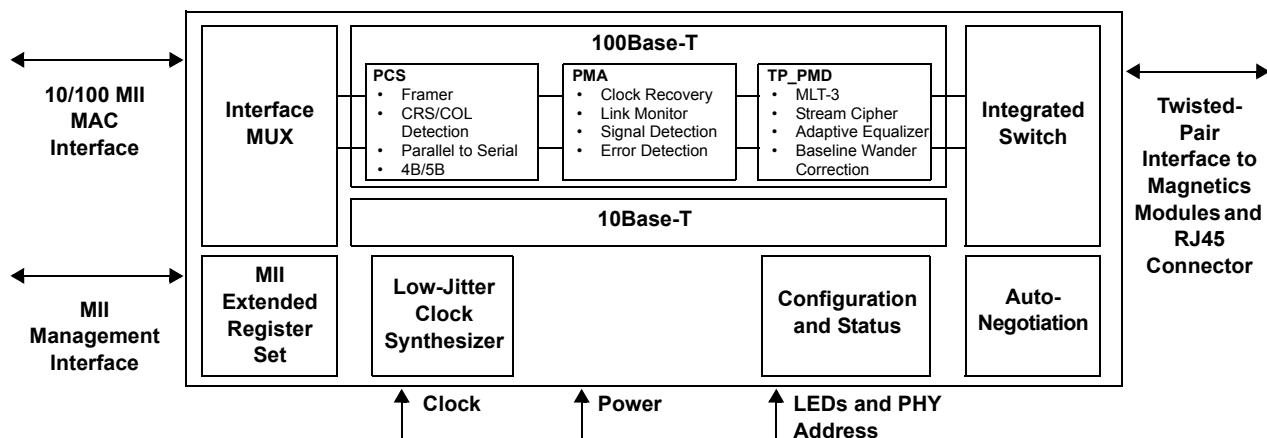
Revision History

- Initial preliminary release of this document, Rev A, dated July 10, 2006.
- Rev B – remove all references to ICS1893CK; removed package drawing and ordering info.
- Rev C – added CK package and ordering information back to datasheet; removed TOC.
- Rev E – changed resistor values in table 9.3 and on Figure 9-1, "ICS1893CF 10TCSR and 100TCSR".
- Rev G – added top side marking for 1893CKILF.
- Rev H – updated hex numerology in table 7-9.
- Rev J, 8/11/09 – added EOL note for ordering information per PDN U-09-01.

Chapter 1 Abbreviations and Acronyms

Table 1-1 lists and interprets the abbreviations and acronyms used throughout this data sheet.

Table 1-1. Abbreviations and Acronyms

Abbreviation / Acronym	Interpretation
4B/5B	4-Bit / 5-Bit Encoding/Decoding
ANSI	American National Standards Institute
CMOS	complimentary metal-oxide semiconductor
CSMA/CD	Carrier Sense Multiple Access with Collision Detection
CW	Command Override Write
DSP	digital signal processing
ESD	End-of-Stream Delimiter
FDDI	Fiber Distributed Data Interface
FLL	frequency-locked loop
FLP	Fast Link Pulse
IDL	A 'dead' time on the link following a 10Base-T packet, not to be confused with idle
IEC	International Electrotechnical Commission
IEEE	Institute of Electrical and Electronic Engineers
ISO	International Standards Organization
LH	Latching High
LL	Latching Low
LMX	Latching Maximum
MAC	Media Access Control
Max.	maximum
Mbps	Megabits per second
MDI	Media Dependent Interface
MDIX	Media Independent Interface Crossed
MF	Management Frame
MII	Media Independent Interface
Min.	minimum
MLT-3	Multi-Level Transition Encoding (3 Levels)
N/A	Not Applicable
NLP	Normal Link Pulse
No.	Number
NRZ	Not Return to Zero
NRZI	Not Return to Zero, Invert on one

Table 1-1.   Abbreviations and Acronyms (*Continued*)

Abbreviation / Acronym	Interpretation
OSI	Open Systems Interconnection
OUI	Organizationally Unique Identifier
PCS	Physical Coding sublayer
PHY	physical-layer device The ICS1893CF is a physical-layer device, also referred to as a 'PHY' or 'PHYceiver'. (The ICS1890 is also a physical-layer device.)
PLL	phase-locked loop
PMA	Physical Medium Attachment
PMD	Physical Medium Dependent
ppm	parts per million
RO	read only
R/W	read/write
R/W0	read/write zero
SC	self-clearing
SF	Special Functions
SFD	Start-of-Frame Delimiter

SI	Stream Interface, Serial Interface, or Symbol Interface.
	With reference to the MII/SI pin, the acronym 'SI' has multiple meanings.
	• Generically, SI means 'Stream Interface', and is documented as such in this data sheet.
	• However, when the MAC Interface is configured for:
	  – 10M operations, SI is an acronym for 'Serial Interface'.
	  – 100M operations, SI is an acronym for 'Symbol Interface'.

SQE	Signal Quality Error
SSD	Start-of-Stream Delimiter
SSOP	Small Shrink Outline Package
STA	Station Management Entity
STP	shielded twisted pair
TAF	Technology Ability Field
TP-PMD	Twisted-Pair Physical Layer Medium Dependent
Typ.	typical
UTP	unshielded twisted pair

August, 2009

Chapter 2   Conventions and Nomenclature

Table 2-1 lists and explains the conventions and nomenclature used throughout this data sheet.

Table 2-1.   Conventions and Nomenclature

Item	Convention / Nomenclature
Bits	• A bit in a register is identified using the format 'register.bit'. For example, bit 0.15 is bit 15 of register 0. • When a colon is used with bits, it indicates the range of bits. For example, bits 1.15:11 are bits 15, 14, 13, 12, and 11 of register 1. • For a range of bits, the order is always from the most-significant bit to the least-significant bit.
Code groups	Within this table, see the item 'Symbols'
Colon (:)	Within this table, see these items: • 'Bits' • 'Pin (or signal) names'

Numbers	• As a default, all numbers use the decimal system (that is, base 10) unless followed by a lowercase letter. A string of numbers followed by a lowercase letter:
	  – A 'b' represents a binary (base 2) number
	  – An 'h' represents a hexadecimal (base 16) number
	  – An 'o' represents an octal (base 8) number
	• All numerical references to registers use decimal notation (and not hexadecimal).

Pin (or signal) names	• All pin or signal names are provided in capital letters.
	• A pin name that includes a forward slash '/' is a multi-function, configuration pin. These pins provide the ability to select between two ICS1893CF functions. The name provided:
	  – Before the '/' indicates the pin name and function when the signal level on the pin is logic zero.
	  – After the '/' indicates the pin name and function when the signal level on the pin is logic one.
	For example, the HW/SW pin selects between Hardware (HW) mode and Software (SW) mode. When the signal level on the HW/SW pin is logic:
	  – Zero, the ICS1893CF Hardware mode is selected.
	  – One, the ICS1893CF Software mode is selected.
	• An 'n' appended to the end of a pin name or signal name (such as RESETn) indicates an active-low operation.
	• When a colon is used with pin or signal names, it indicates a range. For example, TXD[3:0] represents pins/signals TXD3, TXD2, TXD1, and TXD0.
	• When pin name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the pin name abbreviation.

Registers	• A bit in a register is identified using the format 'register.bit'. For example, bit 0.15 is bit 15 of register 0. • All numerical references to registers use decimal notation (and not hexadecimal). • When register name abbreviations are spelled out, words in parentheses indicate additional description that is not part of the register name abbreviation.

Table 2-1. Conventions and Nomenclature (*Continued*)

Item	Convention / Nomenclature
Signal references	• When referring to signals, the terms: – 'FALSE', 'low', or 'zero' represent signals that are logic zero. – 'TRUE', 'high', or 'one' represent signals that are logic one. • Chapter 9, "DC and AC Operating Conditions" defines the electrical specifications for 'logic zero' and 'logic one' signals.
Symbols	• In this data sheet, code group names are referred to as 'symbols' and they are shown between '/' (slashes). For example, the symbol /J/ represents the first half of the Start-of-Stream Delimiter (SSD1). • Symbol sequences are shown in succession. For example, /I/J/K/ represents an IDLE followed by the SSD.
Terms: 'set', 'active', 'asserted',	The terms 'set', 'active', and 'asserted' are synonymous. They do not necessarily infer logic one. (For example, an active-low signal can be set to logic zero.)
Terms: 'cleared', 'de-asserted', 'inactive'	The terms 'cleared', 'inactive', and 'de-asserted' are synonymous. They do not necessarily infer logic zero.
Terms: 'twisted-pair receiver'	In reference to the ICS1893CF, the term 'Twisted-Pair Receiver' refers to the set of Twisted-Pair Receive output pins (TP_RXP and TP_RXN).
Terms: 'twisted-pair transmitter'	In reference to the ICS1893CF, the term 'Twisted-Pair Transmitter' refers to the set of Twisted-Pair Transmit output pins (TP_TXP and TP_TXN).

Chapter 3   Overview of the ICS1893CF

The ICS1893CF is a stream processor. During data transmission, it accepts sequential nibbles from its MAC (Media Access Control) converts them into a serial bit stream, encodes them, and transmits them over the medium through an external isolation transformer. When receiving data, the ICS1893CF converts and decodes a serial bit stream (acquired from an isolation transformer that interfaces with the medium) into sequential nibbles. It subsequently presents these nibbles to its MAC Interface.

The ICS1893CF implements the OSI model's physical layer, consisting of the following, as defined by the ISO/IEC 8802-3 standard:

• Physical Coding sublayer (PCS)
• Physical Medium Attachment sublayer (PMA)
• Physical Medium Dependent sublayer (PMD)
• Auto-Negotiation sublayer

The ICS1893CF is transparent to the next layer of the OSI model, the link layer. The link layer has two sublayers: the Logical Link Control sublayer and the MAC sublayer. The ICS1893CF can interface directly to the MAC.

The ICS1893CF transmits framed packets acquired from its MAC Interface and receives encapsulated packets from another PHY, which it translates and presents to its MAC Interface.

Note: As per the ISO/IEC standard, the ICS1893CF does not affect, nor is it affected by, the underlying structure of the MAC frame it is conveying.

3.1   100Base-TX Operation

During 100Base-TX data transmission, the ICS1893CF accepts packets from a MAC and inserts Start-of-Stream Delimiters (SSDs) and End-of-Stream Delimiters (ESDs) into the data stream. The ICS1893CF encapsulates each MAC frame, including the preamble, with an SSD and an ESD. As per the ISO/IEC Standard, the ICS1893CF replaces the first octet of each MAC preamble with an SSD and appends an ESD to the end of each MAC frame.

When receiving data from the medium, the ICS1893CF removes each SSD and replaces it with the pre-defined preamble pattern before presenting the nibbles to its MAC Interface. When the ICS1893CF encounters an ESD in the received data stream, signifying the end of the frame, it ends the presentation of nibbles to its MAC Interface. Therefore, the local MAC receives an unaltered copy of the transmitted frame sent by the remote MAC.

During periods when MAC frames are being neither transmitted nor received, the ICS1893CF signals and detects the IDLE condition on the Link Segment. In the 100Base-TX mode, the ICS1893CF transmit channel sends a continuous stream of scrambled ones to signify the IDLE condition. Similarly, the ICS1893CF receive channel continually monitors its data stream and looks for a pattern of scrambled ones. The results of this signaling and monitoring provide the ICS1893CF with the means to establish the integrity of the Link Segment between itself and its remote link partner and inform its Station Management Entity (STA) of the link status.

For 100M data transmission, the ICS1893CF MAC Interface is configured to provide a 100M Media Independent Interface (MII).

3.2   10Base-T Operation

During 10Base-T data transmission, the ICS1893CF inserts only the IDL delimiter into the data stream. The ICS1893CF appends the IDL delimiter to the end of each MAC frame. However, since the 10Base-T preamble already has a Start-of-Frame delimiter (SFD), it is not required that the ICS1893CF insert an SSD-like delimiter.

When receiving data from the medium (such as a twisted-pair cable), the ICS1893CF uses the preamble to synchronize its receive clock. When the ICS1893CF receive clock establishes lock, it presents the preamble nibbles to its MAC Interface. The 10M MAC Interface uses the standard MII Interface.

In 10M operations, during periods when MAC frames are being neither transmitted nor received, the ICS1893CF signals and detects Normal Link Pulses. This action allows the integrity of the Link Segment with the remote link partner to be established and then reported to the ICS1893CF's STA.

Chapter 4   Operating Modes Overview

The ICS1893CF operating modes are typically controlled from software.

The ICS1893CF register bits are accessible through a standard MII (Media Independent Interface) Serial Management Port.

The ICS1893CF is configured to support the MAC Interface as a 10M MII or a 100M MII. The protocol on the Medium Dependent Interface (MDI) can be configured to support either 10M or 100M operations in either half-duplex or full-duplex modes.

The ICS1893CF is fully compliant with the ISO/IEC 8802-3 standard, as it pertains to both 10Base-T and 100Base-TX operations. The feature-rich ICS1893CF allows easy migration from 10-Mbps to 100-Mbps operations as well as from systems that require support of both 10M and 100M links.

This chapter is an overview of the following ICS1893CF modes of operation:

- Section 4.1, "Reset Operations"
- Section 4.2, "Power-Down Operations"
- Section 4.3, "Automatic Power-Saving Operations"
- Section 4.4, "Auto-Negotiation Operations"
- Section 4.5, "100Base-TX Operations"
- Section 4.6, "10Base-T Operations"
- Section 4.7, "Half-Duplex and Full-Duplex Operations"
- Section 4.8, "Auto-MDI/MDIX Crossover"

4.1   Reset Operations

This section first discusses reset operations in general and then specific ways in which the ICS1893CF can be configured for various reset options.

4.1.1   General Reset Operations

The following reset operations apply to all the specific ways in which the ICS1893CF can be reset, which are discussed in Section 4.1.2, "Specific Reset Operations".

4.1.1.1   Entering Reset

When the ICS1893CF enters a reset condition (either through hardware, power-on reset, or software), it does the following:

1.   Isolates the MAC Interface input pins
2.   Drives all MAC Interface output pins low
3.   Tri-states the signals on its Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
4.   Initializes all its internal modules and state machines to their default states
5.   Enters the power-down state
6.   Initializes all internal latching low (LL), latching high (LH), and latching maximum (LMX) Management Register bits to their default values

4.1.1.2   Exiting Reset

When the ICS1893CF exits a reset condition, it does the following:

1.   Exits the power-down state
2.   Latches the Serial Management Port Address of the ICS1893CF into the Extended Control Register, bits 16.10:6. [See Section 7.11.3, "PHY Address (bits 16.10:6)".]
3.   Enables all its internal modules and state machines
4.   Sets all Management Register bits to their default values
5.   Enables the Twisted-Pair Transmit pins (TP_TXP and TP_TXN)
6.   Resynchronizes both its Transmit and Receive Phase-Locked Loops, which provide its transmit clock (TXCLK) and receive clock (RXCLK)
7.   Releases all MAC Interface pins, which takes a maximum of 640 ns after the reset condition is removed

4.1.1.3   Hot Insertion

As with the ICS189X products, the ICS1893CF reset design supports 'hot insertion' of its MII. (That is, the ICS1893CF can connect its MAC Interface to a MAC while power is already applied to the MAC.)

4.1.2   Specific Reset Operations

This section discusses the following specific ways that the ICS1893CF can be reset:

- Hardware reset (using the RESETn pin)
- Power-on reset (applying power to the ICS1893CF)
- Software reset (using Control Register bit 0.15)

Note: At the completion of a reset (either hardware, power-on, or software), the ICS1893CF sets all registers to their default values.

4.1.2.1   Hardware Reset

Entering Hardware Reset

Holding the active-low RESETn pin low for a minimum of five REF_IN clock cycles initiates a hardware reset (that is, the ICS1893CF enters the reset state). During reset, the ICS1893CF executes the steps listed in Section 4.1.1.1, "Entering Reset".

Exiting Hardware Reset

After the signal on the RESETn pin transitions from a low to a high state, the ICS1893CF completes in 640 ns (that is, in 16 REF_IN clocks) steps 1 through 5, listed in Section 4.1.1.2, "Exiting Reset". After the first five steps are completed, the Serial Management Port is ready for normal operations, but this action does not signify the end of the reset cycle. The reset cycle completes when the transmit clock (TXCLK) and receive clock (RXCLK) are available, which is typically 53 ms after the RESETn pin goes high. [For details on this transition, see Section 9.5.16, "Reset: Hardware Reset and Power-Down".]

Note:

1. The MAC Interface is not available for use until the TXCLK and RXCLK are valid.
2. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset.

4.1.2.2   Power-On Reset

Entering Power-On Reset

When power is applied to the ICS1893CF, it waits until the potential between VDD and VSS achieves a minimum voltage before entering reset and executing the steps listed in Section 4.1.1.1, "Entering Reset". After entering reset from a power-on condition, the ICS1893CF remains in reset for approximately 20 μs. (For details on this transition, see Section 9.5.15, "Reset: Power-On Reset".)

Exiting Power-On Reset

The ICS1893CF automatically exits reset and performs the same steps as for a hardware reset. (See Section 4.1.1.2, "Exiting Reset".)

Note: The only difference between a hardware reset and a power-on reset is that during a power-on reset, the ICS1893CF isolates its RESETn input pin. All other functionality is the same. As with a hardware reset, Control Register bit 0.15 does not represent the status of a power-on reset.

4.1.2.3   Software Reset

Entering Software Reset

Initiation of a software reset occurs when a management entity writes a logic one to Control Register bit 0.15. When this write occurs, the ICS1893CF enters the reset state for two REF_IN clock cycles.

Note: Entering a software reset is nearly identical to entering a hardware reset or a power-on reset, except that during a software-initiated reset, the ICS1893CF does not enter the power-down state.

Exiting Software Reset

At the completion of a reset (either hardware, power-on, or software), the ICS1893CF sets all registers to their default values. This action automatically clears (that is, sets equal to logic zero) Control Register bit 0.15, the software reset bit. Therefore, for a software reset (only), bit 0.15 is a self-clearing bit that indicates the completion of the reset process.

Note:

1. The RESETn pin is active low but Control Register bit 0.15 is active high.

2. Exiting a software reset is nearly identical to exiting a hardware reset or a power-on reset, except that upon exiting a software-initiated reset, the ICS1893CF does not re-latch its Serial Management Port Address into the Extended Control Register. [For information on the Serial Management Port Address, see Section 7.11.3, "PHY Address (bits 16.10:6)".]

3. The Control Register bit 0.15 does not represent the status of a hardware reset. It is a self-clearing bit that is used to initiate a software reset. During a hardware or power-on reset, Control Register bit 0.15 does not get set to logic one. As a result, this bit 0.15 cannot be used to indicate the completion of the reset process for hardware or power-on resets.

4.2   Power-Down Operations

The ICS1893CF enters the power-down state whenever either (1) the RESETn pin is low or (2) Control Register bit 0.11 (the Power-Down bit) is logic one. In the power-down state, the ICS1893CF disables all internal functions and drives all MAC Interface output pins to logic zero except for those that support the MII Serial Management Port. In addition, the ICS1893CF tri-states its Twisted-Pair Transmit pins (TP_TXP and TP_TXN) to achieve an additional reduction in power.

There is one significant difference between entering the power-down state by setting Control Register bit 0.11 as opposed to entering the power-down state during a reset. When the ICS1893CF enters the power-down state:

- By setting Control Register bit 0.11, the ICS1893CF maintains the value of all Management Register bits except for the latching low (LL), latching high (LH), and latching maximum (LMX) status bits. Instead, these LL, LH, and LMX Management Register bits are re-initialized to their default values.

- During a reset, the ICS1893CF sets all of its Management Register bits to their default values. It does not maintain the state of any Management Register bit.

For more information on power-down operations, see the following:

- Section 7.14, "Register 19: Extended Control Register 2"

- Section 9.4, "DC Operating Characteristics", which has tables that specify the ICS1893CF power consumption while in the power-down state

4.3   Automatic Power-Saving Operations

The ICS1893CF has power-saving features that automatically minimize its total power consumption while it is operating. Table 4-1 lists the ICS1893CF automatic power-saving features for the various modes.

Table 4-1.   Automatic Power-Saving Features, 10Base-T and 100Base-TX Modes

Power-Saving Feature	Mode for ICS1893CF	
	10Base-T Mode	**100Base-TX Mode**
Disable Internal Modules	In 10Base-T mode, the ICS1893CF disables all its internal 100Base-TX modules.	In 100Base-TX mode, the ICS1893CF disables all its internal 10Base-T modules.
STA Control of Automatic Power-Saving Features	When an STA sets the state of the ICS1893CF Extended Control Register 2, bit 19.0 to logic: • Zero, the 100Base-TX modules always remain enabled, even during 10Base-T operations. • One, the ICS1893CF automatically disables 100Base-TX modules while the ICS1893CF is operating in 10Base-T mode.	When an STA sets the state of the ICS1893CF Extended Control Register 2, bit 19.1 to logic: • Zero, the 10Base-T modules always remain enabled, even during 100Base-TX operations. • One, the ICS1893CF automatically disables 10Base-T modules while the ICS1893CF is operating in 100Base-TX mode.

4.4   Auto-Negotiation Operations

The ICS1893CF has an Auto-Negotiation sublayer and provides a Control Register bit (bit 0.12) to determine whether its Auto-Negotiation sublayer is enabled or disabled.

When enabled, the ICS1893CF Auto-Negotiation sublayer exchanges technology capability data with its remote link partner and automatically selects the highest-performance operating mode it has in common with its remote link partner. For example, if the ICS1893CF supports 100Base-TX and 10Base-T modes – but its link partner supports 100Base-TX and 100Base-T4 modes – the two devices automatically select 100Base-TX as the highest-performance common operating mode. For details regarding initialization and control of the auto-negotiation process, see Section 6.2, "Functional Block: Auto-Negotiation".

4.5   100Base-TX Operations

The ICS1893CF 100Base-TX mode provides 100Base-TX physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 100Base-TX mode, the ICS1893CF is a 100M translator between a MAC and the physical transmission medium. As such, the ICS1893CF has two interfaces, both of which are fully configurable: one to the MAC and one to the Link Segment. In 100Base-TX mode, the ICS1893CF provides the following functions:

• Data conversion from both parallel-to-serial and serial-to-parallel formats

• Data encoding/decoding (4B/5B, NRZ/NRZI, and MLT-3)

• Data scrambling/descrambling

• Data transmission/reception over a twisted-pair medium

To accurately transmit and receive data, the ICS1893CF employs DSP-based wave shaping, adaptive equalization, and baseline wander correction. In addition, in 100Base-TX mode, the ICS1893CF provides a variety of control and status means to assist with Link Segment management. For more information on 100Base-TX, see Section 6.4, "Functional Block: 100Base-TX TP-PMD Operations".

4.6   10Base-T Operations

The ICS1893CF 10Base-T mode provides 10Base-T physical layer (PHY) services as defined in the ISO/IEC 8802-3 standard. In the 10Base-T mode, the ICS1893CF is a 10M translator between a MAC and the physical transmission medium. In 10Base-T mode, the ICS1893CF provides the following functions:

• Data conversion from both parallel-to-serial and serial-to-parallel formats

• Manchester data encoding/decoding

• Data transmission/reception over a twisted-pair medium

4.7   Half-Duplex and Full-Duplex Operations

The ICS1893CF supports half-duplex and full-duplex operations for both 10Base-T and 100Base-TX applications. Full-duplex operation allows simultaneous transmission and reception of data, which effectively doubles the Link Segment throughput to either 20 Mbps (for 10Base-T operations) or 200 Mbps (for 100Base-TX operations).

As per the ISO/IEC standard, full-duplex operations differ slightly from half-duplex operations. These differences are necessary, as during full-duplex operations a PHY actively uses both its transmit and receive data paths simultaneously.

• In 10Base-T full-duplex operations, the ICS1893CF disables its loopback function (that is, it does not automatically loop back data from its transmitter to its receiver) and disables its SQE Test function.

• In both 10Base-T and 100Base-TX full-duplex operations, the ICS1893CF asserts its CRS signal only in response to receive activity while its COL signal always remains inactive.

For more information on half-duplex and full-duplex operations, see the following sections:

• Section 7.2, "Register 0: Control Register"

• Section 7.2.8, "Duplex Mode (bit 0.8)"

• Section 7.3, "Register 1: Status Register"

• Section 7.6, "Register 4: Auto-Negotiation Register"

4.8   Auto-MDI/MDIX Crossover (New)

The ICS1893CF includes the auto-MDI/MDIX crossover feature. In a typical CAT 5 Ethernet installation the transmit twisted pair signal pins of the RJ45 connector are crossed over in the CAT 5 wiring to the partners receive twisted pair signal pins and receive twisted pair to the partners transmit twisted pair. This is usually accomplished in the wiring plant. Hubs generally wire the RJ45 connector crossed to accomplish the crossover. Two types of CAT 5 cables (straight and crossed) are available to achieve the correct connection. The Auto-MDI/MDIX feature automatically corrects for miss-wired installations by automatically swapping transmit and receive signal pairs at the PHY when no link results. Auto-MDI/MDIX is automatic, but may be disabled for test purposes using the AMDIX_EN pin or by writing MDIO register 19 Bits 9:8 in the MDIO register. The Auto-MDI/MDIX function is independent of Auto-Negotiation and preceeds Auto-Negotiation when enabled.

Chapter 5   Interface Overviews

The ICS1893CF MAC Interface is fully configurable, thereby allowing it to accommodate many different applications.

This chapter includes overviews of the following MAC-to-PHY interfaces:

- Section 5.1, "MII Data Interface"
- Section 5.2, "Serial Management Interface"
- Section 5.3, "Twisted-Pair Interface"
- Section 5.4, "Clock Reference Interface"
- Section 5.5, "Status Interface"

5.1   MII Data Interface

The ICS1893CF's MAC Interface is the Media Independent Interface (MII) operating at either 10 Mbps or 100 Mbps. The ICS1893CF MAC Interface is configured for the MII Data Interface mode, data is transferred between the PHY and the MAC as framed, 4-bit parallel nibbles. In addition, the interface also provides status and control signals to synchronize the transfers.

The ICS1893CF provides a full complement of the ISO/IEC-specified MII signals. Its MII has both a transmit and a receive data path to synchronously exchange 4 bits of data (that is, nibbles).

- The ICS1893CF's MII transmit data path includes the following:
  - A data nibble, TXD[3:0]
  - A transmit data clock to synchronize transfers, TXCLK
  - A transmit enable signal, TXEN
  - The TXER pin is not available on the ICS1893CF
- The ICS1893CF's MII receive data path includes the following:
  - A separate data nibble, RXD[3:0]
  - A receive data clock to synchronize transfers, RXCLK
  - A receive data valid signal, RXDV

Both the MII transmit clock and the MII receive clock are provided to the MAC/Reconciliation sublayer by the ICS1893CF (that is, the ICS1893CF sources the TXCLK and RXCLK signals to the MAC).

Clause 22 also defines as part of the MII a Carrier Sense signal (CRS) and a Collision Detect signal (COL). The ICS1893CF is fully compliant with these definitions and sources both of these signals to the MAC. When operating in:

- Half-duplex mode, the ICS1893CF asserts the Carrier Sense signal when data is being either transmitted or received. While operating in half-duplex mode, the ICS1893CF also asserts its Collision Detect signal to indicate that data is being received while a transmission is in progress.
- Full-duplex mode, the ICS1893CF asserts the Carrier Sense signal only when receiving data and forces the Collision Detect signal to remain inactive.

As mentioned in Section 4.1.1.3, "Hot Insertion", the ICS1893CF design allows hot insertion of its MII. That is, it is possible to connect its MII to a MAC when power is already applied to the MAC. To support this functionality, the ICS1893CF isolates its MII signals and tri-states the signals on all Twisted-Pair Transmit pins (TP_TXP and TP_TXN) during a power-on reset. Upon completion of the reset process, the ICS1893CF enables its MII and enables its Twisted-Pair Transmit signals.

5.2 Serial Management Interface

The ICS1893CF provides an ISO/IEC compliant, two-wire Serial Management Interface as part of its MAC Interface. This Serial Management Interface is used to exchange control, status, and configuration information between a Station Management entity (STA) and the physical layer device (PHY), that is, the ICS1893CF.

The ISO/IEC standard also specifies a frame structure and protocol for this interface as well as a set of Management Registers that provide the STA with access to a PHY such as the ICS1893CF. A Serial Management Interface is comprised of two signals: a bi-directional data pin (MDIO) along with an associated input pin for a clock (MDC). The clock is used to synchronize all data transfers between the ICS1893CF and the STA.

In addition to the ISO/IEC defined registers, the ICS1893CF provides several extended status and control registers to provide more refined control of the MII and MDI interfaces. For example, the QuickPoll Detailed Status Register provides the ability to acquire the most-important status functions with a single MDIO read.

Note: In the ICS1893CF, the MDIO and MDC pins remain active for all the MAC Interface modes (that is, 10M MII, 100M MII, 100M Symbol, and 10M Serial).

5.3 Twisted-Pair Interface

For the twisted-pair interface, the ICS1893CF uses 1:1 ratio transformers for both transmit and receive.

Better operation results from using a split ground plane through the transformer. In this case:

- The RJ-45 transformer windings must be on the chassis ground plane along with the Bob Smith termination.
- The ICS1893CF system ground plane must include the ICS1893CF-side transformer windings along with the 49.9Ω resistors and the 100 nF capacitor.
- The transformer provides the isolation with one set of windings on one ground plane and another set of windings on the second ground plane.

5.3.1 Twisted-Pair Transmitter

The twisted-pair transmitter driver uses an H-bridge configuration. IDT transformer requirements:

- Turns Ratio 1:1
- Chokes may be used on chip or cable side or both sides
- No power connections to the transformer. Transformer power is supplied by the ICS1893CF
- MIDCOM 7090-37 or equivalent symetrical magnetics are used

Figure 5-1 shows the design for the ICS1893CF twisted-pair interface.

- Two 49.9Ω 1% resistors are in series with a 100 nF capacitor to ground between them. These components form a network that connects across both pairs of twisted pairs A and B.
- Both twisted pairs A and B have an assigned plus and minus.

Note:

1. Keep all TX traces as short as possible.
2. When longer board twisted pair traces are used, 50Ω characteristic board trace impedance is desirable.


Figure 5-1.   ICS1893CF Twisted Pair *
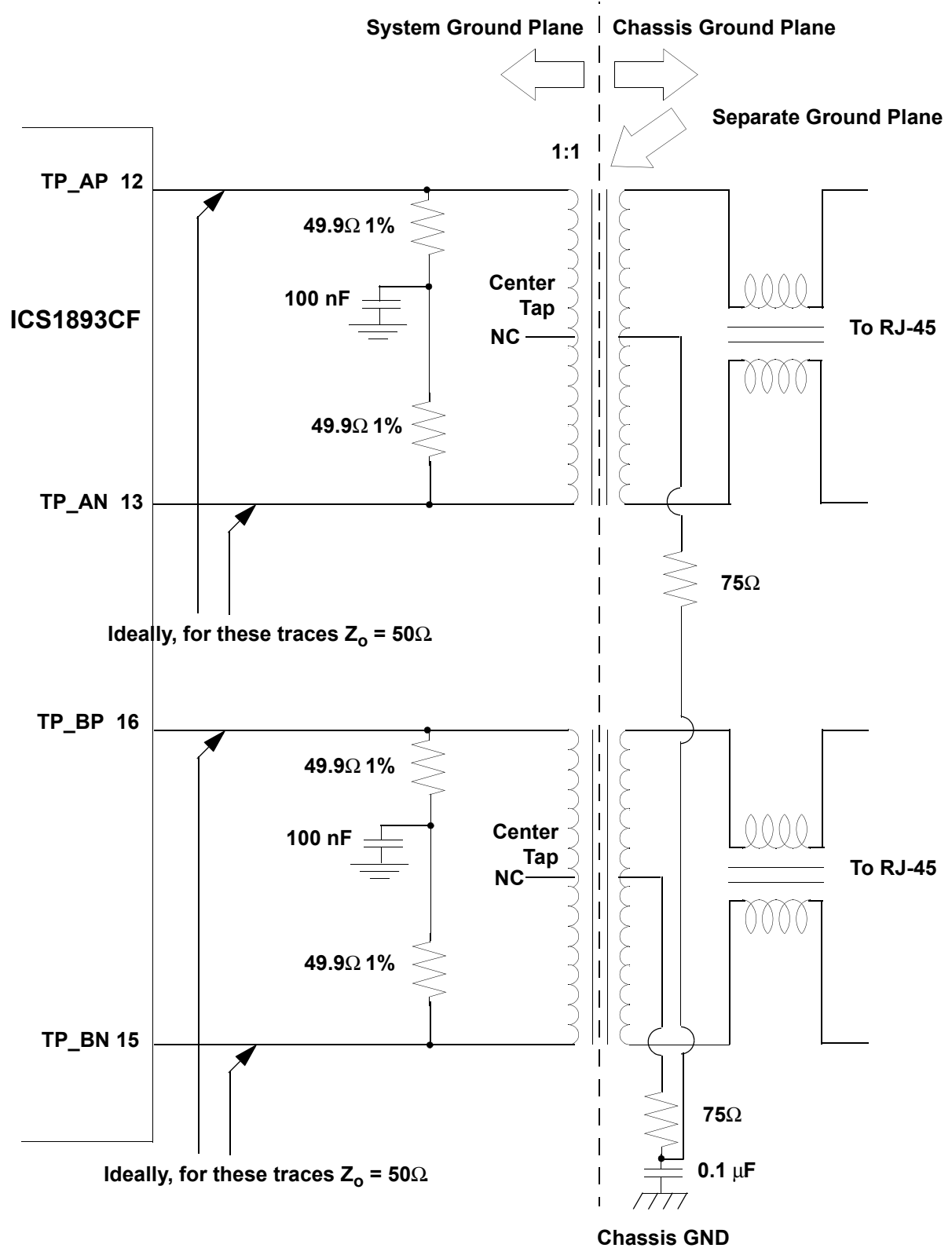
* For backward compatibility, refer to the the "1893C Alternate Schematic" application note.

5.4   Clock Reference Interface

The REF_IN pin provides the ICS1893CF Clock Reference Interface. The ICS1893CF requires a single clock reference with a frequency of 25 MHz ±50 parts per million. This accuracy is necessary to meet the interface requirements of the ISO/IEEE 8802-3 standard, specifically clauses 22.2.2.1 and 24.2.3.4. The ICS1893CF supports two clock source configurations: a CMOS oscillator or a CMOS driver. The input to REF_IN is CMOS (10% to 90% VDD), not TTL. Alternately, a 25MHz crystal may be used. The Oscillator specifications are shown in Table 5.2.

Figure 5-2.   Crystal or Oscillator Operation

Crystal
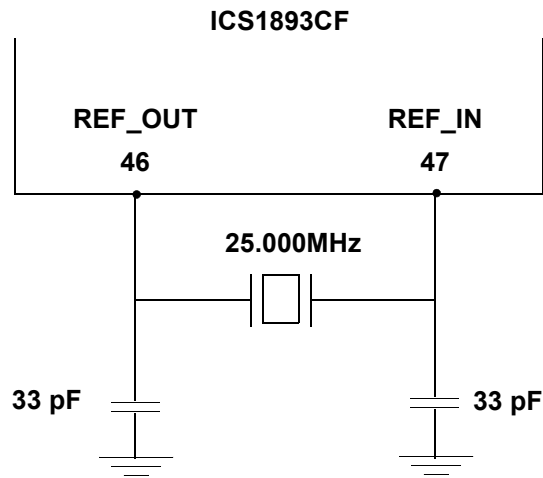
Oscillator
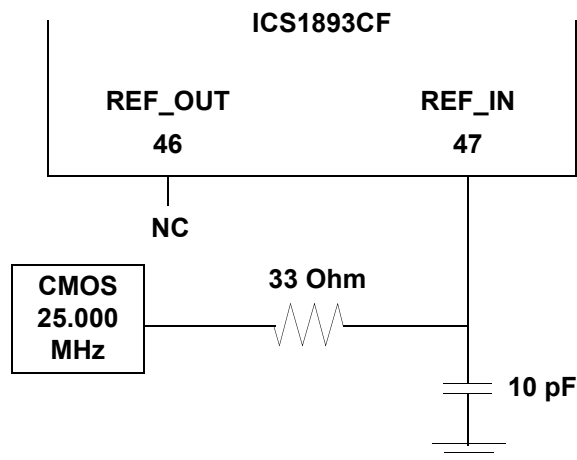
If a crystal is used as the clocking source, connect it to both the Ref_in (pin 47) and Ref_out (pin 46) pins of the ICS1893CF. A pair of bypass capacitors on either side of the crystal are connected to ground. The crystal is used in the parallel resonance or anti-resonance mode. The value of the load caps serve to adjust the final frequency of the crystal oscillation. Typical applications would use 33pF load caps. The exact value will be affected by the board routing capacitance on Ref_in and Ref_out pins. Smaller load capacitors raise the frequency of oscillation. Once the exact value of load capacitance is established it will be the same for all boards using the same specification crystal. The best way to measure the crystal frequency is to measure the frequency of TXCLK (pin 37) using a frequency counter with a 1 second gate time. Using the buffered output TXCLK prevents the crystal frequency from being affected by the measurement. The crystal specification is shown in Table 5.1.

Table 5-1. 25MHz Crystal Specification

Specifications	Symbol	Minimum	Typical	Maximum	Unit
Fundamental Frequency (tolerance is sum of freq., temp., stability and aging.)	F0	24.99875	25.00000	25.00125	MHz
Freq. Tolerance	ΔF/f			$\pm$50	ppm
Input Capacitance	Cin		3		pF

Table 5-2. 25MHz Oscillator Specification

Specifications	Symbol	Minimum	Typical	Maximum	Unit
Output Frequency	F0	24.99875	25.00000	25.00125	MHz
Freq. Stability (including aging)	ΔF/f			$\pm$50	ppm
Duty cycle CMOS level one-half VDD	Tw/T	35		65	%
VIH		2.79			Volts
VIL				0.33	Volts
Period Jitter	Tjitter			500	pS
Input Capacitance	CIN		3		pF

5.5   Status Interface

The ICS1893CF provides five multi-function configuration pins that report the results of continual link monitoring by providing signals that are intended for driving LEDs. (For the pin numbers, see Table 8.6.)

Table 5-3.   Pins for Monitoring the Data Link

| Pin	LED Driven by the Pin's Output Signal
P0AC	AC (Link **Ac**tivity) LED
P1CL	CL (**Col**lisions) LED
P2LI	LI (**L**ink **I**ntegrity) LED
P3TD	TD (**T**ransmit **D**ata) LED
P4RD	RD (**R**eceive **D**ata) LED

Note:

1. During either a power-on reset or a hardware reset, each multi-function configuration pin is an input that is sampled when the ICS1893CF exits the reset state. After sampling is complete, these pins are output pins that can drive status LEDs.

2. A software reset does not affect the state of a multi-function configuration pin. During a software reset, all multi-function configuration pins are outputs.

3. Each multi-function configuration pin must be pulled either up or down with a resistor to establish the address of the ICS1893CF. LEDs may be placed in series with these resistors to provide a designated status indicator as described in Table 5-3. Use 1KΩ resistors.

    Caution: All pins listed in Table 5-3 must not float.

4. As outputs, the asserted state of a multi-function configuration pin is the inverse of the sense sampled during reset. This inversion provides a signal that can illuminate an LED during an asserted state. For example, if a multi-function configuration pin is pulled down to ground through an LED and a current-limiting resistor, then the sampled sense of the input is low. To illuminate this LED for the asserted state, the output is driven high.

5. Adding 10KΩ resistors across the LEDs ensures the PHY address is fully defined during slow VDD power-ramp conditions.

6. PHY address 00 tri-states the MII interface. (Do not select PHY address 00 unless you want the MII tri-stated.)

Figure 5-3 shows typical biasing and LED connections for the ICS1893CF.

Figure 5-3.   ICS1893CF LED - PHY Interface
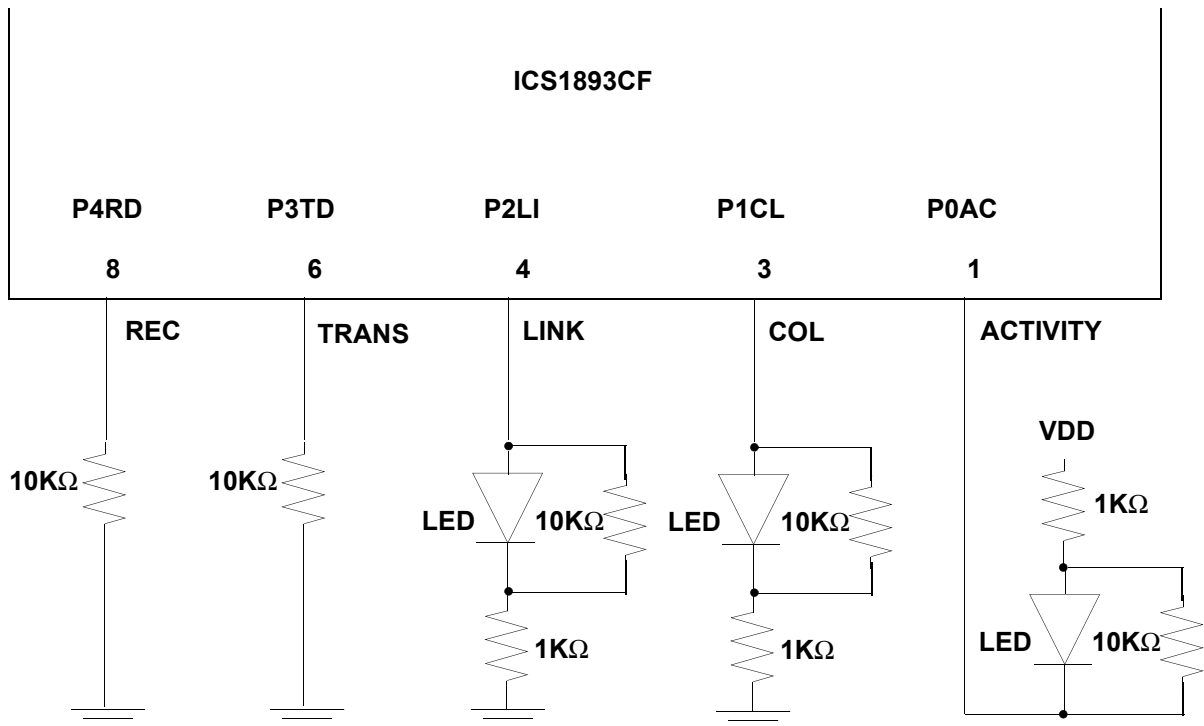
This circuit decodes to PHY address = 1.

Notes:

1. **All LED pins must be set during reset.**
2. **Caution: PHY address 00 tri-states the MII interface. Don't use PHY address 00.**
3. **For more reliable address capture during power-on reset, add a 10KΩ resistor across the LED.**

Chapter 6   Functional Blocks

This chapter discusses the following ICS1893CF functional blocks.

6.1   Functional Block: Media Independent Interface

All ICS1893CF MII interface signals are fully compliant with the ISO/IEC 8802-3 standard. In addition, the ICS1893CF MIIs can support two data transfer rates: 25 MHz (for 100Base-TX operations) and 2.5 MHz (for 10Base-T operations).

The Media Independent Interface (MII) consists of two primary components:

1. An interface between a MAC (Media Access Control sublayer) and the PHY (that is, the ICS1893CF). This MAC-PHY part of the MII consists of three subcomponents:

   a. A synchronous Transmit interface that includes the following signals:
      (1) A data nibble, TXD[3:0]
      (2) A delimiter, TXEN
      (3) A clock, TXCLK

   b. A synchronous Receive interface that includes the followings signals:
      (1) A data nibble, RXD[3:0]
      (2) An error indicator, RXER
      (3) A delimiter, RXDV
      (4) A clock, RXCLK

   c. A Media Status or Control interface that consists of a Carrier Sense signal (CRS) and a Collision Detection signal (COL).

2. An interface between the PHY (the ICS1893CF) and an STA (Station Management entity). The STA-PHY part of the MII is a two-wire, Serial Management Interface that consists of the following:

   a. A clock (MDC)

   b. A synchronous, bi-directional data signal (MDIO) that provides an STA with access to the ICS1893CF Management Register set

The ICS1893CF Management Register set (discussed in Chapter 7, "Management Register Set") consists of the following:

- Basic Management registers.

  As defined in the ISO/IEC 8802-3 standard, these registers include the following:
  – Control Register (register 0), which handles basic device configuration
  – Status Register (register 1), which reports basic device capabilities and status

- Extended Management registers.

  As defined in the ISO/IEC 8802-3 standard, the ICS1893CF supports Extended registers that provide access to the Organizationally Unique Identifier and all auto-negotiation functionality.

- ICS (Vendor-Specific) Management registers.

  The ICS1893CF provides vendor-specific registers for enhanced PHY operations. Among these is the QuickPoll Detailed Status Register that provides a comprehensive and consolidated set of real-time PHY information. Reading the QuickPoll register enables the MAC to obtain comprehensive status data with a single register access.