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QUAD LVDS OSCILLATOR/BUFFER

ICS556-03

Description

The ICS556-03 is a clock oscillator with quad LVDS outputs. Using a standard 25 MHz crystal, no additional external components are required to generate quad LVDS outputs at 25 MHz.

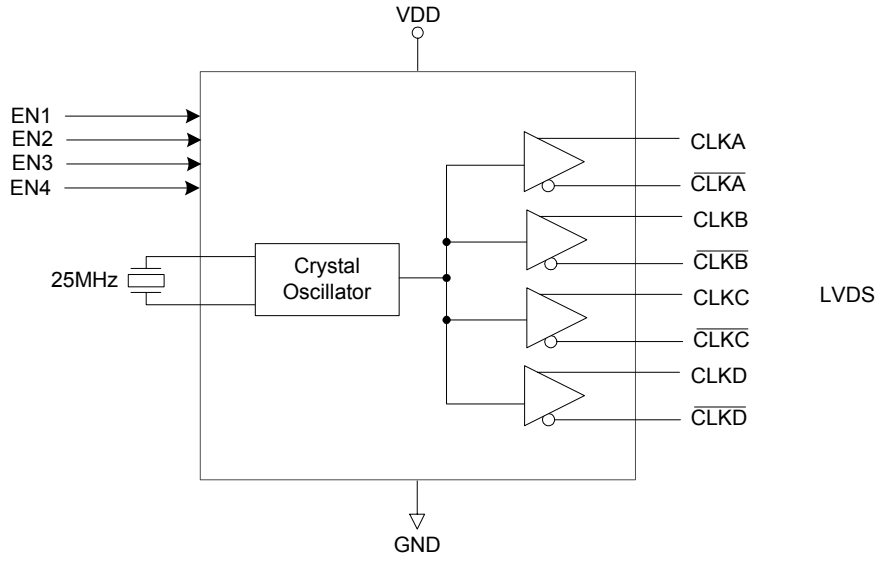
This product is intended for clock generation. It has low output jitter (variation in the output period), but input to output skew and jitter are not defined nor guaranteed.

Features

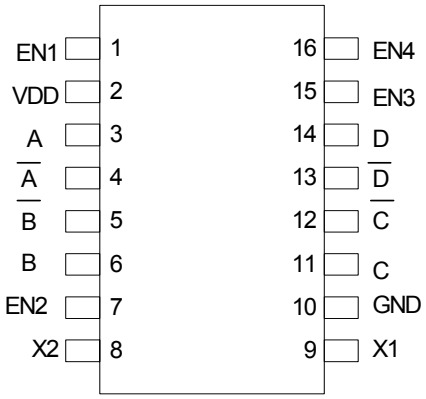
- Packaged in 16-pin TSSOP
- Requires no external components
- Low Phase Jitter: <1ps from 10 kHz to 10 MHz
- Quad, Differential LVDS outputs
- Operating voltage of 2.5 Volt
- Advanced, low-power, sub-micron CMOS process

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



16-Pin (150 mil) SOIC

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	EN1	Input	Enable pin for Outputs A and $\overline{A}$. EN1 high enables A, $\overline{A}$ outputs. EN1 low tri states A, $\overline{A}$ outputs. No Pull-Up resistor.
2	VDD	Power	Power supply. Connect to 2.5 V.
3	A	Output	Differential clock output.
4	$\overline{A}$	Output	Inverting differential clock output.
5	$\overline{B}$	Output	Inverting differential clock output.
6	B	Output	Differential clock output.
7	EN2	Input	Enable pin for Outputs B and $\overline{B}$. EN2 high enables B, $\overline{B}$ outputs. EN2 low tri states B, $\overline{B}$ outputs. No Pull-Up resistor.
8	X2	Input	Crystal connection.
9	X1	Input	Crystal input.
10	GND	Power	Connect to ground.
11	C	Output	Differential clock output.
12	$\overline{C}$	Output	Inverting differential clock output.
13	$\overline{D}$	Output	Inverting differential clock output.

Pin Number	Pin Name	Pin Type	Pin Description
14	D	Output	Differential clock output.
15	EN3	Input	Enable pin for Outputs C and $\overline{C}$. EN4 high enables C, $\overline{C}$ outputs. EN3 low tri states C, $\overline{C}$ outputs.No Pull-Up resistor.
16	EN4	Input	Enable pin for Outputs D and $\overline{D}$. EN4 high enables D, $\overline{D}$ outputs. EN4 low tri states D, $\overline{D}$ outputs.No Pull-Up resistor.

External Component Selection

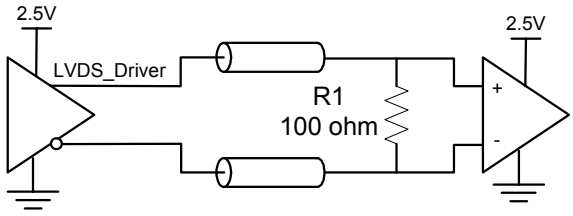
The ICS556-03 requires a minimum number of external components for proper operation.

Decoupling Capacitors

A decoupling capacitor of 0.01µF should be connected between VDD and GND on pins 2 and 10 as close to the ICS556-03 possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

LVDS Driver Termination

A general LVDS interface is shown in Figure 2. In a 100 ohm differential transmission line environment, LVDS drivers require a matched load termination of 100 across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the un-used outputs.



100 Ohm Differential Transmission Line

Figure 2. Typical LVDS Driver Termination

Quartz Crystal

The ICS556-03, a quad 25 MHz LVDS Clock utilizes an external crystal to generate 4 pairs of low phase noise outputs. The crystal should be a fundamental mode, parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation

Crystal Caps (pf)= (C_L-12)x2

In the equation, CL is the crystal Load capacitance. So for the crystal with 16pF load capacitance, two 8 pF[(16-12)x2] capacitors should be used.

The external crystal must be connected as close to the chip as possible and should be on the same side of the PCB as the ICS556-03. There should be no via's between the crystal pins and the X1 and X2 device pins. There should be no signal traces underneath or close to the crystal.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS556-03. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+2.375		+2.625	V
Reference crystal parameters	Refer to page 3			

DC Electrical Characteristics

VDD=2.5 V ±5% , Ambient temperature 0 to +70° C, unless stated otherwise

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		2.375		2.625	V
Output High Voltage	V_{OH}	Note 1	1.375			V
Output Low Voltage	V_{OL}	Note 1			1.125	V
Input High Voltage (EN1, EN2,EN3 & EN4)	V_{IH}		2.0			V
Input High Voltage (EN1, EN2,EN3 & EN4)	V_{IL}				0.5	V
Operating Supply Current	IDD	OE1:4:1		17		mA
		OE1:4:0		4		mA
Short Circuit Current	I_{OS}			±50		mA

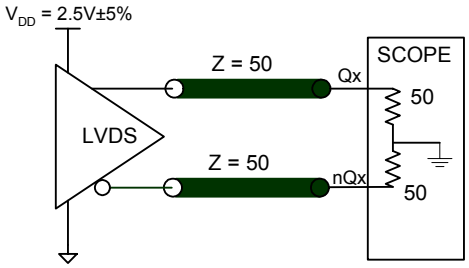
Note 1: Outputs terminated with 50Ω to VDD/2

AC Electrical Characteristics

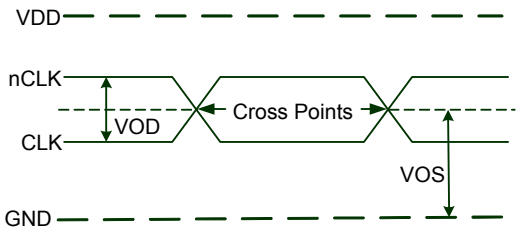
VDD = 2.5 V ±5%, Ambient Temperature 0 to +70° C, CL=5 pF, unless stated otherwise

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Frequency			25		MHz
Output Frequency			25		MHz
Differential Output Voltages (V_{OD})		250	350	450	mV
Δ V_{OD}	V_{OD} Magnitude Change	-40	0	40	mV
Offset Voltage (V_{OS})		1.125	1.25	1.375	V
Δ V_{OS}	V_{OS} Magnitude Change		3	25	mV
Differential Output Short Circuit Current (I_{OSD})			-3.5		mA
Output Short Circuit Current (I_{OS})			-3.5		mA
Output Rise Time	20% to 80%, no load		0.8	1.2	ns
Output Fall Time	20% to 80%, no load		0.8	1.2	ns
Output Clock Duty Cycle	Measured at 1.25V,	45	50	55	%
Output Short Circuit Current			±50		mA
Channel Output to output Skew			20	100	ps
Part to Part Skew				1.5	ns
Maximum Output Jitter (p-p)			40		ps
Phase Jitter (RMS)	Phase Noise integrated from 10 kHz to 10 MHz		2	5	ps

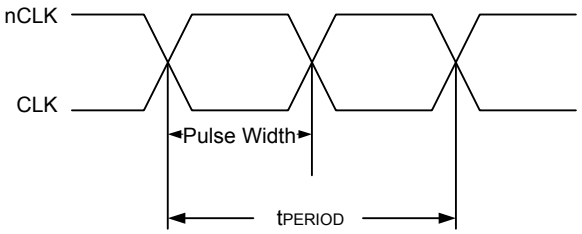
Parameter Measurement Information



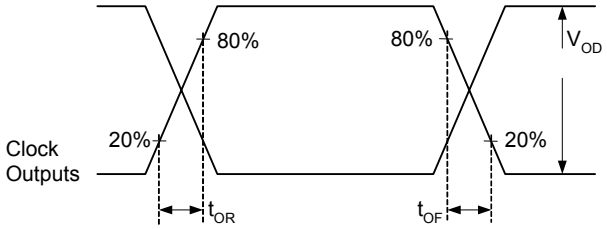
2.5V OUTPUT LOAD AC TEST CIRCUIT



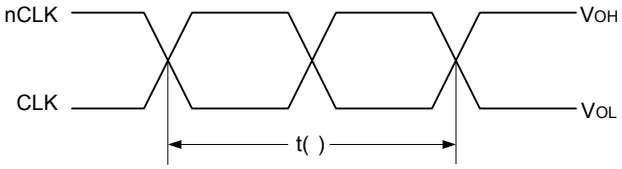
DIFFERENTIAL INPUT LEVEL



tPW & tPERIOD

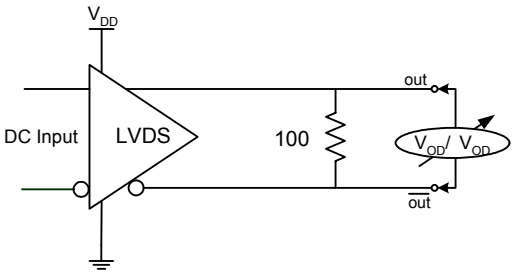


OUTPUT RISE/FALL TIME

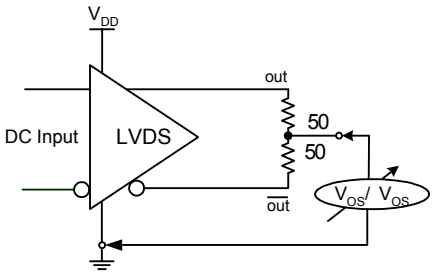


$tjit(\ ) = \left| t(\ ) - t(\ )_{mean} \right|$ = Phase Jitter

PHASE JITTER



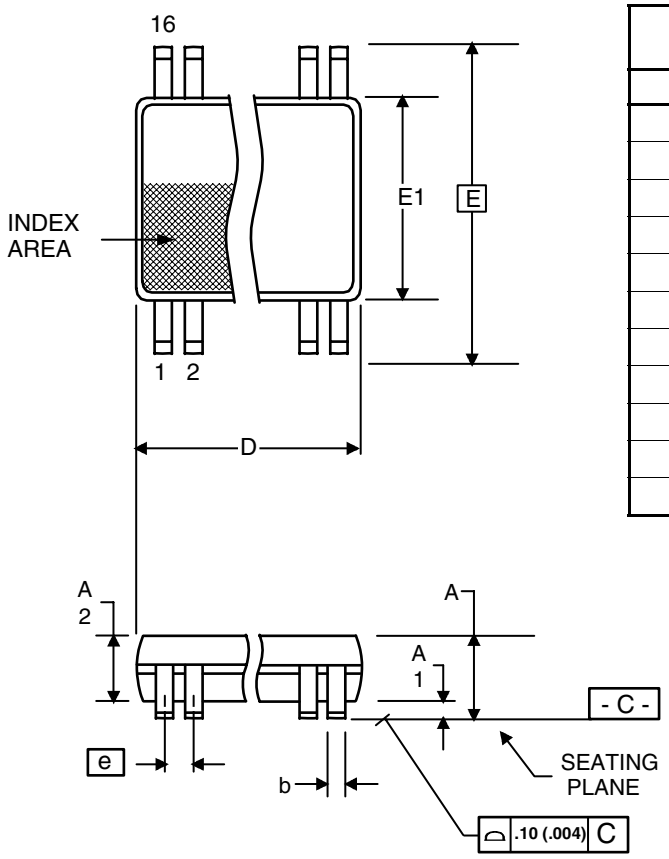
V_{OD} SETUP



V_{OS} SETUP

Package Outline and Package Dimensions (16-pin TSSOP, 4.40 mm Body, 0.65 mm Pitch)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	Min	Max	Min	Max
A	--	1.20	--	0.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	4.90	5.1	0.193	0.201
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	0.018	0.030
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping/Packaging	Package	Temperature
556G-03I*	ICS556-03I	Tubes	16-pin TSSOP	-40° to +85°C
556G-03IT*	ICS556-03I	Tape and Reel	16-pin TSSOP	-40° to +85°C
556G-03ILF	55603ILF	Tubes	16-pin TSSOP	-40° to +85°C
556G-03ILFT	55603ILF	Tape and Reel	16-pin TSSOP	-40° to +85°C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

"LF" denotes Pb free packaging, RoHS compliant

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