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NETWORKING CLOCK SYNTHESIZER AND ZERO DELAY BUFFER ICS680-01

Description

The ICS680-01 generates four high-frequency clock outputs and a reference from a 25 MHz crystal or clock input. The device includes a low-skew, single input to four output zero delay clock buffer. It can replace multiple crystals and oscillators, saving board space and cost.

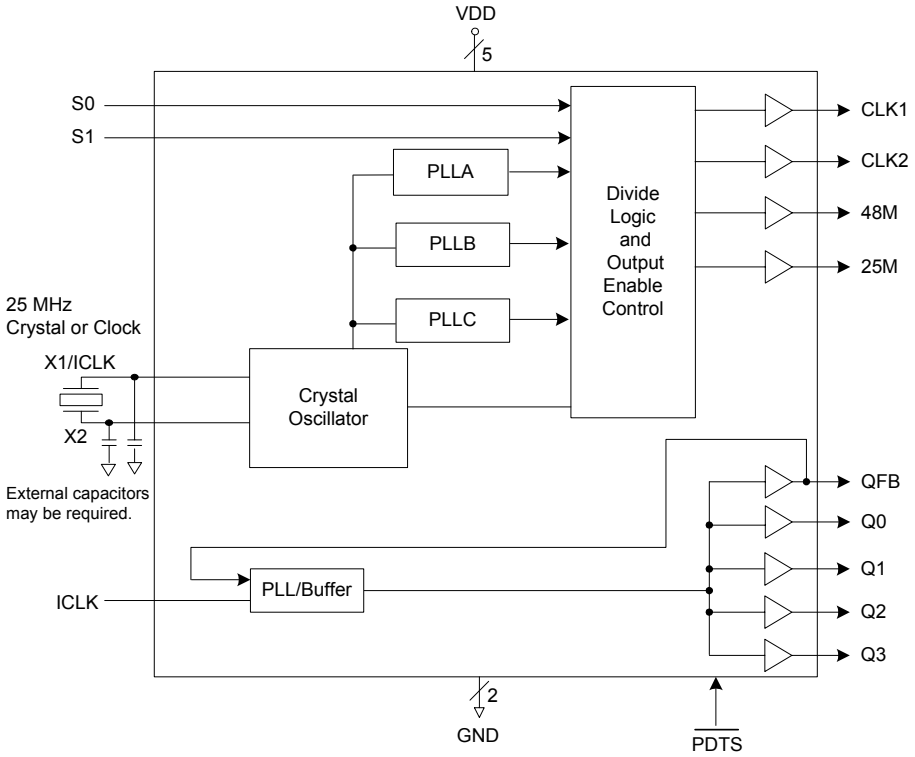
The device has a power-down tri-state ($\overline{\text{PDTS}}$) pin that place the clock outputs in a high-impedance state when pulled low. The $\overline{\text{PDTS}}$ pin includes an internal pull-up resistor.

Features

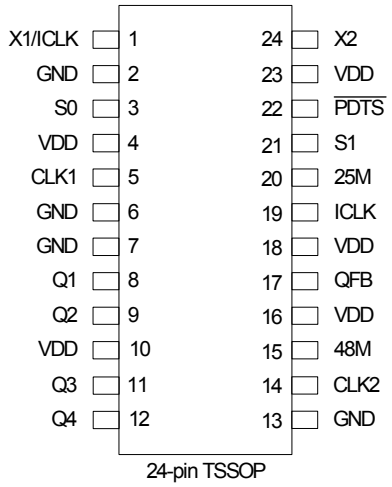
- Packaged in 24-pin TSSOP
- Available in Pb (lead) free package
- Replaces multiple crystals and oscillators
- Input crystal or clock frequency of 25 MHz
- Five output driver driven by external clock
- Duty cycle of 45/55
- Operating voltage of 3.3 V
- Advanced, low-power CMOS process
- Fixed output frequencies of 25 MHz and 48 MHz
- Selectable output frequencies of 24 MHz, 48 MHz, 50 MHz and 66.6666 MHz
- Qx outputs replace costly discrete buffer
- Low-skew buffer outputs (250 ps)

NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01

Block Diagram



Pin Assignment



24-pin TSSOP

Output Clock Select Table

S0	S1	CLK1 (MHz)	CLK2 (MHz)
M	M	OFF	48
0	0	50	48
0	1	66.6666	48
1	0	50	24
1	1	66.6666	24

Pin Descriptions

Pin Number	Pin Name	Pin Type	Pin Description
1	X1/ICLK	XI	Crystal input. Connect this pin to a crystal or external clock source.
2	GND	Power	Connect to ground.
3	S0	Input	Select pin 0. See table above.
4	VDD	Power	Connect to voltage supply.
5	CLK1	Output	Selectable output clock. See table above. Weak internal pull-down when tri-state.
6	GND	Power	Connect to ground.
7	GND	Power	Connect to ground.
8	Q1	Output	Clock output 1. Weak internal pull-down when tri-state.
9	Q2	Output	Clock output 2. Weak internal pull-down when tri-state.
10	VDD	Power	Connect to voltage supply.
11	Q3	Output	Clock output 3. Weak internal pull-down when tri-state.
12	Q4	Output	Clock output 4. Weak internal pull-down when tri-state.
13	GND	Power	Connect to ground.
14	CLK2	Output	Selectable output clock. See table above. Weak internal pull-down when tri-state.
15	48M	Output	48 MHz output clock. Weak internal pull-down when tri-state.
16	VDD	Power	Connect to voltage supply.
17	QFB	Output	Feedback pin. Internally connected.

Pin Number	Pin Name	Pin Type	Pin Description
18	VDD	Power	Connect to voltage supply.
19	ICLK	Input	Zero Delay Buffer Input. Weak Internal pull-up.
20	25M	Output	25 MHz reference output clock. Weak internal pull-down when tri-state.
21	S1	Input	Select pin 1. See table above.
22	$\overline{PDTS}$	Power	Power-down tri-state. Powers down entire chip and tri-states outputs when low. Internal pull-up resistor.
23	VDD	Power	Connect to voltage supply.
24	X2	XO	Crystal output. Connect this pin to a crystal. Float for clock input.

External Components

The ICS680-01 requires a minimum number of external components for proper operation.

Decoupling Capacitor

A decoupling capacitor of 0.01µF must be connected between VDD (pins 5 and 16) and GND (pins 6 and 15), as close to these pins as possible. For optimum device performance, the decoupling capacitor should be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit.

Series Termination Resistor

When the PCB trace between the clock outputs and the loads are over 1 inch, series termination should be used. To series terminate a 50Ω trace (a commonly used trace impedance) place a 33Ω resistor in series with the clock line, as close to the clock output pin as possible. The nominal impedance of the clock output is 20Ω

Crystal Information

The crystal used should be a fundamental mode (do not use third overtone), parallel resonant. Crystal capacitors should be connected from pins X1 to ground and X2 to ground to optimize the initial accuracy. The value of these capacitors is given by the following equation crystal caps (pF) = $(C_L-6)x2$

In the equation, C_L is the crystal load capacitance. So for a crystal with a 16 pF load capacitance, two 20 pF[(16-6)x2] capacitors should be used

PCB Layout Recommendations

For optimum device performance and lowest output phase noise, the following guidelines should be observed.

1) The 0.01µF decoupling capacitor should be mounted on the component side of the board as close to the VDD pin as possible. No vias should be used between decoupling capacitor and VDD pin. The PCB trace to VDD pin should be kept as short as possible, as should the PCB trace to the ground via.

2) The external crystal should be mounted just next to the device with short traces. The X1 and X2 traces should not be routed next to each other with minimum spaces, instead they should be separated and away from other traces.

3) To minimize EMI, the 33Ω series termination resistor (if needed) should be placed close to the clock output.

4) An optimum layout is one with all components on the same side of the board, minimizing vias through other signal layers. Other signal traces should be routed away from the ICS680-01. This includes signal traces just underneath the device, or on layers adjacent to the ground plane layer used by the device.

Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the ICS680-01. These ratings, which are standard values for ICS commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
Supply Voltage, VDD	7 V
All Inputs and Outputs	-0.5 V to VDD+0.5 V
Ambient Operating Temperature	0 to +70° C
Storage Temperature	-65 to +150° C
Junction Temperature	125° C
Soldering Temperature	260° C

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature	0		+70	° C
Power Supply Voltage (measured in respect to GND)	+3.13	+3.3	+3.46	V

DC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Operating Voltage	VDD		3.13	3.3	3.46	V
Supply Current	IDD	No load,$\overline{PDTS}$=1		32		mA
		No load,$\overline{PDTS}$=0		300		µA
Input High Voltage, binary inputs	V_{IH}	$\overline{PDTS}$, ICLK	2			V
Input High Voltage, trinary inputs	V_{IH}	S0, S1	VDD-0.5			V
Input Low Voltage, binary inputs	V_{IL}	$\overline{PDTS}$, ICLK			0.8	V
Input Low Voltage, trinary inputs	V_{IL}	S0, S1			0.5	V
Output High Voltage	V_{OH}	I_{OH} = -4 mA	VDD-0.4			V
Output High Voltage	V_{OH}	I_{OH} = -12 mA	2.4			V
Output Low Voltage	V_{OL}	I_{OL} = 12 mA			0.8	V
		I_{OL} = 4 mA			0.4	V
Short Circuit Current	I_{OS}	CLK output		±50		mA
Input Capacitance, Inputs	C_{IN}			5		pF
Nominal Output Impedance	Z_{OUT}			20		Ω
On-Chip Pull-up Resistor, Inputs	R_{PU}	$\overline{PDTS}$, SEL		250		kΩ
On-Chip Pull-down Resistor, Outputs	R_{PD}	CLK outputs		250		kΩ

AC Electrical Characteristics

Unless stated otherwise, **VDD = 3.3 V ±5%**, Ambient Temperature 0 to +70° C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Frequency	f_{IN}	X1		25		MHz
		ICLK		33		MHz
Output Frequency	f_{OUT}	Q0 to Q3, QFB, Note 1		33		MHz
Output Rise Time	t_{OR}	20% to 80%, Note 1		1.5		ns
Output Fall Time	t_{OF}	80% to 20%, Note 1		1.5		ns
Output Clock Duty Cycle	t_D	at VDD/2, Note 2	40		60	%
Power-up Time		PLL lock-time from power-up to 1% of final frequency			10	ms
		$\overline{\text{PDTS}}$ goes high until stable CLK outputs at 1% of final frequency			2	ms
One Sigma Clock Period Jitter		Configuration dependent		50		ps
Maximum Absolute Jitter	t_{ja}	Deviation from mean. Configuration dependent.		±200		ps
QFB to ICLK Skew	t_{PD}	Measured at VDD/2, Note 3	-350		350	
Pin-to-pin Skew		QFB, Q0 to Q3, Note 3	-250		250	ps

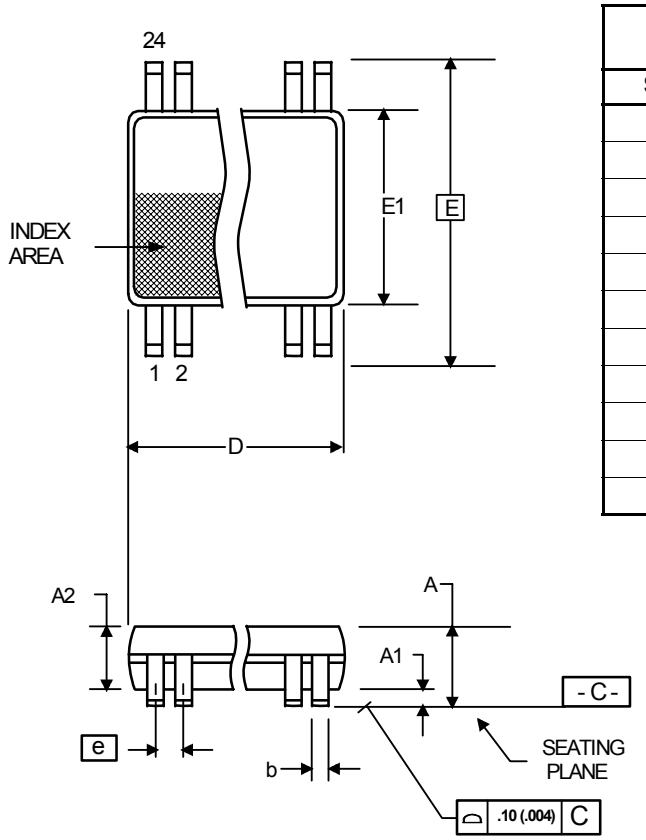
Note 1: Measured with a 15 pF load.

Note 2: Duty cycle is configuration dependent. Most configurations are min 45% / max 55%.

Note 3: Skew is measured at 1.4 V on rising edges with a 33 MHz ICLK.

Package Outline and Package Dimensions (24-pin TSSOP, 173 Mil. Body)

Package dimensions are kept current with JEDEC Publication No. 95



	Millimeters		Inches	
Symbol	**Min**	**Max**	**Min**	**Max**
	—	1.20	—	.047
A1	0.05	0.15	0.002	0.006
A2	0.80	1.05	0.032	0.041
b	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	7.70	7.90	0.303	0.311
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	0.169	0.177
e	0.65 Basic		0.0256 Basic	
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°

Ordering Information

Part / Order Number	Marking	Shipping Packaging	Package	Temperature
680G-01*	680G-01	Tubes	24-pin TSSOP	0 to +70° C
680G-01T*	680G-01	Tape and Reel	24-pin TSSOP	0 to +70° C
680G-01LF	680G-01LF	Tubes	24-pin TSSOP	0 to +70° C
680G-01LFT	680G-01LF	Tape and Reel	24-pin TSSOP	0 to +70° C

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01**

"LF" denotes Pb (lead) free package.

Revision History

Rev.	Originator	Date	Description of Change
D	P.Griffith	10/01/04	Removed power supply ramp-up time spec; added trinary input specs to DC chars; added a second Output Low Voltage spec; updated Supply Current specs from 50 to 32 mA, and 50 to 300 uA; changed pull-down resistor value from 525 to 250 kohms; changed Output Rise/Fall times from 1 to 1.5 ns
E	P.Griffith	12/21/04	Released as standard product from custom device.
F	J. Sarma	02/03/05	Add LF ordering info.
G		11/04/09	Added EOL note for non-green parts.

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