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LOW SKEW, 1-TO-2, DIFFERENTIAL-TO-2.5V, 3.3V LVPECL/ECL FANOUT BUFFER

ICS853011C

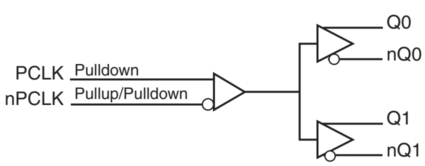
General Description

The ICS853011C is a low skew, high performance 1-to-2 Differential-to-2.5V, 3.3V LVPECL/ECL Fanout Buffer and a member of the HiPerClockS ™ family of High Performance Clock Solutions from IDT. The ICS853011C is characterized to operate from either a 2.5V or a 3.3V power supply. Guaranteed output and part-to-part skew characteristics make the ICS853011C ideal for those clock distribution applications demanding well defined performance and repeatability.

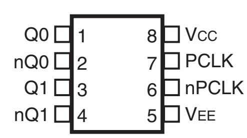
Features

- Two differential 2.5V or 3.3V LVPECL/ECL outputs
- One differential PCLK, nPCLK input pair
- PCLK, nPCLK pair can accept the following differential input levels: LVPECL, LVDS, CML, SSTL
- Output frequency: >2.5GHz
- Translates any single ended input signal to 3.3V LVPECL levels with resistor bias on nPCLK input
- Additive phase jitter, RMS: 0.16ps (typical)
- Output skew: 15ps (maximum)
- Part-to-part skew: 130ps (maximum)
- Propagation delay: 330ps (maximum)
- LVPECL mode operating voltage supply range: V_{CC} = 2.375V to 3.8V, V_{EE} = 0V
- ECL mode operating voltage supply range: V_{CC} = 0V, V_{EE} = -3.8V to -2.375V
- -40°C to 85°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Block Diagram



Pin Assignment



ICS853011C
8 Lead SOIC, 150MIL
3.90mm x 4.90mm x 1.37mm package body
M Package
Top View

ICS853011C
8 Lead TSSOP, 118mil
3.0mm x 3.0mm x 0.97 package body
G Package
Top View

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2	Q0, nQ0	Output		Differential output pair. LVPECL/ECL interface levels.
3, 4	Q1, nQ1	Output		Differential output pair. LVPECL/ECL interface levels.
5	V_{EE}	Power		Negative supply pin.
6	nPCLK	Input	Pullup/ Pulldown	Inverting differential LVPECL clock input. $V_{CC}/2$ default when left floating.
7	PCLK	Input	Pulldown	Non-inverting differential LVPECL clock input.
8	V_{CC}	Power		Positive supply pin.

NOTE: *Pullup and Pulldown* refers to internal input resistors. See Table 2, *Pin Characteristics,* for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
R_{PULLUP}	Input Pullup Resistor			37		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			75		kΩ

Absolute Maximum Ratings

NOTE: Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Item	Rating
Supply Voltage, V_{CC}	4.6V (LVPECL mode, V_{EE} = 0V)
Negative Supply Voltage, V_{EE}	-4.6V (ECL mode, V_{CC} = 0V)
Inputs, V_I (LVPECL mode)	-0.5V to V_{CC} + 0.5V
Inputs, V_I (ECL mode)	0.5V to V_{EE} – 0.5V
Outputs, I_O Continuos Current Surge Current	 50mA 100mA
Operating Temperature Range, T_A	-40°C to 85°C
Storage Temperature, T_{STG}	-65°C to 150°C
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 8 Lead SOIC	 112.7°C/W (0 lfpm)
Package Thermal Impedance, θ_{JA} (Junction-to-Ambient) for 8 Lead TSSOP	 101.7°C/W (0 mps)

DC Electrical Characteristics

Table 3A. Power Supply DC Characteristics, V_{CC} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Positive Supply Voltage		2.375	3.3	3.8	V
I_{EE}	Power Supply Current				24	mA

Table 3B. LVPECL DC Characteristics, V_{CC} = 3.3V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C Min	-40°C Typ	-40°C Max	25°C Min	25°C Typ	25°C Max	80°C Min	80°C Typ	80°C Max	Units
V_{OH}	Output High Current; NOTE 1		2.175	2.275	2.38	2.225	2.295	2.37	2.22	2.295	2.365	V
V_{OL}	Output Low Current; NOTE 1		1.405	1.545	1.68	1.425	1.52	1.615	1.44	1.535	1.63	V
V_{PP}	Peak-to-Peak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		3.3	1.2		3.3	1.2		3.3	V
I_{IH}	Input High Current	PCLK/nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

Table 3C. LVPECL DC Characteristics, V_{CC} = 2.5V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C Min	-40°C Typ	-40°C Max	25°C Min	25°C Typ	25°C Max	80°C Min	80°C Typ	80°C Max	Units
V_{OH}	Output High Current; NOTE 1		1.375	1.475	1.58	1.425	1.495	1.57	1.42	1.495	1.565	V
V_{OL}	Output Low Current; NOTE 1		0.605	0.745	0.88	0.625	0.72	0.815	0.64	0.735	0.83	V
V_{PP}	Peak-toPeak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		1.2		2.5	1.2		2.5	1.2		2.5	V
I_{IH}	Input High Current	PCLK/nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

Table 3D. ECL DC Characteristics, V_{CC} = 0V; V_{EE} = -3.8V to -2.375V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{OH}	Output High Current; NOTE 1		-1.125	-1.025	-0.92	-1.075	-1.005	-0.93	-1.08	-1.005	-0.935	V
V_{OL}	Output Low Current; NOTE 1		-1.895	-1.755	-1.62	-1.875	-1.78	-1.685	-1.86	-1.765	-1.67	V
V_{PP}	Peak-toPeak Input Voltage		150	800	1200	150	800	1200	150	800	1200	V
V_{CMR}	Input High Voltage Common Mode Range; NOTE 2, 3		V_{EE}+1.2		0	V_{EE}+1.2		0	V_{EE}+1.2		0	V
I_{IH}	Input High Current	PCLK/ nPCLK			150			150			150	µA
I_{IL}	Input Low Current	PCLK	-10			-10			-10			µA
		nPCLK	-150			-150			-150			µA

Input and output parameters vary 1:1 with V_{CC}. V_{EE} can vary +0.925V to -0.5V.
NOTE 1: Outputs terminated with 50Ω to V_{CC} – 2V.
NOTE 2: Common mode voltage is defined as V_{IH}.
NOTE 3: For single-ended applications, the maximum input voltage for PCLK, nPCLK is V_{CC} + 0.3V.

AC Electrical Characteristics

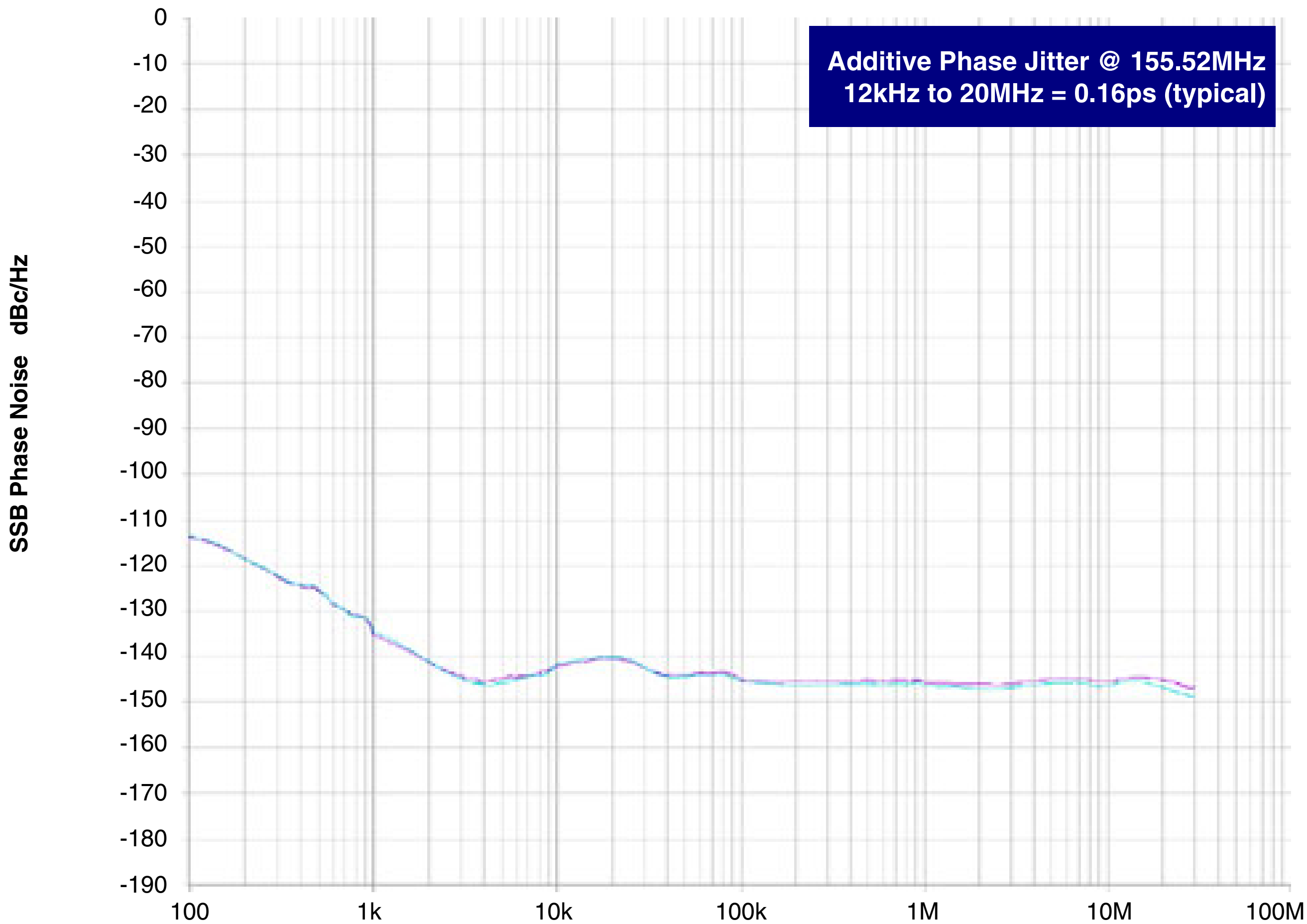
Table 4. AC Characteristics, V_{CC} = 0V; V_{EE} = -3.8V to -2.375V or, V_{CC} = 2.375V to 3.8V; V_{EE} = 0V, T_A = -40°C to 85°C

Symbol	Parameter		-40°C			25°C			80°C			Units
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{MAX}	Output Frequency				>2.5			>2.5			>2.5	GHz
t_{PD}	Propagation Delay; NOTE 1		170		320	180		330	190		345	ps
*t*jit	Additive Phase Jitter, RMS; refer to Additive Phase Jitter section			0.16			0.16			0.16		ps
*t*sk(o)	Output Skew; NOTE 2, 4				15			15			15	ps
*t*sk(pp)	Part-to-Part Skew; NOTE 3, 4				150			150			150	ps
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		250	100		250	100		250	ps
odc	Output Duty Cycle		48		52	48		52	48		52	%

All parameters are measured at f ≤ 1.4GHz, unless otherwise noted.
NOTE 1: Measured from the differential input crossing point to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.
NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

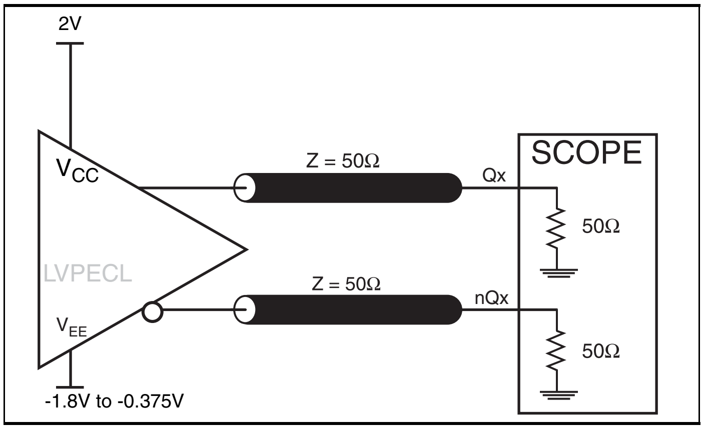
Additive Phase Jitter

The spectral purity in a band at a specific offset from the fundamental compared to the power of the fundamental is called the ***dBc Phase Noise.*** This value is normally expressed using a Phase noise plot and is most often the specified plot in many applications. Phase noise is defined as the ratio of the noise power present in a 1Hz band at a specified offset from the fundamental frequency to the power value of the fundamental. This ratio is expressed in decibels (dBm) or a ratio of the power in the 1Hz band to the power in the fundamental. When the required offset is specified, the phase noise is called a ***dBc*** value, which simply means dBm at a specified offset from the fundamental. By investigating jitter in the frequency domain, we get a better understanding of its effects on the desired application over the entire time record of the signal. It is mathematically possible to calculate an expected bit error rate given a phase noise plot.

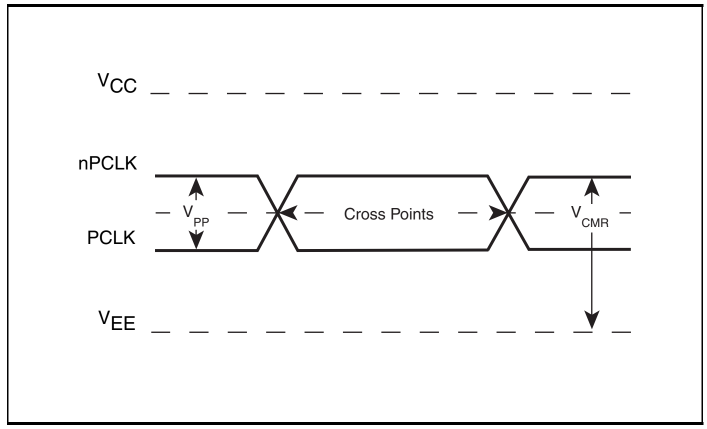


As with most timing specifications, phase noise measurements have issues. The primary issue relates to the limitations of the equipment. Often the noise floor of the equipment is higher than the noise floor of the device. This is illustrated above. The device meets the noise floor of what is shown, but can actually be lower. The phase noise is dependant on the input source and measurement equipment.

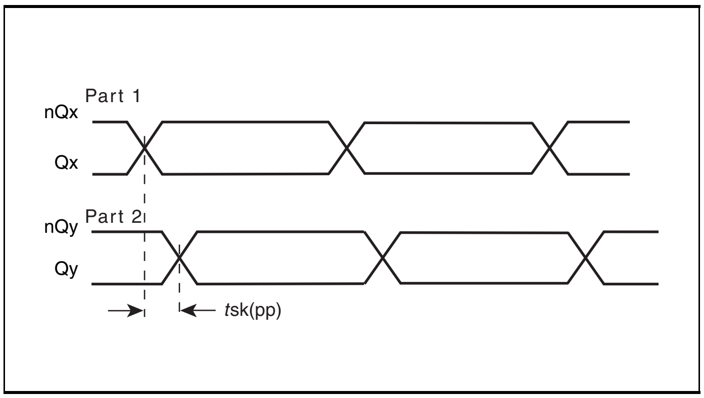
Parameter Measurement Information



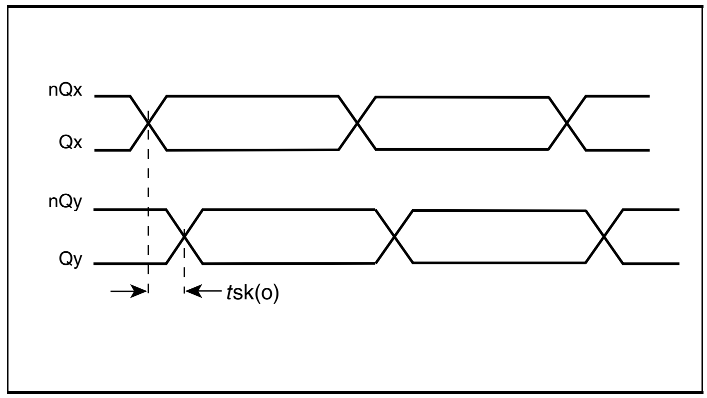
LVPECL Output Load AC Test Circuit



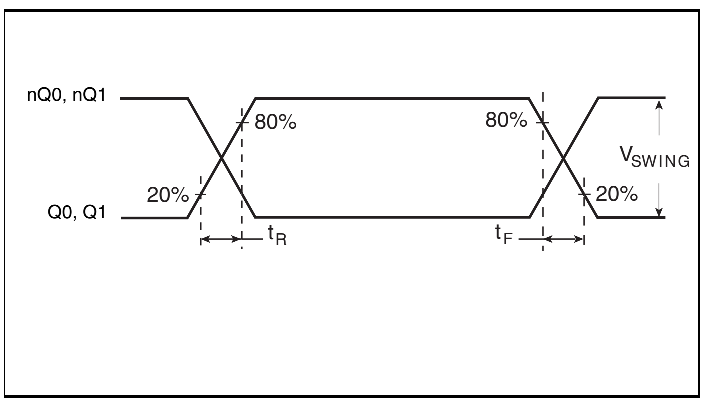
Differential Input Level



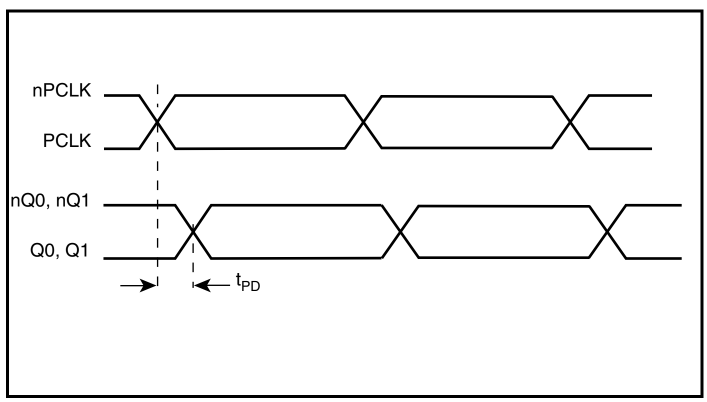
Part-to-Part Skew



Output Skew

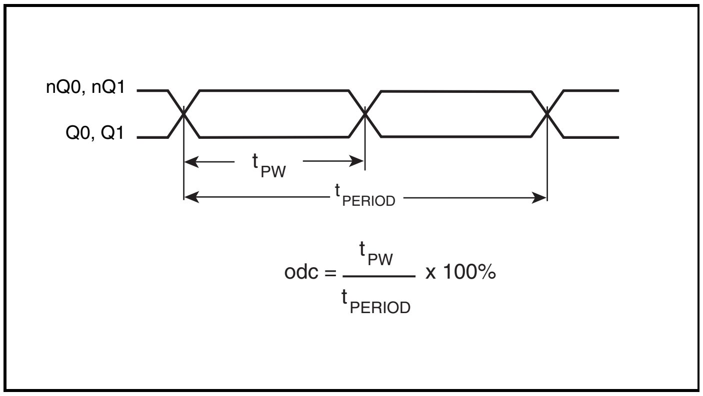


Output Rise/Fall Time



Propagation Delay

Parameter Measurement Information, continued



Output Duty Cycle/Pulse Width/Period

Application Information

Wiring the Differential Input to Accept Single Ended Levels

Figure 1 shows how the differential input can be wired to accept single ended levels. The reference voltage V_REF = $V_{CC}/2$ is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio of R1 and R2 might need to be adjusted to position the V_REF in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and V_{CC} = 3.3V, V_REF should be 1.25V and R2/R1 = 0.609.

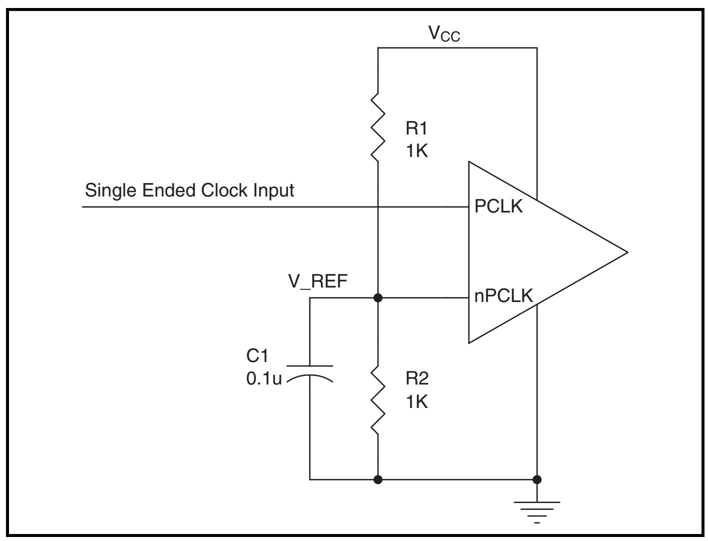


Figure 1. Single-Ended Signal Driving Differential Input

LVPECL Clock Input Interface

The PCLK/nPCLK accepts LVPECL, LVDS, CML, SSTL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. *Figures 2A to 2E* show interface examples for the HiPerClockS PCLK/nPCLK input driven by the most common driver types. The input interfaces suggested here are examples only. If the driver is from another vendor, use their termination recommendation. Please consult with the vendor of the driver component to confirm the driver termination requirements.

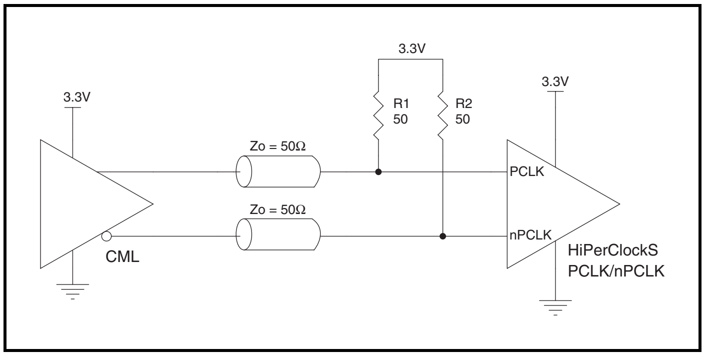


Figure 2A. HiPerClockS PCLK/nPCLK Input Driven by an Open Collector CML Driver

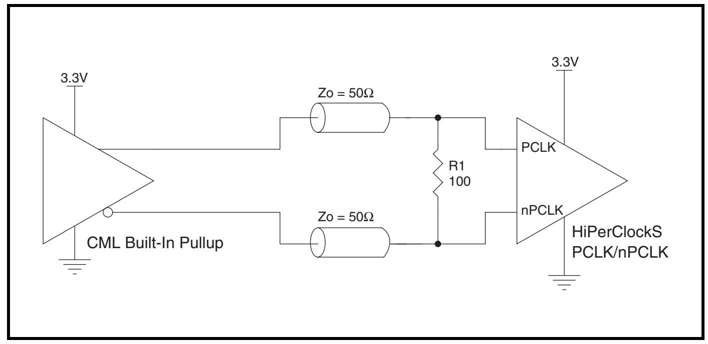


Figure 2B. HiPerClockS PCLK/nPCLK Input Driven by a Built-In Pullup CML Driver

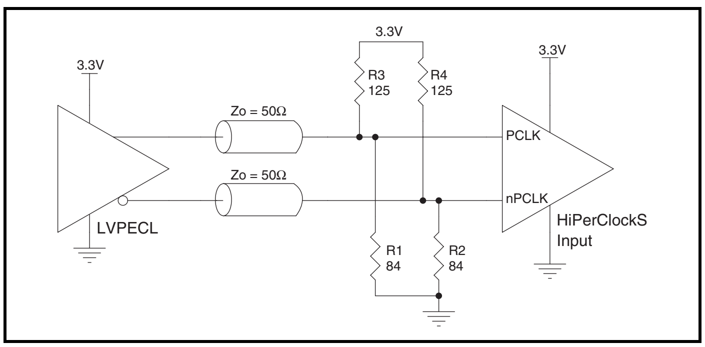


Figure 2C. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver

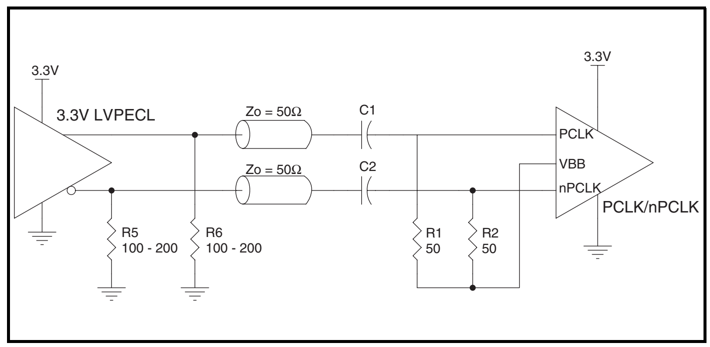


Figure 2D. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVPECL Driver with AC Couple

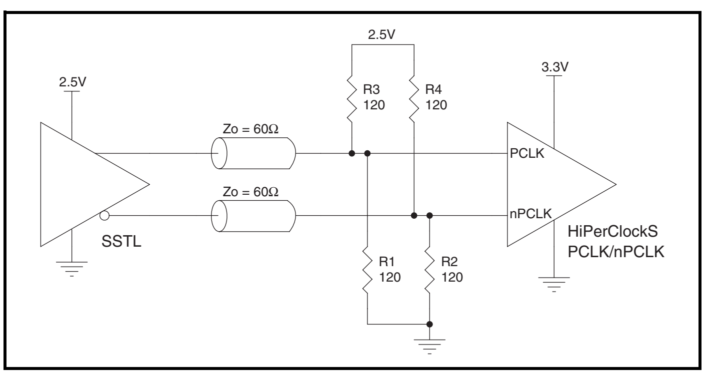


Figure 2E. HiPerClockS PCLK/nPCLK Input Driven by an SSTL Driver

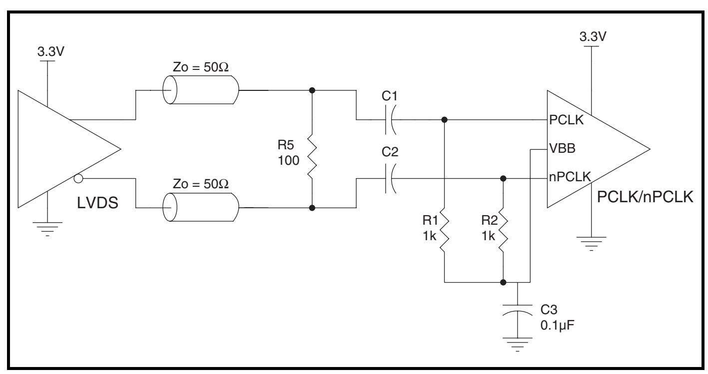


Figure 2F. HiPerClockS PCLK/nPCLK Input Driven by a 3.3V LVDS Driver

Recommendations for Unused Output Pins

Outputs:

LVPECL Outputs:

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Outputs

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 3A and 3B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

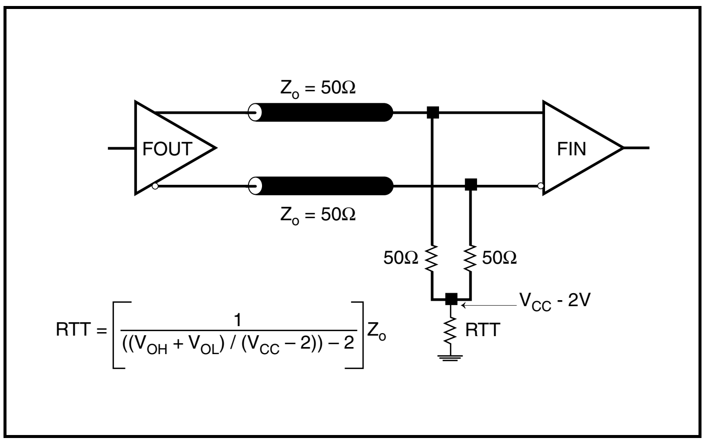


Figure 3A. 3.3V LVPECL Output Termination

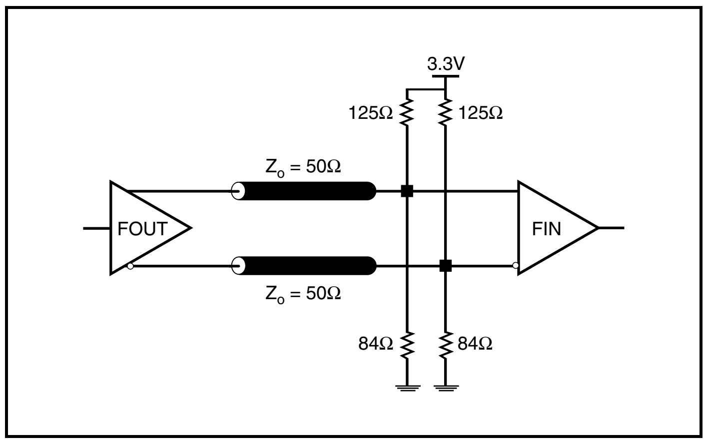


Figure 3B. 3.3V LVPECL Output Termination

Termination for 2.5V LVPECL Outputs

Figure 4A and *Figure 4B* show examples of termination for 2.5V LVPECL driver. These terminations are equivalent to terminating 50Ω to V_{CC} – 2V. For V_{CC} = 2.5V, the V_{CC} – 2V is very close to ground level. The R3 in Figure 4B can be eliminated and the termination is shown in *Figure 4C.*

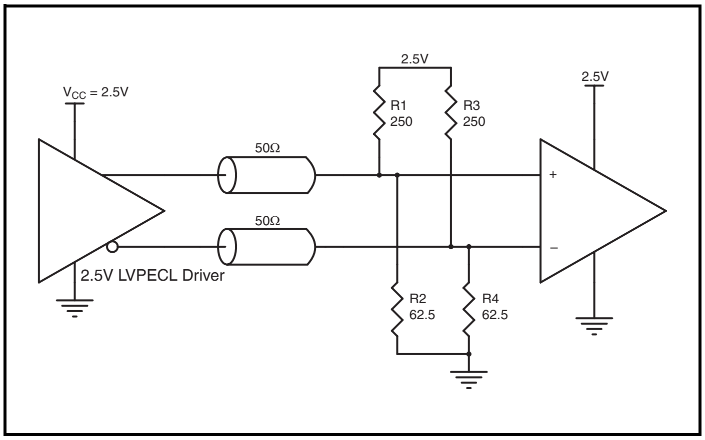


Figure 4A. 2.5V LVPECL Driver Termination Example

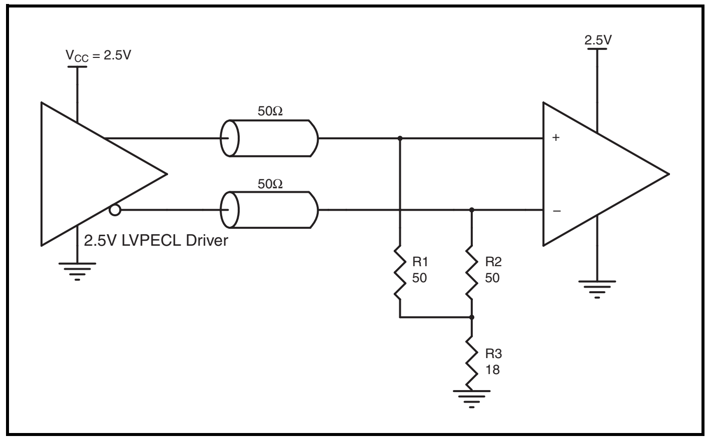


Figure 4B. 2.5V LVPECL Driver Termination Example

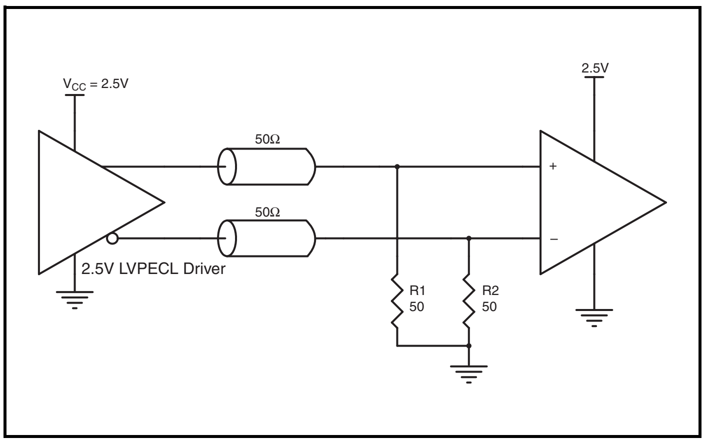


Figure 4C. 2.5V LVPECL Driver Termination Example

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS53011C.
Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS53011C is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.8V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.8V * 24mA = **91.2mW**
- Power (outputs)$_{MAX}$ = **30.94mW/Loaded Output pair**
  If all outputs are loaded, the total power is 2 * 30.94mW = **61.88mW**

Total Power$_{\_MAX}$ (3.8V, with all outputs switching) = 91.2mW + 61.88mW = **153.08mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS devices is 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow or 200 linear feet per minute and a multi-layer board, the appropriate value is 103.3°C/W per Table 5A below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 0.153W * 103.3°C/W = 100.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (single layer or multi-layer).

Table 5A. Thermal Resitance θ_{JA} for 8 Lead SOIC, Forced Convection

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 5B. Thermal Resitance θ_{JA} for 8 Lead TSSOP, Forced Convection

θ_{JA} by Velocity			
Meters Per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

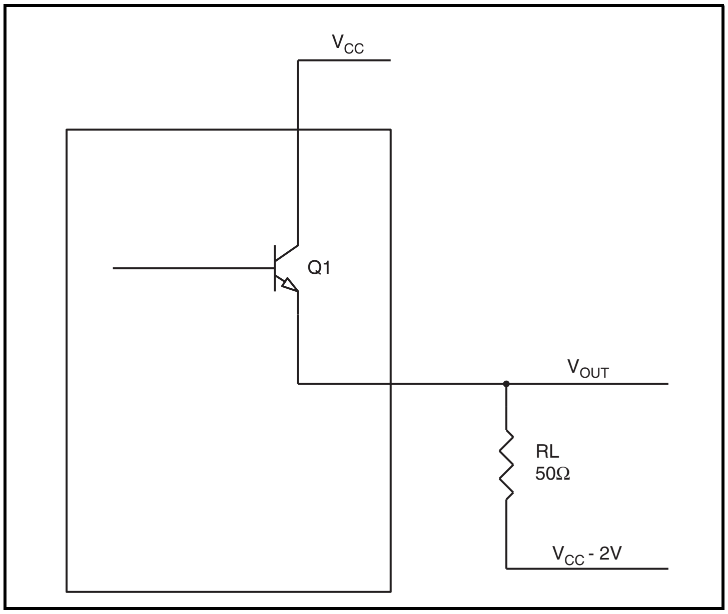


Figure 5. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CC} – 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CC\_MAX} – 0.935V}$
  $(V_{CC\_MAX} – V_{OH\_MAX})$ = **0.935V**
- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CC\_MAX} – 1.67V}$
  $(V_{CC\_MAX} – V_{OL\_MAX})$ = **1.67V**

Pd_H is power dissipation when the output drives high.

Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OH\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OH\_MAX}) =$
$[(2V – 0.935V)/50\Omega] * 0.935V =$ **19.92mW**

$Pd\_L = [(V_{OL\_MAX} – (V_{CC\_MAX} – 2V))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) = [(2V – (V_{CC\_MAX} – V_{OL\_MAX}))/R_L] * (V_{CC\_MAX} – V_{OL\_MAX}) =$
$[(2V – 1.67V)/50\Omega] * 1.67V =$ **11.02mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.94mW**

Reliability Information

Table 6A. θ_{JA} vs. Air Flow Table for an 8 Lead SOIC

θ_{JA} by Velocity			
Linear Feet per Minute	**0**	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	153.3°C/W	128.5°C/W	115.5°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	112.7°C/W	103.3°C/W	97.1°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Table 6B. θ_{JA} vs. Air Flow Table for an 8 Lead TSSOP

θ_{JA} by Velocity			
Meters Per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	101.7°C/W	90.5°C/W	89.8°C/W

Transistor Count

The transistor count for ICS853011C is: 96
Pin compatible with MC100LVEP11 and SY100EP11U

Package Outline and Package Dimension

Package Outline - G Suffix for 8 Lead TSSOP

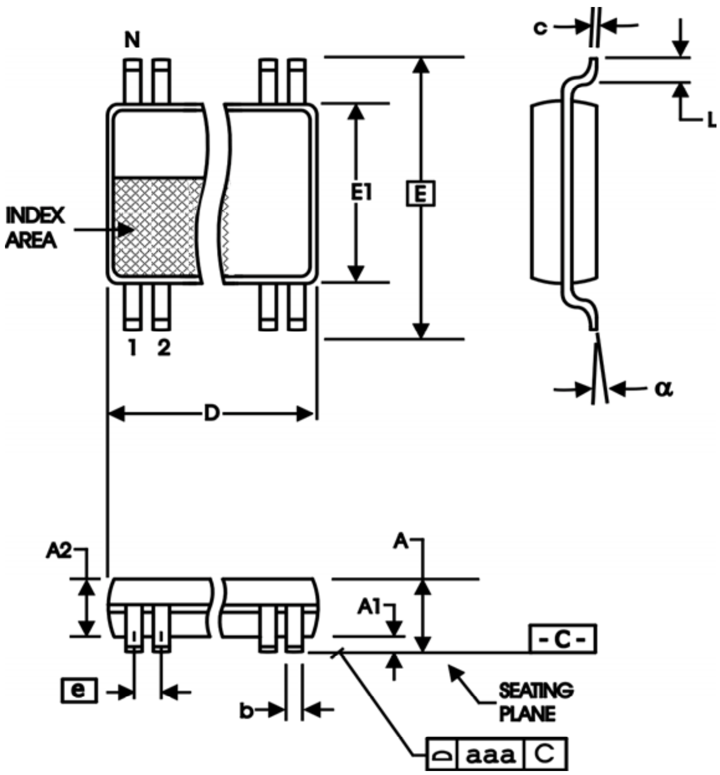


Table 7A. Package Dimensions

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A		1.10
A1	0	0.15
A2	0.79	0.97
b	0.22	0.38
c	0.08	0.23
D	3.00 Basic	
E	4.90 Basic	
E1	3.00 Basic	
e	0.65 Basic	
e1	1.95 Basic	
L	0.40	0.80
α	0°	8°
aaa		0.10

Reference Document: JEDEC Publication 95, MO-187

Package Outline - M Suffix for 8 Lead SOIC

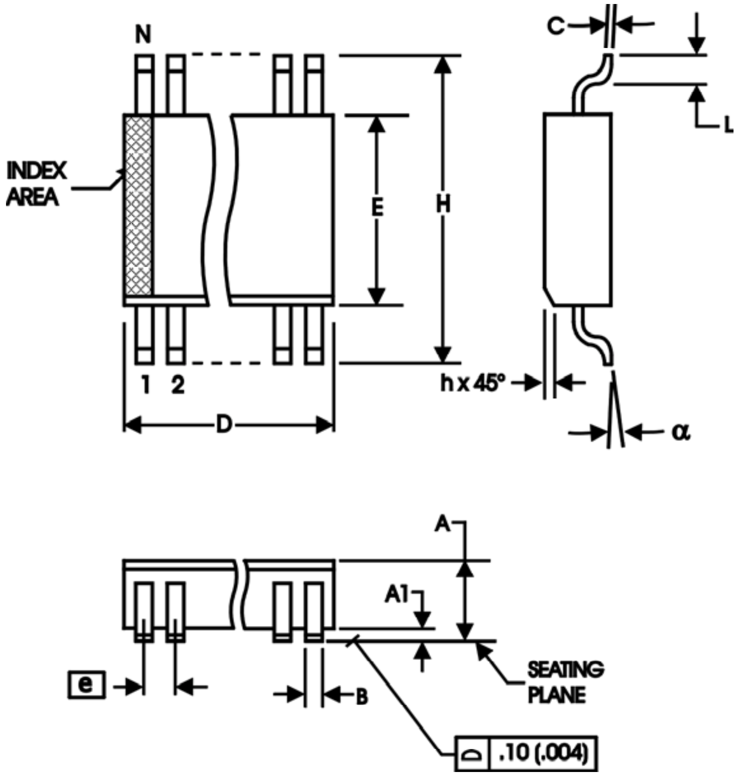


Table 7B. Package Dimensions for 8 Lead SOIC

All Dimensions in Millimeters		
Symbol	**Minimum**	**Maximum**
N	8	
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 Basic	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-012

Ordering Information

Table 8. Ordering Information

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS853011CM	853011C	8 Lead SOIC	Tube	-40°C to 85°C
ICS853011CMT	853011C	8 Lead SOIC	2500 Tape & Reel	-40°C to 85°C
ICS853011CMLF	3011CLF	“Lead-Free” 8 Lead SOIC	Tube	-40°C to 85°C
ICS853011CMLFT	3011CLF	“Lead-Free” 8 Lead SOIC	2500 Tape & Reel	-40°C to 85°C
ICS853011CG	011C	8 Lead TSSOP	Tube	-40°C to 85°C
ICS853011CGT	011C	8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C
ICS853011CGLF	11CL	“Lead-Free” 8 Lead TSSOP	Tube	-40°C to 85°C
ICS853011CGLFT	11CL	“Lead-Free” 8 Lead TSSOP	2500 Tape & Reel	-40°C to 85°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

Revision History Sheet

Rev	Table	Page	Description of Change	Date
A	T8	16	Ordering Information table - added lead-free marking for TSSOP package.	6/12/07
A	T7B	15	Corrected Package Dimensions Table for 8 Lead SOIC.	7/28/08

Contact Information:

www.IDT.com

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support
netcom@idt.com
+480-763-2056

Corporate Headquarters
Integrated Device Technology, Inc.
6024 Silver Creek Valley Road
San Jose, CA 95138
United States
800-345-7015 (inside USA)
+408-284-8200 (outside USA)