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Integrated Circuit Systems, Inc.

AV9155C

Low Cost 20-Pin Frequency Generator

General Description

The **AV9155C** is a low cost frequency generator designed specifically for desktop and notebook PC applications with either 3.3V or 5.0V power supply voltage. Its CPU clocks provide all necessary CPU frequencies for 286, 386 and 486 systems, including support for the latest speeds of processors. The device uses a 14.318 MHz crystal to generate the CPU and all peripheral clocks for integrated desktop motherboards.

The dual 14.318 MHz clock outputs allows one output for the system and one to be the input to an ICS graphics frequency generator such as the AV9194.

The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this ideal device to use whenever slowing the CPU speed. The **AV9155C** makes a gradual transition between frequencies, so that it obeys the Intel cycle-to-cycle timing specification for 486 systems. The simultaneous 2X and 1X CPU clocks offer controlled skew to within 1.5ns (max) of each other.

ICS offers several versions of the **AV9155C**. The different devices are shown below:

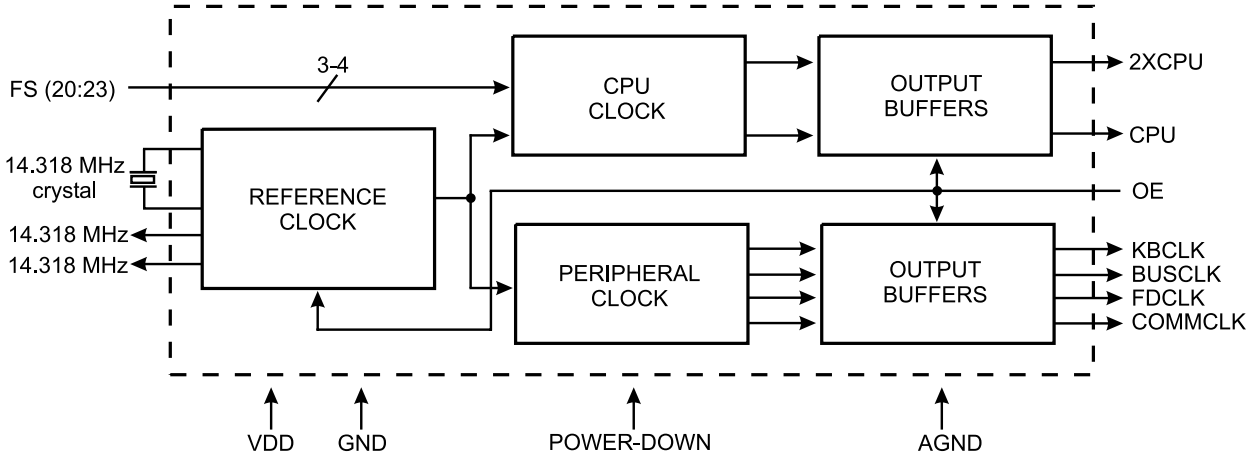
PART	DESCRIPTION
AV9155C-01	Motherboard clock generator with 16 MHz BUS CLK
AV9155C-02	Motherboard clock generator with 32 MHz BUS CLK
AV9155C-23	Includes Pentium™ frequencies
AV9155C-36	Features a special 40 MHz SCSI clock

Features

- Compatible with 286, 386, and 486 CPUs
- Supports turbo modes
- Generates communications clock, keyboard clock, floppy disk clock, system reference clock, bus clock and CPU clock
- Output enable tristates outputs
- Up to 100 MHz at 5V or 3.3V
- 20-pin DIP or SOIC
- All loop filter components internal
- Skew-controlled 2X and 1X CPU clocks
- Power-down option

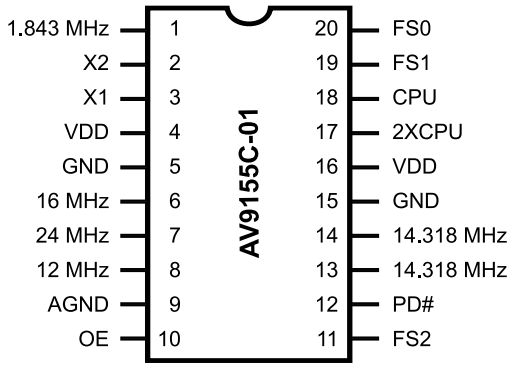
ICS has been shipping motherboard frequency generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The **AV9155C** is a third generation device, and uses ICS's patented analog CMOS phase-locked loop technology for low phase jitter. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost-effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

Block Diagram

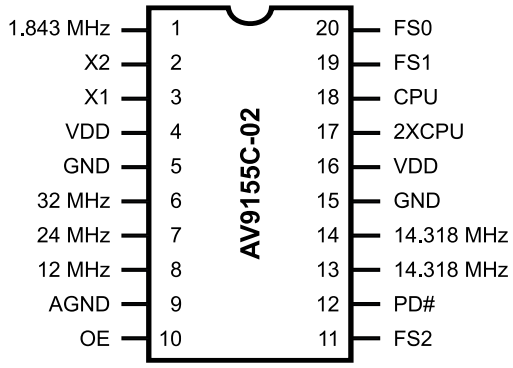


Pentium is a trademark of Intel Corporation.

Pin Configuration



20-Pin DIP or SOIC



20-Pin DIP or SOIC

Pin Descriptions for AV9155C-01, -02

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	1.843 MHz	Output	1.84 MHz clock output.
2	X2	Output	Crystal connection.
3	X1	Input	Crystal connection.
4	VDD	-	Digital power supply (3.3V or 5.0V).
5	GND	-	Digital Ground.
6	16 MHz/32 MHz	Output	16 MHz (-01) or 32 MHz (-02) clock output.
7	24 MHz	Output	24 MHz floppy disk/combination I/O clock output.
8	12 MHz	Output	12 MHz keyboard clock output.
9	AGND	-	Analog ground (original version).
10	OE	Input	Output enable. Tristates all outputs when low. (Has internal pull-up.)
11	FS2	Input	CPU clock frequency select #2. (Has internal pull-up.)
12	PD#	Input	Power-down. Shuts off entire chip when low. (Has internal pull-up.)
13	14.318 MHz	Output	14.318 MHz reference clock output.
14	14.318 MHz	Output	14.318 MHz reference clock output.
15	GND	-	Digital ground.
16	VDD	-	Digital power supply (3.3V or 5.0V).
17	2XCPU	Output	2X CPU clock output.
18	CPU	Output	1X CPU clock output.
19	FS1	Input	CPU clock frequency select #1. (Has internal pull-up.)
20	FS0	Input	CPU clock frequency select #0. (Has internal pull-up.)

Functionality - AV9155C-01

(Using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

FS2 (Pin 11)	FS1 (Pin 19)	FS0 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	100*	50*

*V_{DD} minimum 3.15V.

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Functionality - AV9155C-02

(Using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

FS2 (Pin 11)	FS1 (Pin 19)	FS0 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	32	16
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	100*	50*

* V_{DD} minimum 3.15V

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	32	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

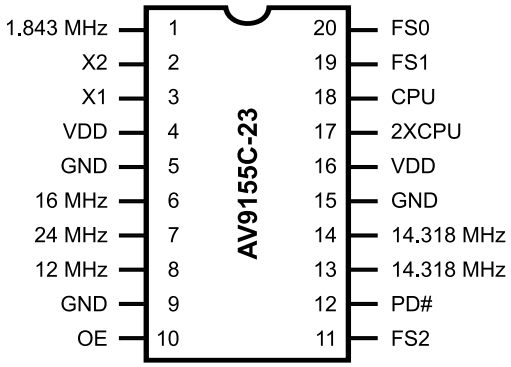
Frequency Transitions

A key feature of the **AV9155C** is its ability to provide smooth, glitch-free frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. These frequency transitions do not violate the Intel 486 specification of less than 0.1% frequency change per clock period.

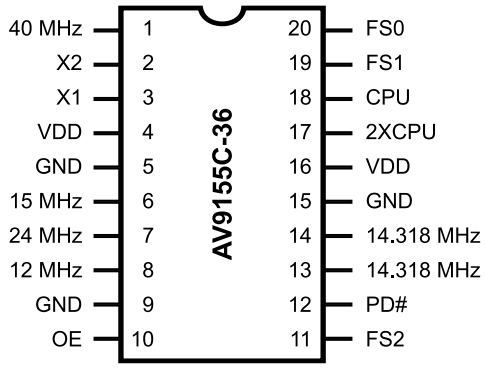
Using an Input Clock as Reference

The **AV9155C** is designed to accept a 14.318 MHz crystal as the input reference. With some external changes, it is possible to use a crystal oscillator or clock input. Please see application note AN04 for details on driving the **AV9155C** with a clock.

Pin Configuration



20-Pin DIP or SOIC



20-Pin DIP or SOIC

Pin Descriptions for AV9155C-23, -36

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	1.843/40 MHz	Output	1.84 MHz (-23)/40 MHz SCSI (-36) clock output.
2	X2	Output	Crystal connection.
3	X1	Input	Crystal connection.
4	VDD	-	Digital power supply (3.3V or 5.0V).
5	GND	-	Digital ground.
6	16 MHz/15 MHz	Output	16 MHz (-23)/15 MHz (-36) clock output.
7	24 MHz	Output	24 MHz floppy disk/combination I/O clock output.
8	12 MHz	Output	12 MHz keyboard clock output.
9	AGND	-	Analog ground (original version).
10	OE	Input	Output enable. Tristates all outputs when low. (Has internal pull-up.)
11	FS2	Input	CPU clock frequency select #2. (-23 has internal pull-up.)
12	PD#	Input	Power-down. Shuts off entire chip when low. (Has internal pull-up.)
13	14.318 MHz	Output	14.318 MHz reference clock output.
14	14.318 MHz	Output	14.318 MHz reference clock output.
15	GND	-	Digital ground.
16	VDD	-	Digital power supply (3.3V or 5.0V).
17	2XCPU	Output	2X CPU clock output.
18	CPU	Output	1X CPU clock output.
19	FS1	Input	CPU clock frequency select #1. (-23 has internal pull-up.)
20	FS0	Input	CPU clock frequency select #0. (-23 has internal pull-up.)

Functionality - AV9155C-23

(Using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

FS2 (Pin 11)	FS1 (Pin 19)	FS0 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	75*	37.5*
0	0	1	32	16
0	1	0	60	30
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	52	26

*V_{DD} minimum 3.15V

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.843	16	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Functionality - AV9155C-36

(Using 14.318 MHz input. All frequencies in MHz.)

CLOCK#2 CPU and 2XCPU

FS2 (Pin 11)	FS1 (Pin 19)	FS0 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8	4
0	0	1	16	8
0	1	0	60	30
0	1	1	40	20
1	0	0	50	25
1	0	1	66.66	33.33
1	1	0	80*	40*
1	1	1	100*	50*

*V_{DD} minimum 3.15V

PERIPHERAL CLOCKS

SCSICLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
40	15	24	12

REFERENCE CLOCKS

REFCLK1 (Pin 13)	REFCLK2 (Pin 14)
14.318	14.318

Absolute Maximum Ratings

VDD referenced to GND 7V
Voltage on I/O pins referenced to GND. . . . . GND -0.5V to VDD +0.5V
Operating temperature under bias. . . . . 0°C to +70°C
Power dissipation . . . . . 0.5 Watts
Storage temperature . . . . . -40°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} = 4.0 to 5.5V (5V +10%/-20%); $T_{A=0}$°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL	VDD=5V	-	-	0.8	V
Input High Voltage	VIH	VDD=5V	2.0	-	-	V
Input High Voltage, PD#	VIHPD	VDD=5V, for PD# input	2.2	-	-	V
Input Low Current	IIL	VIN=0V (pull-up pin)	-	16	35	µA
Input High Current	IIH	VIN=VDD	-5	0	5	µA
Output Low Voltage	VOL	IOL=8mA	-	0.15	0.4	V
Output High Voltage [1]	VOH	IOH=-25mA	2.4	3.7	-	V
Output Low Current [1]	IOL	VOL=0.8	15	32	-	mA
Output High Current [1]	IOH	VOH=2.0V	-	-48	-30	mA
Supply Current	IDD	Unloaded, 66 MHz	-	38	60	mA
Supply Current, Power-down	IDDPD	SCLKx=000 PD#=0	-	0.7	1.5	mA
Output Frequency Change over Supply and Temperature [1]	FD	With respect to typical frequency	-	0.002	0.01	%
Short circuit current [1]	ISC	Each output clock	25	40	-	mA
Input Capacitance [1]	CI	Except X1, X2	-	-	10	pF
Load Capacitance [1]	CL	Pins X1, X2	-	20	-	pF
Pull-up Resistor [1]	Rpu	at VIN=VDD-1V	120	350	700	k ohm

Notes:
1 Parameter is guaranteed by design and characterization, not subject to production testing.

Electrical Characteristics at 5V

V_{DD} = 4.0 to 5.5V (5V +10%/-20%); $T_{A=0}$°C to 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time [1]	tICr		-	-	20	ns
Input Clock Fall Time [1]	tICf		-	-	20	ns
Output Rise time [1]	tr	25pF load, 0.8 to 2.0V	-	1.5	2	ns
Rise time [1]	tr	25pF load, 20% to 80% VDD	-	2.0	4.0	ns
Output Fall time [1]	tf	25pF load, 2.0 to 0.8V	-	1.0	2.0	ns
Fall time [1]	tf	25pF load, 80% to 20% VDD	-	1.3	3.0	ns
Duty cycle [1]	dt	25pF load at 1.4V	45/55	48/52	55/45	%
Duty cycle,[1] reference clocks	dt	25pF load at 1.4V	36	43	50	%
Jitter, one sigma [1] , 20 to 50 MHz clocks [1] on CPU and 40 to 100 MHz on 2XCPU	tjls1	10,000 cycles	-	0.8	2.0	%
Jitter, one sigma [1] , fixed clock & clocks below 20 MHz on CPU, below 40 MHz on 2XCPU	tjls2	10,000 cycles	-	0.8	2.0	%
Jitter, absolute [1] , 20 to 50 MHz clocks [1] on CPU and 40 to 100 MHz on 2XCPU	tjab1	10,000 cycles	-4.0	2.0	4.0	%
Jitter, absolute [1] , fixed clock & clocks below 20 MHz on CPU, below 40 MHz on 2XCPU	tjab2	10,000 cycles	-5.0	2.0	5.0	%
Input Frequency [1]	fin		2	14.318	32	MHz
Maximum Output Frequency [1]	fout	at 2XCPU	100	220		MHz
Clock skew between CPU and 2XCPU outputs [1]	Tsk		-	140	400	ps
Power-up Time [1]	ttPO	to 66 MHz	-	8	15	ms
Frequency Transition Time [1]	tft	from 8 to 66.66 MH	-	6.5	12	ms
		from 32 to 80 MHz	-	1.8	3.2	ms
		from 80 to 32 MHz	-	2.5	5.0	ms

Notes:
1 Parameter is guaranteed by design and characterization, not subject to production testing.

Electrical Characteristics at 3.3V

V_{DD} =3.0V to 3.7V, $T_{A=0}$°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	VIL	VDD=3.3V	-	-	0.2VDD	V
Input High Voltage	VIH	VDD=3.3V	0.7VDD	-	-	V
Input High Voltage, PD#	VIHPD	VDD=3.3V, for PD# input	2.2	-	-	V
Input Low Current	IIL	VIN=0V (pull-up pin)	-	11	25	µA
Input High Current	IIH	VIN=VDD	-5	0	5	µA
Output Low Voltage	VOL	IOL=4mA	-	0.05VDD	0.1VDD	V
Output High Voltage [1]	VOH	IOH=-3.5mA	-	0.94VDD	-	V
Output Low Current [1]	IOL	VOL=0.2VDD	12	22	-	mA
Output High Current [1]	IOH	VOH=0.7VDD	-	-11	-6.5	mA
Supply Current	IDD	Unloaded, 66.6 MHz	-	28	45	mA
Supply Current, Power-down	IDDPD	SCLKx=000 PD#=0	-	0.25	0.5	mA
Output Frequency Change over Supply and Temperature [1]	FD	With respect to typical frequency	-	0.002	0.01	%
Short circuit current [1]	ISC	Each output clock	20	30	-	mA
Input Capacitance [1]	CI	Except X1, X2	-	-	10	pF
Load Capacitance [1]	CL	Pins X1, X2	-	20	-	pF
Pull-up Resistor [1]	Rpu	at VIN=VDD-1V	120	330	650	k ohm

Notes:
1 Parameter is guaranteed by design and characterization, not subject to production testing.

Electrical Characteristics at 3.3V

V_{DD} = +3.3V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Clock Rise Time [1]	tICr		-	-	20	ns
Input Clock Fall Time [1]	tICf		-	-	20	ns
Rise time [1]	tr	25pF load, 20% to 80% VDD	-	3.0	4.0	ns
Fall time [1]	tf	25pF load, 80% to 20% VDD	-	1.8	2.5	ns
Duty cycle [1]	dt	25pF load at 50% VDD	40	48	60	%
Duty cycle,[1] reference clocks	dt	25pF load at 50% VDD	33	36	67	%
Jitter, one sigma [1]	tjls1	10,000 cycles	-	0.8	2.5	%
Jitter, absolute [1]	tjab1	10,000 cycles	-5.0	2.0	5.0	%
Input Frequency [1]	fin		2	14.318	32	Mhz
Maximum Output Frequency [1,2]	fout	at 2XCPU	7	140	-	MHz
Clock skew between CPU and 2XCPU outputs [1]	Tsk		100	220	500	ps
Power-up Time [1]	ttPO	to 66 MHz	-	6	12	ms
Frequency Transition Time [1]	tft	from 8 to 50.0 MHz	-	6	12	ms

Notes:
1 Parameter is guaranteed by design and characterization, not subject to production testing.
2 Output frequencies on 2XCPU of 80 or 100 MHz require minimum V_{DD} of 3.15V (3.3 -5%).

Actual Output Frequencies

(Using 14.318 MHz input. All frequencies in MHz.)

AV9155C-01 and AV9155C-02

CLOCK#2 CPU and 2XCPU

FS2 (Pin 11)	FS1 (Pin 19)	FS0 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	7.50	3.75
0	0	1	15.51	7.76
0	1	0	32.22	16.11
0	1	1	40.09	20.05
1	0	0	50.11	25.06
1	0	1	66.82	33.41
1	1	0	80.18	40.09
1	1	1	100.23	50.11

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	32.01 or 16.00	24.00	12.00

AV9155C-23

CPU CLOCK

FS2 (Pin 11)	FS1 (Pin 19)	FS0 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	75.170	37.585*
0	0	1	31.940	15.970
0	1	0	60.136	30.068
0	1	1	40.090	20.045
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	80.181	40.091
1	1	1	51.903	25.952

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 6)	FDCLK (Pin 7)	KBCLK (Pin 8)
1.846	16.00	24.00	12.00

AV9155C-36

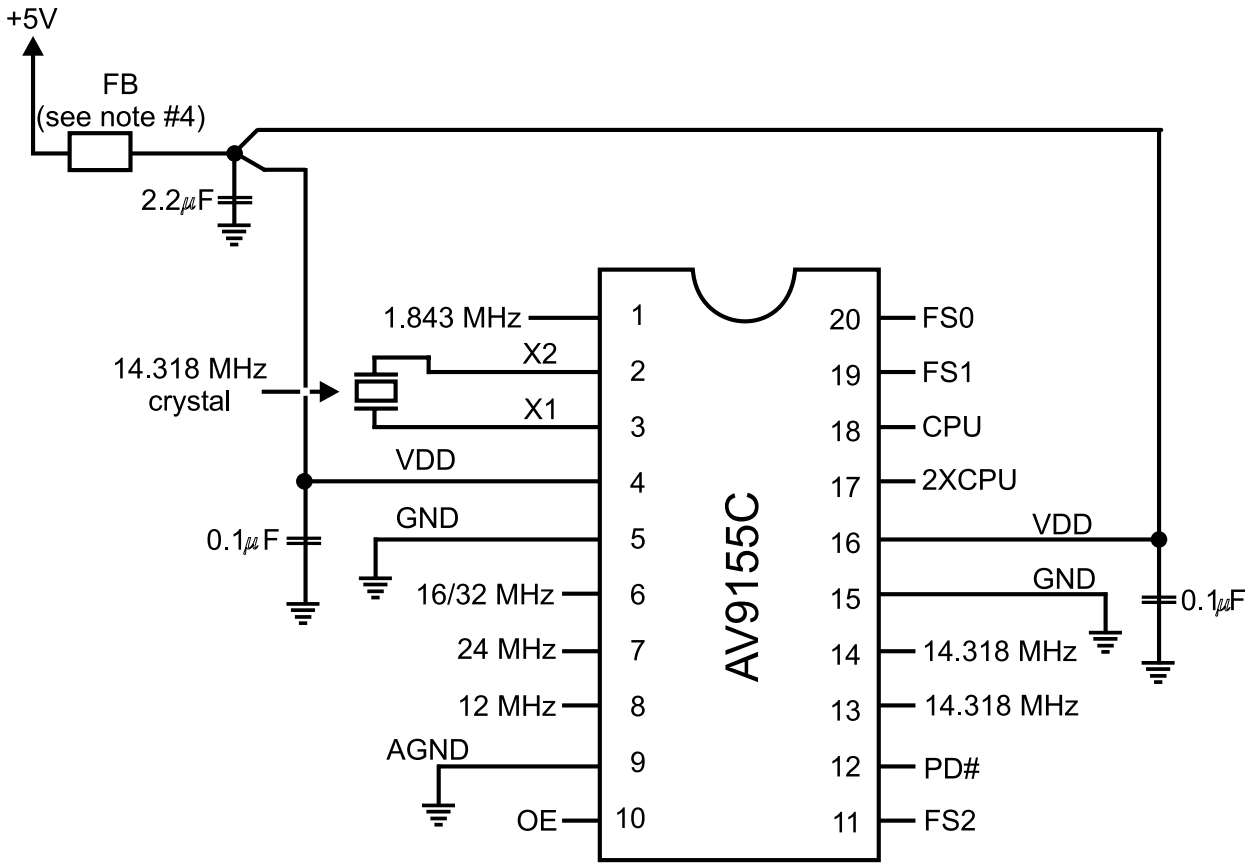
CPU CLOCK

FS2 (Pin 11)	FS1 (Pin 19)	FS0 (Pin 20)	2XCPU (Pin 17)	CPU (Pin 18)
0	0	0	8.054	4.027
0	0	1	16.002	8.001
0	1	0	59.875	29.936
0	1	1	39.886	19.943
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	80.181	40.091
1	1	1	100.226	50.113

PERIPHERAL CLOCKS

COMMCLK (Pin 1)	BUSCLK (Pin 7)	FDCLK (Pin 6)	KBCLK (Pin 8)
40.00	15.00	24.00	12.00

AV9155C Recommended External Circuit



Notes:

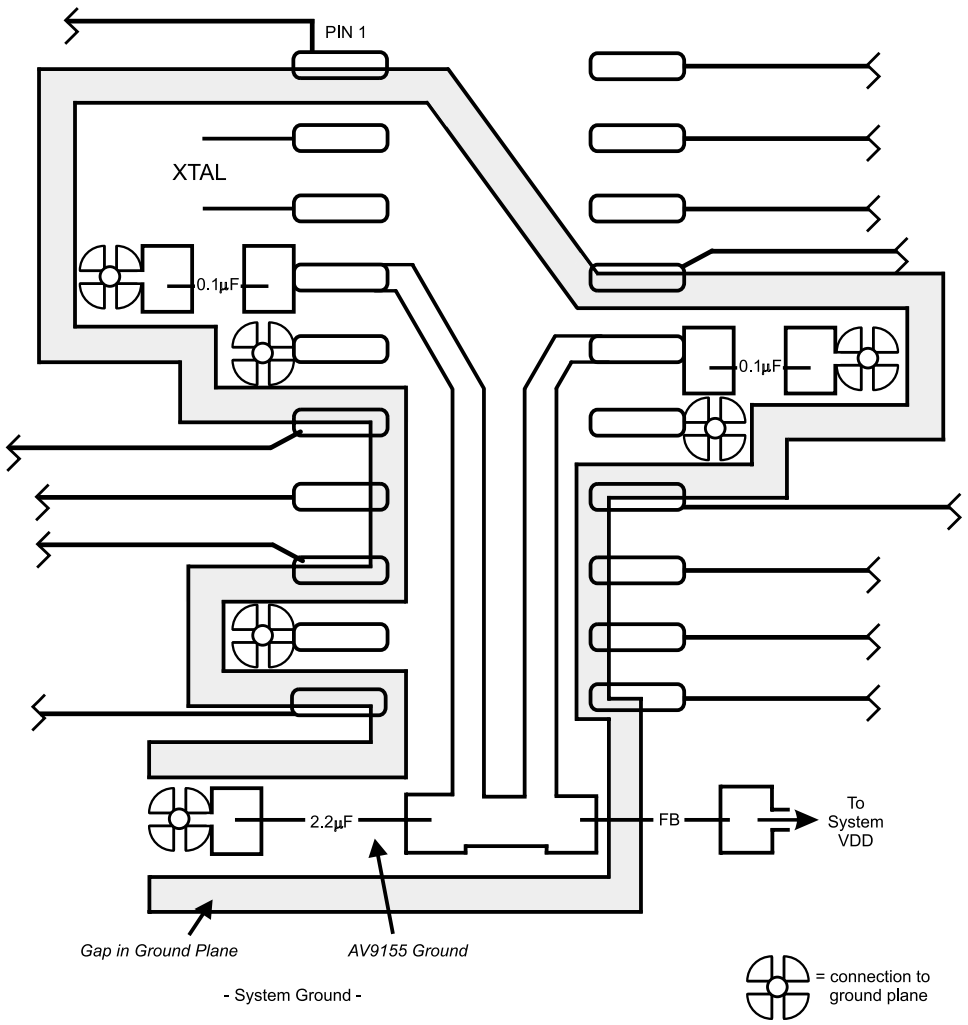
1. ICS recommends the use of an isolated ground plane for the **AV9155C**. All grounds shown on this drawing should be connected to this ground plane. This ground plane should be connected to the system ground plane at a single point. Please refer to **AV9155C** Board Layout Diagram.

2. A single power supply connection for all VDD lines at the 2.2**µ**F decoupling capacitor is recommended to reduce interaction of analog and digital circuits. The 0.1**µ**F decoupling capacitors should be located as close to each VDD pin as possible.

3. A 33**Ω** series termination resistor should be used on any clock output which drives more than one load or drives a long trace (more than about two inches), especially when using high frequencies (>50 MHz). This termination resistor is put in series with the clock output line close to the clock output. It helps improve jitter performance and reduce EMI by damping standing waves caused by impedance mismatches in the output clock circuit trace.

4. The ferrite bead does not enhance the performance of the **AV9155C**, but will reduce EMI radiation from the VDD line.

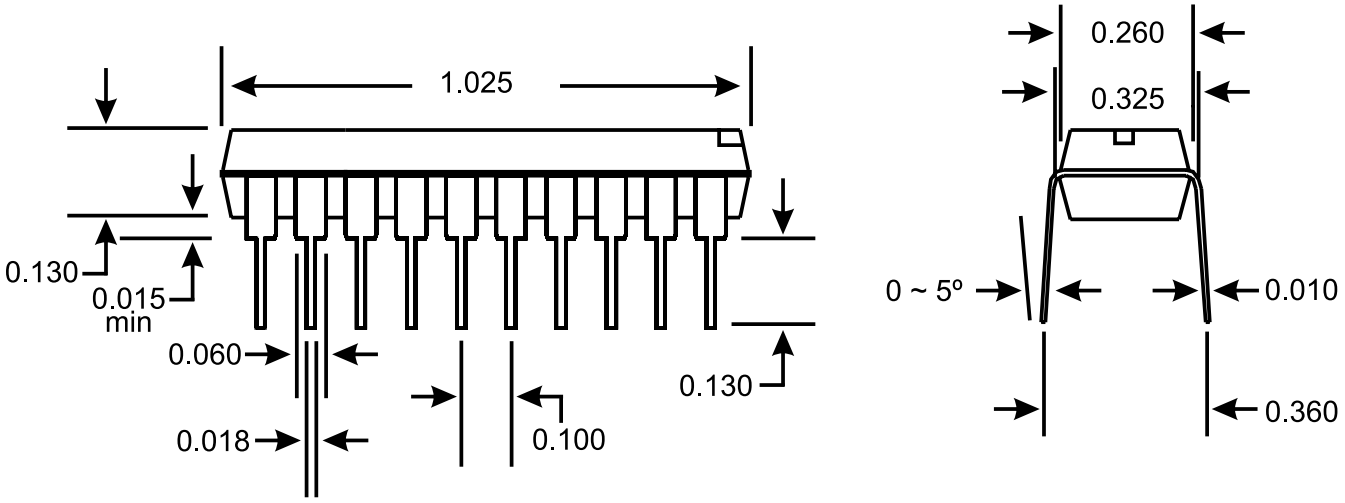
AV9155C Recommended Board Layout



This is the recommended layout for the **AV9155C** to maximize clock performance. Shown are the power and ground connections, the ground plane, and the input/output traces.

Use of the isolated ground plane and power connection, as shown, will prevent stray high frequency ground and system noise from propagating through the device. When compared to using the system ground and power planes, this technique will minimize output clock jitter. The isolated ground plane should be connected to the system ground plane at one point, near the 2.2µF decoupling cap. For lowest jitter performance, this isolated ground plane should be kept away from clock output pins and traces. Keeping the isolated ground plane area as small as possible will minimize EMI radiation. Use a sufficient gap between the isolated ground plane and system ground plane to prevent AC coupling. The ferrite bead in the VDD line optional, but will help reduce EMI.

The traces to distribute the output clocks should be over a system ground or power supply plane. The trace width should be about two times the thickness of the PC board between the trace and the underlying plane. These guidelines help minimize clock jitter and EMI radiation. The traces to distribute power should be as wide as possible.



20-Pin DIP Package

Ordering Information

AV9155C-02CN20,
AV9155C-23CN20, AV9155C-36CN20

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

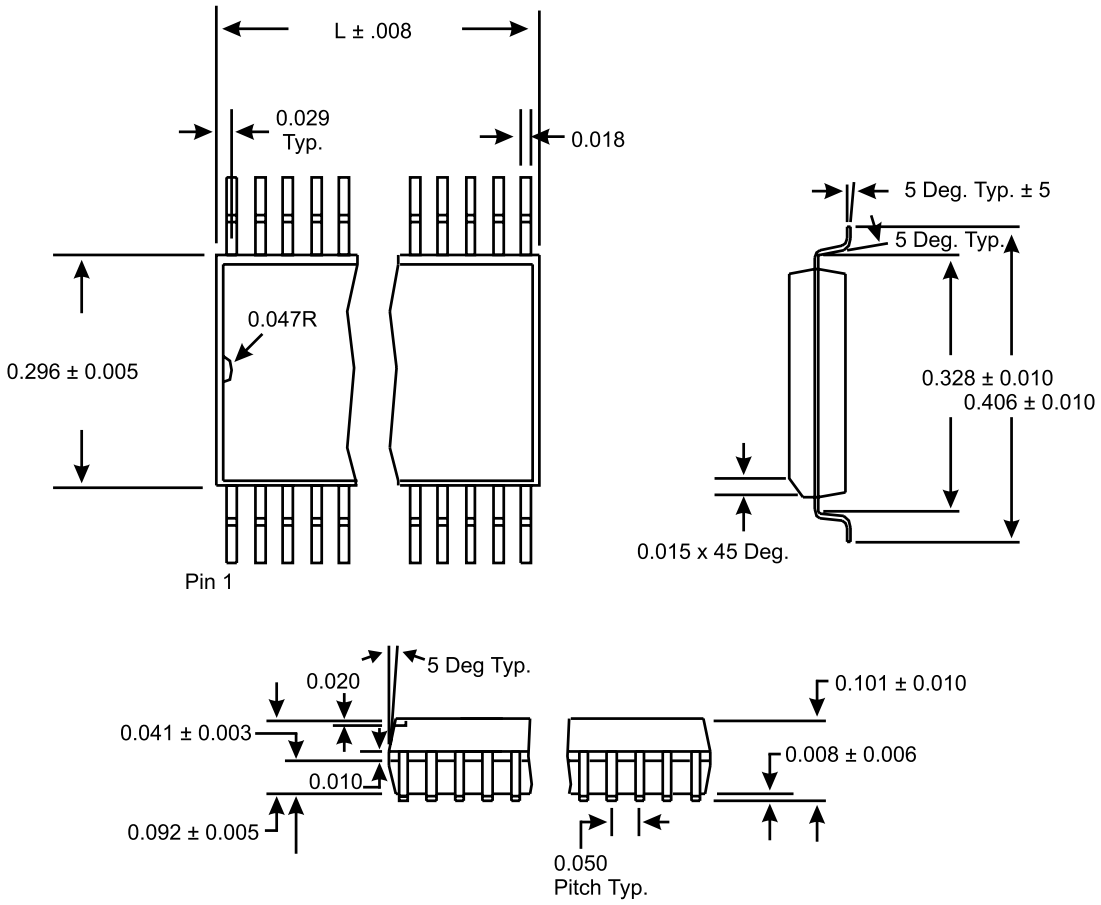
Package Type
N=DIP (Plastic#) T&R=Tape and Reel

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device

Notes:
Tape and reel packaging should be ordered with the suffix T&R. For instance, if the -01 in DIP and tape & reel is required, order the part as AV9155C-01CN20T&R.



LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	0.354	0.404	0.454	0.504	0.604	0.704	0.804

Ordering Information

AV9155C-01CW20, AV9155C-02CM20,
AV9155C-23CM20, AV9155C-36CM20

Example:

ICS XXXX-PPP M X#W

Lead Count & Package Width
Lead Count=1, 2 or 3 digits
W=.3" SOIC or .6" DIP; None=Standard Width

Package Type
W=SOIC T&R=Tape and Reel

Pattern Number (2 or 3 digit number for parts with ROM code patterns)

Device Type (consists of 3 or 4 digit numbers)

Prefix
ICS, AV=Standard Device