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Integrated Circuit Systems, Inc.

ICS9248-192

Frequency Timing Generator for Transmeta Systems

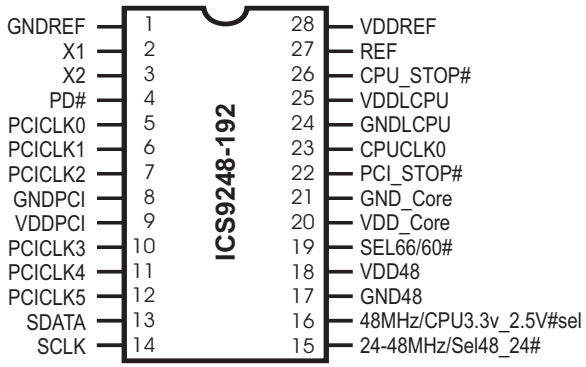
Recommended Application:
Transmeta

Output Features:
- 1CPU(2.5V or 3.3V selectable) up to 66.6MHz & overclocking of 66MHz.
- 6 PCI (3.3V) @ 33.3MHz (all are free running selectable).
- 1 REF (3.3V) at 14.318MHz.
- 1 48MHz (3.3V).
- 1 24_48MHz selectable output.

Features:
- Supports Spread Spectrum modulation for CPU and PCI clocks, default -0.4 downspread.
- Efficient Power management scheme through stop clocks and power down modes.
- Uses external 14.318MHz crystal, no external load cap required for CL=18pF crystal.
- 28-pin TSSOP package, 4.40mm (173mil).

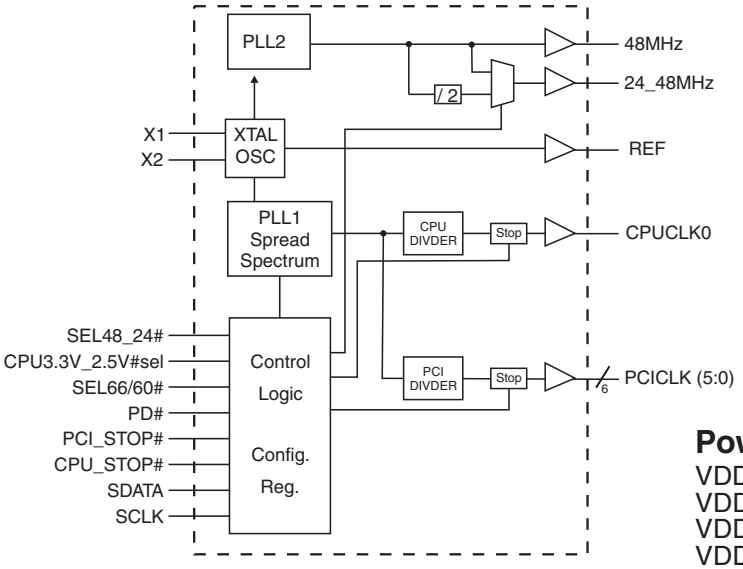
Skew Characteristics:
- CPU – CPU ≤175ps
- PCI – PCI ≤ 500ps
- CPU(early) – PCI = 1.5ns – 4ns.

Pin Configuration



28-Pin TSSOP

Block Diagram



Power Groups

VDD_Core, GND_Core = PLL core
VDDREF, GNDREF = REF, X1, X2
VDDPCI, GNDPCI = PCICLK (5:0)
VDD48, GND48 = 48MHz (1:0)

Pin Descriptions

Pin number	Pin name	Type	Description
1	GNDREF	Power	Ground for 14.318 MHz reference clock outputs
2	X1	Input	14.318 MHz crystal input
3	X2	Output	14.318 MHz crystal output
4	PD#	Input	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 3ms.
12, 11, 10, 7, 6, 5	PCICLK (5:0)	Output	3.3V PCI clock outputs, free running selectable
8	GNDPCI	Power	Ground for PCI clock outputs
9	VDDPCI	Power	3.3V power for the PCI clock outputs
15	Sel48_24#	Input	Selects 24MHz (0) or 48MHz (1) output
	24_48MHz	Output	Selectable output either 24MHz or 48MHz
13	SDATA	I/O	Data pin for I^2C circuitry 5V tolerant
14	SCLK	IN	Clock pin of I^2C circuitry 5V tolerant
16	CPU3.3-2.5#	Input	3.3 (1) or 2.5 (0) VDD buffer strength selection, has pullup to VDD, nominal 30K resistor.
	48MHz	Output	3.3V 48 MHz clock output, fixed frequency clock typically used with USB devices
17	GND48	Power	Ground for 48 MHz clocks
18	VDD48	Power	3.3V power for 48/24 MHz clocks
19	SEL 66/60#	Input	Control for the frequency of clocks at the CPU & PCICLK output pins. "0" = 60 MHz. "1" = 66.6 MHz. The PCI clock is multiplexed to run at 33.3 MHz for both selected cases.
20	VDD_Core	Power	Isolated 3.3V power for core
21	GND_Core	Power	Isolated ground for core
22	PCI_Stop#	Input	Synchronous active low input used to stop the PCICLK in active low state. It will not effect PCICLK_F or any other outputs.
23	CPUCLK0	Output	CPU clock outputs selectable 2.5V or 3.3V.
24	GNDLCPU	Power	Ground for CPU clock outputs
25	VDDLCPU	Power	2.5V or 3.3V power for CPU clock outputs
26	CPU_STOP#	Input	Asynchronous active low input pin used to stop the CPUCLK in active low state, all other clocks will continue to run. The CPUCLK will have a "Turnon " latency of at least 3 CPU clocks.
27	REF	Output	3.3V 14.318 MHz reference clock output
28	VDDREF	Power	3.3V power for 14.318 MHz reference clock outputs.

CPU Select Functions

SEL 66/60#	CPU (MHz)
0	60MHz
1	66.6MHz

Power Management

Clock Enable Configuration

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	REF	Crystal	VCOs
X	X	0	Low	Low	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running
0	1	1	Low	33.3 MHz	Running	Running	Running
1	0	1	60/66.6MHz	Low	Running	Running	Running
1	1	1	60/66.6MHz	33.3 MHz	Running	Running	Running

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. During power up and power down operations using the PD# pin will not cause clocks of a short or longer pulse than that of the running clock. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

ICS9248-192 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency No. of rising edges of free running PCICLK
CPU_ STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PCI_STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PD#	1 (Normal Operation)[3]	3ms
	0 (Power Down)[4]	2max

Notes.
1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, PCICLK only.
   The REF will be stopped independant of these.

General I²C serial interface information

The information in this section assumes familiarity with I²C programming.

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address D2 (H)
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy command code
- ICS clock will ***acknowledge***
- Controller (host) sends a dummy byte count
- ICS clock will ***acknowledge***
- Controller (host) starts sending first byte (Byte 0) through byte 6
- ICS clock will ***acknowledge*** each byte ***one at a time***.

How to Write:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D2(H)	
	ACK
Dummy Command Code	
	ACK
Dummy Byte Count	
	ACK
Byte 0	
	ACK
Byte 1	
	ACK
Byte 2	
	ACK
Byte 3	
	ACK
Byte 4	
	ACK
Byte 5	
	ACK
Byte 6	
	ACK
Stop Bit	

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the read address D3 (H)
- ICS clock will ***acknowledge***
- ICS clock will send the ***byte count***
- Controller (host) acknowledges
- ICS clock sends first byte ***(Byte 0) through byte 6***
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a stop bit

How to Read:	
Controller (Host)	**ICS (Slave/Receiver)**
Start Bit	
Address D3(H)	
	ACK
	Byte Count
ACK	
	Byte 0
ACK	
	Byte 1
ACK	
	Byte 2
ACK	
	Byte 3
ACK	
	Byte 4
ACK	
	Byte 5
ACK	
	Byte 6
ACK	
Stop Bit	

Notes:

1. The ICS clock generator is a slave/receiver, I²C component. It can read back the data stored in the latches for verification. **Read-Back will support Intel PIIX4 "Block-Read" protocol**.
2. The data transfer rate supported by this clock generator is 100K bits/sec or less (standard mode)
3. The input is operating at 3.3V logic levels.
4. The data byte format is 8 bit bytes.
5. To simplify the clock generator I²C interface, the protocol is set to use only "**Block-Writes**" from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The Command code and Byte count shown above must be sent, but the data is ignored for those two bytes. The data is loaded until a Stop sequence is issued.
6. At power-on, all registers are set to a default condition, as shown.

Serial Configuration Command Bitmap

Byte0: Functionality and Frequency Select Register (default = 0)

Bit	Bit2 FS4	Bit7 FS3	Bit6 FS2	Bit5 FS1	Bit4 FS0	CPU	PCI	Spread %	PWD
Bit 2,7:4	0	0	0	0	0	60	30	-0.4 % down spread	00000
	0	0	0	0	1	60	30	-0.6 % down spread	
	0	0	0	1	0	60	30	-0.8 % down spread	
	0	0	0	1	1	60	30	-1.0 % down spread	
	0	0	1	0	0	66.6	33.3	-0.4 % down spread	
	0	0	1	0	1	66.6	33.3	-0.6 % down spread	
	0	0	1	1	0	66.6	33.3	-0.8 % down spread	
	0	0	1	1	1	66.6	33.3	-1.0 % down spread	
	0	1	0	0	0	67.32	33.66	2% over-clocking	
	0	1	0	0	1	68.64	34.32	4% over-clocking	
	0	1	0	1	0	69.96	34.98	6% over-clocking	
	0	1	0	1	1	72.6	36.3	10% over-clocking	
	0	1	1	0	0	61.5	30.75	over-clocking	
	0	1	1	0	1	63	31.5	over-clocking	
	0	1	1	1	0	64	32	over-clocking	
	0	1	1	1	1	65	32.5	over-clocking	
	1	0	0	0	0	60	30	+/- 0.5% center spread	
	1	0	0	0	1	66.6	33.3	+/- 0.5% center spread	
	1	0	0	1	0	50	25	under-clocking	
	1	0	0	1	1	48	24	under-clocking	
	1	0	1	0	0	58.8	29.4	2% under-clock	
	1	0	1	0	1	57.6	28.8	4% under-clock	
	1	0	1	1	0	56.4	28.2	6% under-clock	
	1	0	1	1	1	54	27	10% under-clock	
	1	1	0	0	0	60	30	-1.4 % down spread	
	1	1	0	0	1	60	30	-1.6 % down spread	
	1	1	0	1	0	60	30	-1.8 % down spread	
	1	1	0	1	1	60	30	-2.0 % down spread	
	1	1	1	0	0	66.6	33.3	-1.4 % down spread	
	1	1	1	0	1	66.6	33.3	-1.6 % down spread	
	1	1	1	1	0	66.6	33.3	-1.8 % down spread	
	1	1	1	1	1	66.6	33.3	-2.0 % down spread	
		Hardware latch inputs can only access these frequencies							
Bit3	0-Frequency is seleced by hardware select. Latched input								0
	1-Frequency is seleced by Bit 2, 7:4								
Bit1	0-Normal 1-Spread spectrun Enabled								0
Bit0	0-Running 1-Tristate all outputs								0

Note: PWD = Power-Up Default

Byte 1: PCI Stop

BIT	PIN#	PWD	DESCRIPTION
Bit 7	12	1	PCICLK5
Bit 6	11	1	PCICLK4
Bit 5	10	1	PCICLK3
Bit 4	7	1	PCICLK2
Bit 3	6	1	PCICLK1
Bit 2	5	1	PCICLK0
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Note:
1 = Inactive
0 = Active

Byte 2: Stop Clocks

BIT	PIN#	PWD	DESCRIPTION
Bit 7	16	1	48MHz
Bit 6	15	1	48_24MHz
Bit 5	23	1	CPUCLK0
Bit 4	27	1	REF
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Note:
1 = Inactive
0 = Active

Byte 3:Free-Running Enable

BIT	PIN#	PWD	DESCRIPTION
Bit 7	12	1	PCICLK5
Bit 6	11	1	PCICLK4
Bit 5	10	1	PCICLK3
Bit 4	7	1	PCICLK2
Bit 3	6	1	PCICLK1
Bit 2	5	1	PCICLK0
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Note:
0 = Not free-running (controlled by PCI_STOP# pin)
1 = Free-running (can override Byte1 PCI Stop Control)

Byte 4: Reserved

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

Byte 5: Reserved

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	X	Reserved
Bit 6	-	X	Reserved
Bit 5	-	X	Reserved
Bit 4	-	X	Reserved
Bit 3	-	X	Reserved
Bit 2	-	X	Reserved
Bit 1	-	X	Reserved
Bit 0	-	X	Reserved

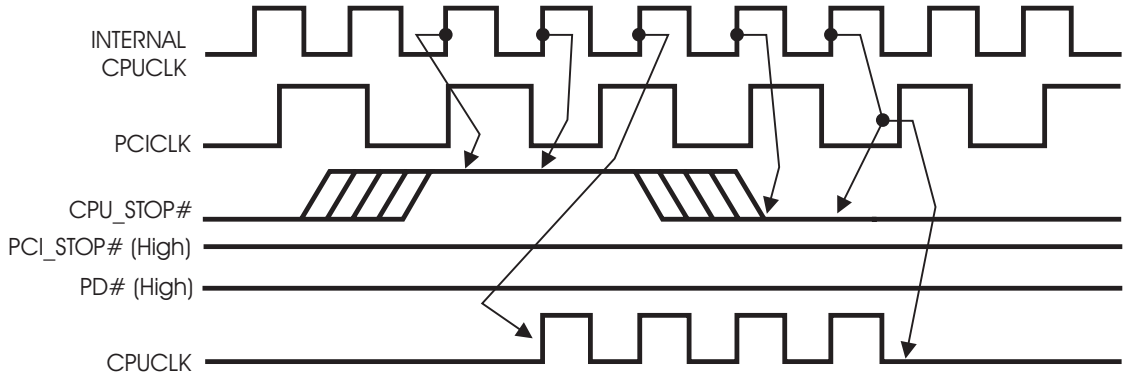
Byte 6: Reserved

BIT	PIN#	PWD	DESCRIPTION
Bit 7	-	0	Reserved
Bit 6	-	0	Reserved
Bit 5	-	0	Reserved
Bit 4	-	0	Reserved
Bit 3	-	0	Reserved
Bit 2	-	1	Reserved
Bit 1	-	1	Reserved
Bit 0	-	0	Reserved

Note: PWD = Power-Up Default

CPU_STOP# Timing Diagram

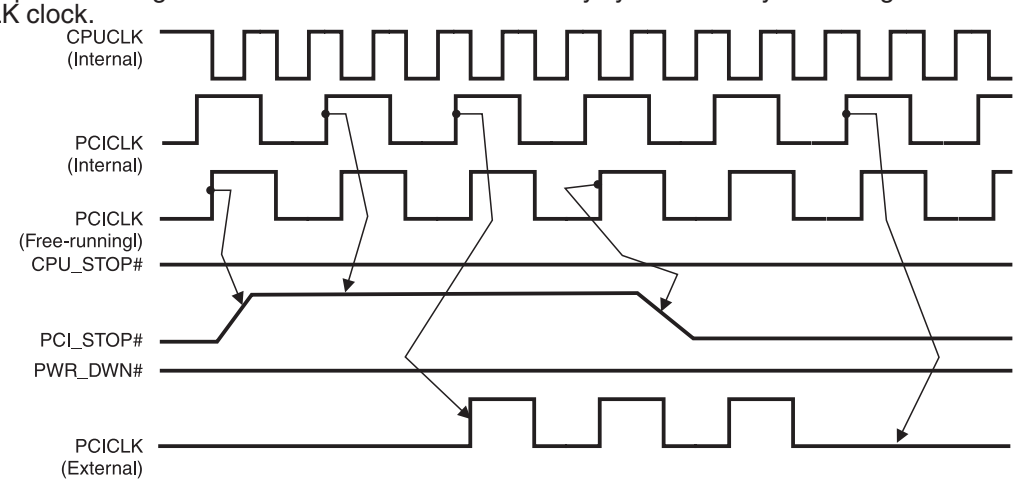
CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9248-192**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:
1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9248-192**.
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9248-192**. It is used to turn off the PCICLK clocks for low power operation. PCI_STOP# is synchronized by the **ICS9248-192** internally. The minimum that the PCICLK clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK clocks. PCICLK clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the **ICS9248-192** device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the **ICS9248-192**.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

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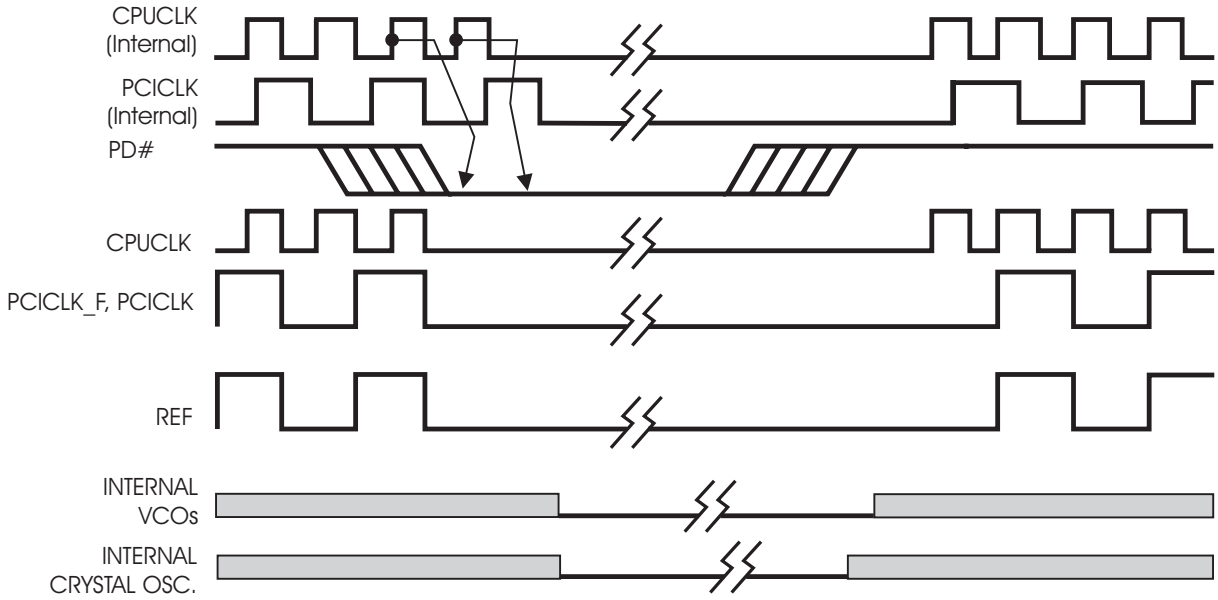
PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internally by the **ICS9248-192** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the crystal oscillator. The power on latency is guaranteed to be less than 3ms. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9248 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9248.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DDL} = 2.5V, V_{DD} = 3.3 V +/-5% (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-5			mA
Input Low Current	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-200			mA
Operating Supply Current	$I_{DD2.5OP66}$	C_L = 0 pF; Select @ 66.6MHz			15	mA
	$I_{DD3.3OP66}$	C_L = 0 pF; Select @ 66.6MHz			80	mA
Power Down Supply Current	$I_{DD3.3PD}$	C_L = 0 pF; With input address to Vdd or GND			600	µA
Input frequency	F_i	V_{DD} = 3.3 V;	11	14.318	16	MHz
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{INX}	X1 & X2 pins	27		45	pF
Transition Time[1]	T_{trans}	To 1st crossing of target Freq.			3	ms
Clk Stabilization[1]	T_{STAB}	From V_{DD} = 3.3 V to 1% target Freq.			3	ms
Skew[1]	$T_{CPU-PCI}$	V_T = 1.5 V; V_{TL} = 1.25 V	1.5		4	ns

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - CPUCLK

T_A = 0 - 70°C; V_{DD} = 3.3 V +/-5%, V_{DDL} = 2.5 V +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH2B}	I_{OH} = -12.0 mA	1.8			V
Output Low Voltage	V_{OL2B}	I_{OL} = 12 mA			0.4	V
Output High Current	I_{OH2B}	V_{OH} = 1.7 V			-27	mA
Output Low Current	I_{OL2B}	V_{OL} = 0.7 V	27			mA
Rise Time	t_{r2B}[1]	V_{OL} = 0.4 V, V_{OH} = 2.0 V	0.4		1.6	ns
Fall Time	t_{f2B}[1]	V_{OH} = 2.0 V, V_{OL} = 0.4 V	0.4		1.6	ns
Duty Cycle	d_{t2B}[1]	V_T = 1.25 V	44		55	%
Skew	t_{sk2B}[1]	V_T = 1.25 V			175	ps
Jitter	$t_{jcyc-cyc2B}$[1]	V_T = 1.25 V			250	ps
	t_{jabs2B}[1]	V_T = 1.25 V	-250		+250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; V_{DD} = 3.3 V , VDDL = 2.5V, +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			4	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			4	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, REF			1000	ps
	t_{jabs5}	V_T = 1.5 V, REF			800	ps
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, 48 MHz			500	ps
	t_{jabs5}	V_T = 1.5 V, 48 MHz			800	ps

Electrical Characteristics - 48MHz

T_A = 0 - 70°C; V_{DD} = 3.3 V , VDDL = 2.5V, +/-5%; C_L = 10 - 20 pF (unless otherwise stated)

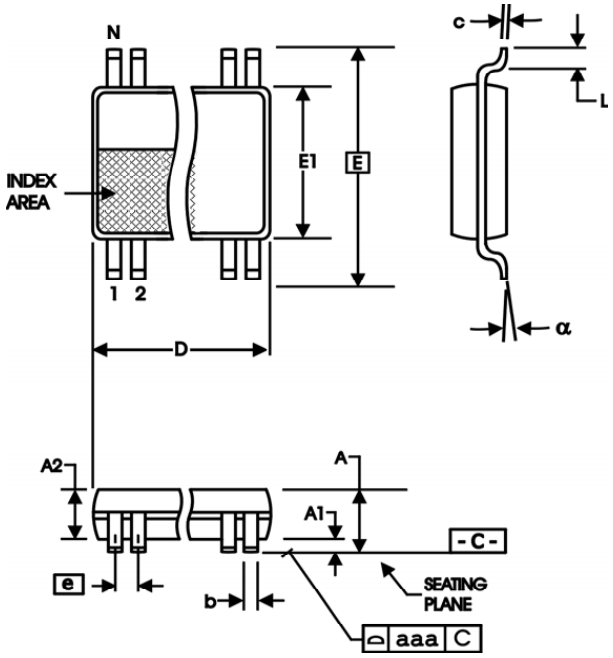
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH5}	I_{OH} = -12 mA	2.6			V
Output Low Voltage	V_{OL5}	I_{OL} = 9 mA			0.4	V
Output High Current	I_{OH5}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL5}	V_{OL} = 0.8 V	16			mA
Rise Time[1]	t_{r5}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			1.2	ns
Fall Time[1]	t_{f5}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			1.2	ns
Duty Cycle[1]	d_{t5}	V_T = 1.5 V	45		55	%
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, REF			1000	ps
	t_{jabs5}	V_T = 1.5 V, REF			800	ps
Jitter[1]	$t_{jcyc-cyc5}$	V_T = 1.5 V, 48 MHz			500	ps
	t_{jabs5}	V_T = 1.5 V, 48 MHz			800	ps

Electrical Characteristics - PCICLK

T_A = 0 - 70°C; V_{DD} = 3.3 V, VDDL = 2.5V +/-5%; C_L = 30 pF

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage	V_{OH1}	I_{OH} = -18 mA	2.1			V
Output Low Voltage	V_{OL1}	I_{OL} = 9.4 mA			0.4	V
Output High Current	I_{OH1}	V_{OH} = 2.0 V			-22	mA
Output Low Current	I_{OL1}	V_{OL} = 0.8 V	16		57	mA
Rise Time[1]	t_{r1}	V_{OL} = 0.4 V, V_{OH} = 2.4 V			2	ns
Fall Time[1]	t_{f1}	V_{OH} = 2.4 V, V_{OL} = 0.4 V			2	ns
Duty Cycle[1]	d_{t1}	V_T = 1.5 V	45		55	%
Skew[1]	t_{sk1}	V_T = 1.5 V			500	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V			500	ps
	t_{jabs1}	V_T = 1.5 V			500	ps

[1]Guaranteed by design, not 100% tested in production.



4.40 mm. Body, 0.65 mm. pitch TSSOP
(173 mil) (0.0256 Inch)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	-	1.20	-	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.19	0.30	.007	.012
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	6.40 BASIC		0.252 BASIC	
E1	4.30	4.50	.169	.177
e	0.65 BASIC		0.0256 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	-	0.10	-	.004

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
28	9.60	9.80	.378	.386

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Ordering Information

ICS9248yG-192LF-T

Example:

ICS XXXX y G - PPP LF - T

- **Designation for tape and reel packaging**
- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  G = TSSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type (consists of 3 to 7 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

0540F—10/27/05

Revision History

Rev.	Issue Date	Description	Page #
F	10/27/2005	Added LF to Ordering Information	12