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EEPROM PROGRAMMABLE 2.5V ZERO DELAY PLL CLOCK DRIVER

IDT5T9820

FEATURES:

- **2.5 V_{DD}**
- **5 pairs of outputs**
- **Low skew: 100ps all outputs at same interface level, 250ps all outputs at different interface levels**
- **Selectable positive or negative edge synchronization**
- **Tolerant of spread spectrum input clock**
- **Synchronous output enable**
- **Selectable inputs**
- **Input frequency: 4.17MHz to 250MHz**
- **Output frequency: 12.5MHz to 250MHz**
- **Internal non-volatile EEPROM**
- **JTAG or I^2C bus serial interface for programming**
- **Hot insertable and over-voltage tolerant inputs**
- **Feedback divide selection with multiply ratios of (1-6, 8, 10, 12)**
- **Selectable HSTL, eHSTL, 1.8V/2.5V LVTTL, or LVEPECL input interface**
- **Selectable HSTL, eHSTL, or 1.8V/2.5V LVTTL output interface for each output bank**
- **Selectable differential or single-ended inputs and ten single-ended outputs**
- **PLL bypass for DC testing**
- **External differential feedback, internal loop filter**
- **Low Jitter: <75ps cycle-to-cycle, all outputs at same interface level: <100ps cycle-to-cycle all outputs at different interface levels**
- **Power-down mode**
- **Lock indicator**
- **Available in VFQFPN package**

DESCRIPTION:

The IDT5T9820 is a 2.5V PLL clock driver intended for high performance computing and data-communications applications. The IDT5T9820 has ten outputs in five banks of two, plus a dedicated differential feedback. The redundant input capability allows for a smooth change over to a secondary clock source when the primary clock source is absent.

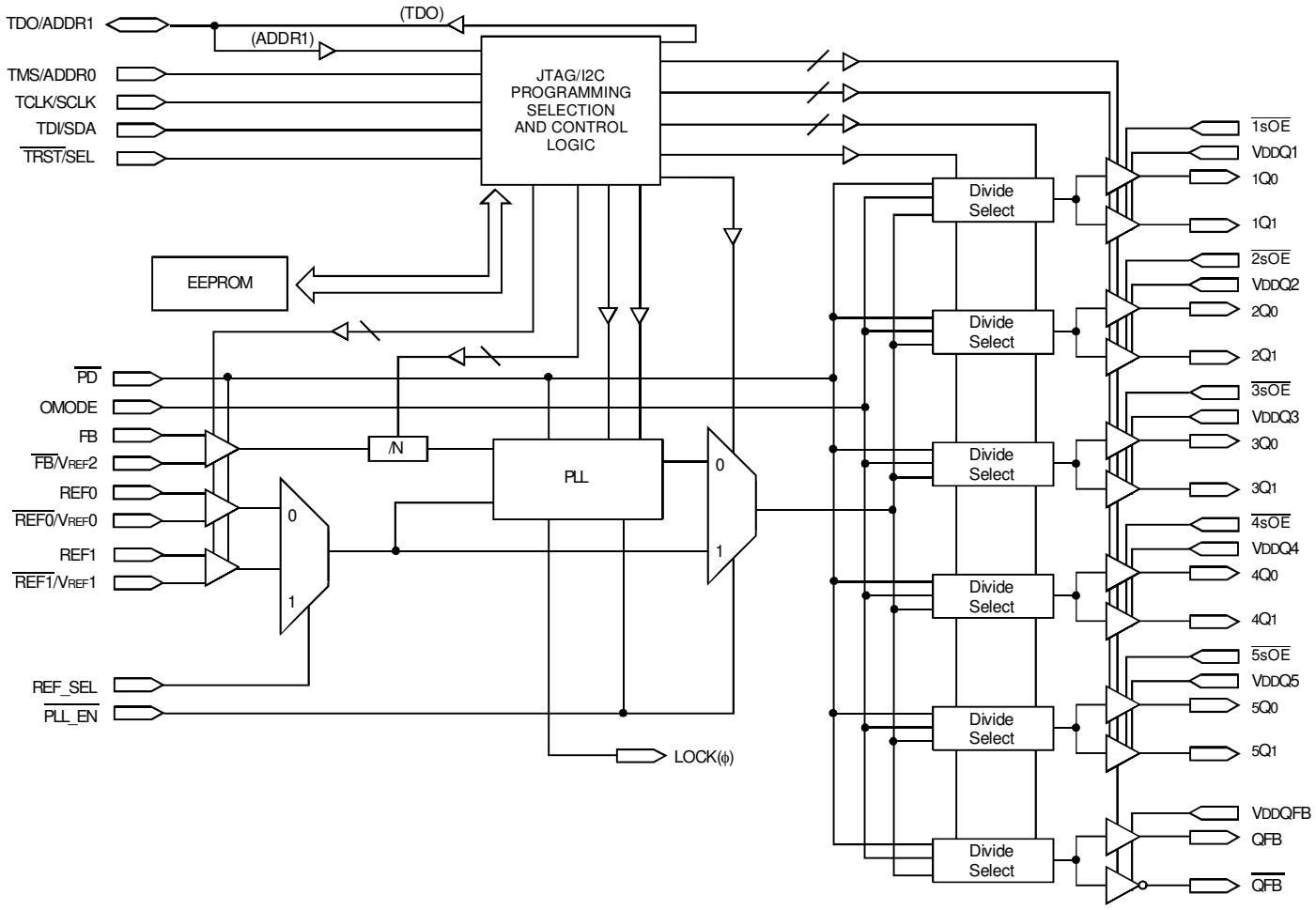
The clock driver can be configured through the use of JTAG/I^2C programming. An internal EEPROM will allow the user to save and restore the configuration of the device.

The feedback bank allows divide-by-functionality from 1 to 12 through the use of JTAG or I^2C programming. This provides the user with frequency multiplication 1 to 12 without using divided outputs for feedback. Each output bank also allows for a divide-by functionality of 2 or 4.

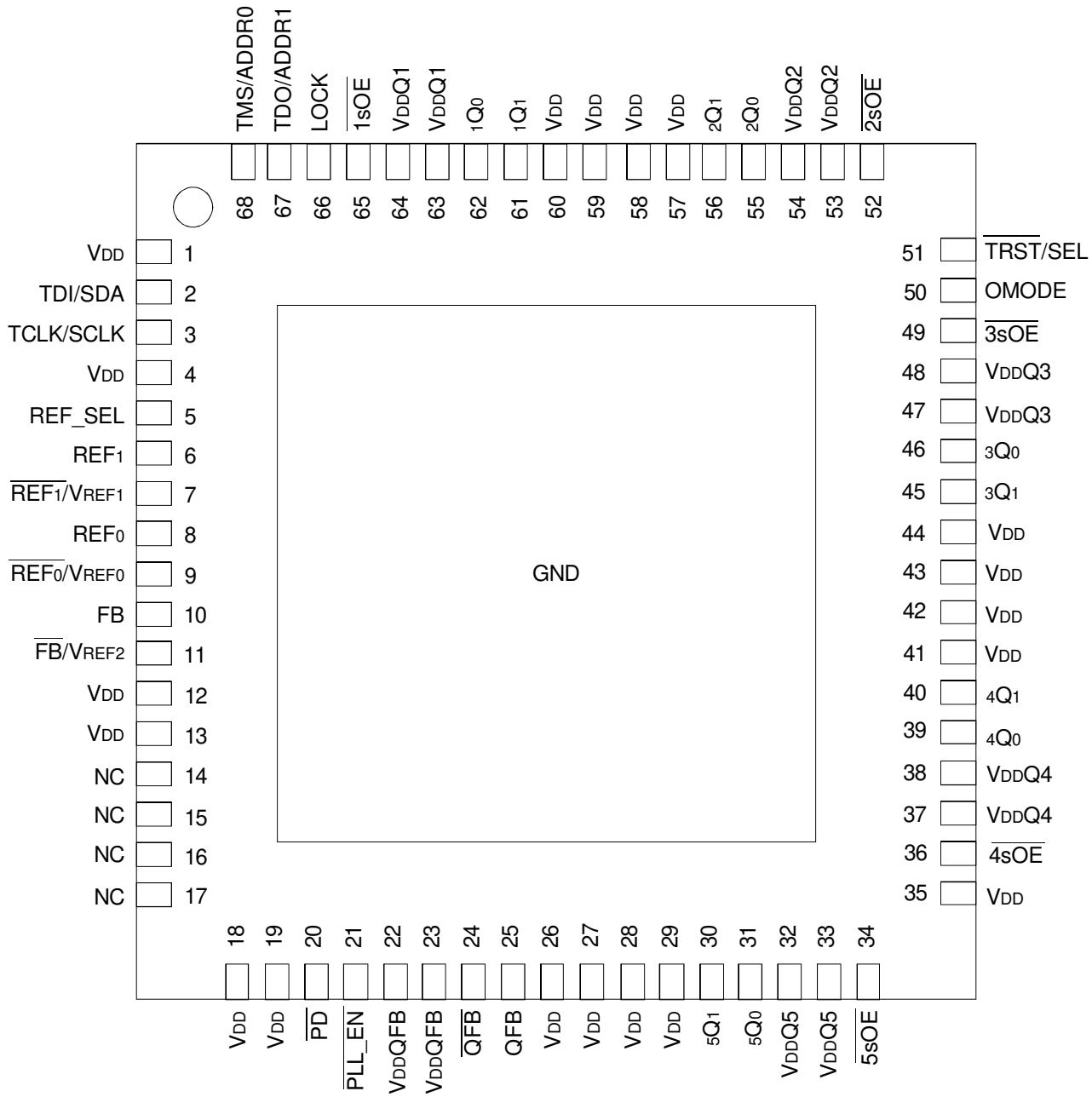
The IDT5T9820 features a user-selectable, single-ended or differential input to ten single-ended outputs. The clock driver also acts as a translator from a differential HSTL, eHSTL, 1.8V/2.5V LVTTL, LVEPECL, or single-ended 1.8V/2.5V LVTTL input to HSTL, eHSTL, or 1.8V/2.5V LVTTL outputs. Each output bank can be individually configured to be either HSTL, eHSTL, 2.5V LVTTL, or 1.8V LVTTL, including the feedback bank. Also, each clock input can be individually configured to accept 2.5V LVTTL, 1.8V LVTTL, or differential signals. The outputs can be synchronously enabled/disabled.

Furthermore, all the outputs can be synchronized with the positive edge of the REF clock input or the negative edge of REF.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



VFQFPN
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V_{DDQN}, V_{DD}	Power Supply Voltage(2)	–0.5 to +3.6	V
V_I	Input Voltage	–0.5 to +3.6	V
V_O	Output Voltage	–0.5 to V_{DDQ} +0.5	V
V_{REF}	Reference Voltage(3)	–0.5 to +3.6	V
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	–65 to +165	°C

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DDQN} and V_{DD} internally operate independently. No power sequencing requirements need to be met.
3. Not to exceed 3.6V.

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{IN} = 0V)

Parameter	Description	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	2.5	3	3.5	pF
C_{OUT}	Output Capacitance	—	6.3	7	pF

NOTE:
1. Capacitance applies to all inputs except JTAG/I^2C signals, SEL, ADDR0, and ADDR1.

RECOMMENDED OPERATING RANGE

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Operating Temperature	–40	+25	+85	°C
V_{DD}(1)	Internal Power Supply Voltage	2.3	2.5	2.7	V
V_{DDQN}(1)	HSTL Output Power Supply Voltage	1.4	1.5	1.6	V
	Extended HSTL and 1.8V LVTTL Output Power Supply Voltage	1.65	1.8	1.95	V
	2.5V LVTTL Output Power Supply Voltage		V_{DD}		V
V_T	Termination Voltage		V_{DDQN} / 2		V

NOTE:
1. All power supplies should operate in tandem. If V_{DD} or V_{DDQN} is at maximum, then V_{DDQN} or V_{DD} (respectively) should be at maximum, and vice-versa.

PIN DESCRIPTION

Symbol	I/O	Type	Description
$REF_{[1:0]}$	I	Adjustable(1)	Clock input. $REF_{[1:0]}$ is the "true" side of the differential clock input. If operating in single-ended mode, $REF_{[1:0]}$ is the clock input.
$\overline{REF}_{[1:0]}$/ $V_{REF[1:0]}$	I	Adjustable(1)	Complementary clock input. $\overline{REF}_{[1:0]}/V_{REF[1:0]}$ is the "complementary" side of $REF_{[1:0]}$ if the input is in differential mode. If operating in single-ended mode, $\overline{REF}_{[1:0]}/V_{REF[1:0]}$ is left floating. For single-ended operation in differential mode, $\overline{REF}_{[1:0]}/V_{REF[1:0]}$ should be set to the desired toggle voltage for $REF_{[1:0]}$: 2.5V LVTTL — V_{REF} = 1250mV (SSTL2 compatible) 1.8V LVTTL, eHSTL — V_{REF} = 900mV HSTL — V_{REF} = 750mV LVEPECL — V_{REF} = 1082mV
FB	I	Adjustable(1)	Clock input. FB is the "true" side of the differential feedback clock input. If operating in single-ended mode, FB is the feedback clock input.
$\overline{FB}/V_{REF2}$	I	Adjustable(1)	Complementary feedback clock input. $\overline{FB}/V_{REF2}$ is the "complementary" side of FB if the input is in differential mode. If operating in single-ended mode, $\overline{FB}/V_{REF2}$ is left floating. For single-ended operation in differential mode, $\overline{FB}/V_{REF2}$ should be set to the desired toggle voltage for FB: 2.5V LVTTL — V_{REF} = 1250mV (SSTL2 compatible) 1.8V LVTTL, eHSTL — V_{REF} = 900mV HSTL — V_{REF} = 750mV LVEPECL — V_{REF} = 1082mV

NOTE:
1. Inputs are capable of translating the following interface standards. User can select between:
   Single-ended 2.5V LVTTL levels
   Single-ended 1.8V LVTTL levels
   or
   Differential 2.5V/1.8V LVTTL levels
   Differential HSTL and eHSTL levels
   Differential LVEPECL levels

PIN DESCRIPTION, CONTINUED

Symbol	I/O	Type	Description
REF_SEL	I	LVTTL(1)	Reference clock select. When LOW, selects REF0 and $\overline{REF}_0$/VREF0. When HIGH, selects REF1 and $\overline{REF}_1$/VREF1.
$\overline{nsOE}$	I	LVTTL(1)	Synchronous output enable/disable. Each outputs's enable/disable state can be controlled either with the $\overline{nsOE}$ pin or through JTAG or I2C programming, corresponding bits 52 - 56. When the $\overline{nsOE}$ is HIGH or the corresponding Bit (52 - 56) is 1, the output will be synchronously disabled. When the $\overline{nsOE}$ is LOW and the corresponding Bit (52 - 56) is 0, the output will be enabled. (See JTAG/I2C Serial Configuration table.)
QFB	O	Adjustable(2)	Feedback clock output
$\overline{QFB}$	O	Adjustable(2)	Complementary feedback clock output
nQ[1:0]	O	Adjustable(2)	Five banks of two outputs
$\overline{PLL\_EN}$	I	LVTTL(1)	PLL enable/disable control. The PLL's enable/disable state can be controlled either with the $\overline{PLL\_EN}$ pin or through JTAG or I2C programming, corresponding Bit 57. When $\overline{PLL\_EN}$ is HIGH or the corresponding Bit 57 is 1, the PLL is disabled and REF[1:0] goes to all outputs. When $\overline{PLL\_EN}$ is LOW and the corresponding Bit 57 is 0, the PLL will be active.
$\overline{PD}$	I	LVTTL(1)	Power down control. When $\overline{PD}$ is LOW, the inputs are disabled and internal switching is stopped. The OMODE pin in conjunction with the corresponding Bit 59 selects whether the outputs are gated LOW/HIGH or tri-stated. When OMODE is HIGH or Bit 59 is 1, Bit 58 determines the level at which the outputs stop. When Bit 58 is 0/1, the nQ[1:0] and QFB are stopped in a HIGH/LOW state, while the $\overline{QFB}$ is stopped in a LOW/HIGH state. When OMODE is LOW and Bit 59 is 0, the outputs are tri-stated. Set $\overline{PD}$ HIGH for normal operation. (See JTAG/I2C Serial Configuration table.)
LOCK	O	LVTTL	PLL lock indication signal. HIGH indicates lock. LOW indicates that the PLL is not locked and outputs may not be synchronized to the inputs. The output will be 2.5V LVTTL. (For more information on application specific use of the LOCK pin, please see AN237.)
OMODE	I	LVTTL(1)	Output disable control. Used in conjunction with $\overline{nsOE}$ and $\overline{PD}$. The outputs' disable state can be controlled either with the OMODE pin or through JTAG or I2C programming, corresponding Bit 59. When OMODE is HIGH or the corresponding Bit 59 is 1, the outputs' disable state will be gated and Bit 58 will determine the level at which the outputs stop. When Bit 58 is 0/1, the nQ[1:0] and QFB are stopped in a HIGH/LOW state, while the $\overline{QFB}$ is stopped in a LOW/HIGH state. When OMODE is LOW and its corresponding bit 59 is 0, the outputs disable state will be the tri-state. (See JTAG/I2C Serial Configuration table.)
$\overline{TRST}$/SEL	I/I	LVTTL/ LVTTL(4,5)	$\overline{TRST}$ - Active LOW input to asynchronously reset the JTAG boundary-scan circuit. SEL - Select programming interface control for the dual-function pins. When HIGH, the dual-function pins are set for JTAG programming. When LOW, the dual-function pins are set for I2C programming and the JTAG interface is asynchronously placed in the Test Logic Reset state.
TDO/ADDR1	O/I	LVTTL/ 3-Level(3,4,5)	TDO - Serial data output pin for instructions as well as test and programming data. Data is shifted in on the falling edge of TCLK. The pin is tri-stated if data is not being shifted out of the device. ADDR1 - Used to define a unique I2C address for this device. Only for I2C programming. (See JTAG/I2C Serial Interface Description.)
TMS/ADDR0	I/I	LVTTL/ 3-Level(3,4,5)	TMS - Input pin that provides the control signal to determine the transitions of the JTAG TAP controller state machine. Transitions within the state machine occur at the rising edge of TCLK. Therefore, TMS must be set up before the rising edge of TCLK. TMS is evaluated on the rising edge TCLK. ADDR0 - Used to define a unique I2C address for this device. Only for I2C programming. (See JTAG/I2C Serial Interface Description.)
TCLK/SCLK	I/I	LVTTL/ LVTTL(4,5)	TCLK - The clock input to the JTAG BST circuitry SCLK - Serial clock for I2C programming
TDI/SDA	I/I	LVTTL/ LVTTL(4,5)	TDI - Serial input pin for instructions as well as test and programming data. Data is shifted in on the rising edge of TCLK. SDA - Serial data for I2C programming. (See JTAG/I2C Serial Description table.)
VDDQN		PWR	Power supply for each pair of outputs. When using 2.5V LVTTL, 1.8V LVTTL, HSTL, or eHSTL outputs, VDDQN should be set to its corresponding outputs (see Front Block Diagram). When using 2.5V LVTTL outputs, VDDQN should be connected to VDD.
VDD		PWR	Power supply for phase locked loop, lock output, inputs, and other internal circuitry
GND		PWR	Ground

NOTES:
1. Pins listed as LVTTL inputs can be configured to accept 1.8V or 2.5V signals through the use of the I2C/JTAG programming, bit 61. (See JTAG/I2C Serial Description.)
2. Outputs are user selectable to drive 2.5V, 1.8V LVTTL, eHSTL, or HSTL interface levels when used with the appropriate VDDQN voltage.
3. 3-level inputs are static inputs and must be tied to VDD or GND or left floating. These inputs are not hot-insertable or over voltage tolerant.
4. The JTAG (TDO, TMS, TCLK, and TDI) and I2C (ADDR1, ADDR0, SCLK, and SDA) signals share the same pins (dual-function pins) for which the $\overline{TRST}$/SEL pin will select between the two programming interfaces.
5. JTAG and I2C pins accept 2.5V signals. The JTAG input pins (TMS, TCLK, TDI, $\overline{TRST}$) will also accept 1.8V signals.

JTAG/ I²C SERIAL DESCRIPTION

Bit	Description
95:62	Reserved Bits. Set bits 95:62 to '0'.
61	Input Interface Selection for control pins (REF_SEL, $\overline{PD}$, $\overline{PLL\_EN}$, OMODE, $\overline{nsOE}$). When bit 61 is '1', the control pins are 2.5V LVTTL. When bit 61 is '0', the control pins are 1.8V LVTTL.
60	VCO Frequency Range. When '0', range is 50MHz-125MHz. When '1', range is 100MHz-250MHz.
59	Output's Disable State. See corresponding external pin OMODE in Pin Description table.
58	Positive/Negative Edge Control. When '0'/'1', the outputs are synchronized with the negative/positive edge of the reference clock.
57	PLL Enable/Disable. See corresponding external pin $\overline{PLL\_EN}$ in Pin Description table.(1)
56	Output Enable/Disable for $1Q_{[1:0]}$ outputs. See corresponding external pin $\overline{1sOE}$ in Pin Description table.
55	Output Enable/Disable for $2Q_{[1:0]}$ outputs. See corresponding external pin $\overline{2sOE}$ in Pin Description table.
54	Output Enable/Disable for $3Q_{[1:0]}$ outputs. See corresponding external pin $\overline{3sOE}$ in Pin Description table.
53	Output Enable/Disable for $4Q_{[1:0]}$ outputs. See corresponding external pin $\overline{4sOE}$ in Pin Description table.
52	Output Enable/Disable for $5Q_{[1:0]}$ outputs. See corresponding external pin $\overline{5sOE}$ in Pin Description table.
51	FB Divide-by-N selection
50	FB Divide-by-N selection
49	FB Divide-by-N selection
48	FB Divide-by-N selection
47	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 1
46	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 1
45	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 2
44	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 2
43	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 3
42	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 3
41	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 4
40	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 4
39	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 5
38	Output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on bank 5
37	FB output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on FB bank
36	FB output drive strength selection for 2.5V LVTTL, 1.8V LVTTL, or HSTL/eHSTL on FB bank
35	REF0 Input interface selection for 2.5V LVTTL, 1.8V LVTTL, or Differential
34	REF0 Input interface selection for 2.5V LVTTL, 1.8V LVTTL, or Differential
33	REF1 input interface selection for 2.5V LVTTL, 1.8V LVTTL, or Differential
32	REF1 input interface selection for 2.5V LVTTL, 1.8V LVTTL, or Differential
31	FB input interface selection for 2.5V LVTTL, 1.8V LVTTL, or Differential
30	FB input interface selection for 2.5V LVTTL, 1.8V LVTTL, or Differential
29	Divide selection for bank 1
28	Divide selection for bank 1
27	Divide selection for bank 1
26	Divide selection for bank 1
25	Divide selection for bank 1
24	Divide selection for bank 2
23	Divide selection for bank 2
22	Divide selection for bank 2
21	Divide selection for bank 2

NOTE:
1. Only for EEPROM operation; bit 57 must be set to 0 to enable the PLL for proper EEPROM operation. The EEPROM access times are based on the VCO frequency of the PLL (refer to the EEPROM Operation section).

JTAG/ I²C SERIAL DESCRIPTION, CONT.

Bit	Description
20	Divide selection for bank 2
19	Divide selection for bank 3
18	Divide selection for bank 3
17	Divide selection for bank 3
16	Divide selection for bank 3
15	Divide selection for bank 3
14	Divide selection for bank 4
13	Divide selection for bank 4
12	Divide selection for bank 4
11	Divide selection for bank 4
10	Divide selection for bank 4
9	Divide selection for bank 5
8	Divide selection for bank 5
7	Divide selection for bank 5
6	Divide selection for bank 5
5	Divide selection for bank 5
4	Divide selection for FB bank
3	Divide selection for FB bank
2	Divide selection for FB bank
1	Divide selection for FB bank
0	Divide selection for FB bank

JTAG/ I²C SERIAL CONFIGURATIONS: OUTPUT ENABLE/DISABLE

Bit 59 (OMODE)	Bit 56-52 ($\overline{nsOE}$)	Output
X (X)	0 and (L)	Normal Operation
0 and (L)	1 or (H)	Tri-Sate
1 or (H)	1 or (H)	Gated(1)

NOTE:
1. OMODE and its corresponding Bit 59 selects whether the outputs are gated LOW/ HIGH or tri-stated. When OMODE is HIGH or the corresponding Bit 59 is 1, the outputs' disable state will be gated. Bit 58 determines the level at which the outputs stop. When Bit 58 is 0/ 1, the $nQ_{[1:0]}$ and QFB are stopped in a HIGH/LOW state, while the $\overline{QFB}$ is stopped in a LOW/HIGH state. When OMODE is LOW and its corresponding Bit 59 is 0, the outputs' disable state will be the tri-state.

JTAG/ I²C SERIAL CONFIGURATIONS: POWERDOWN

$\overline{PD}$	Bit 59 (OMODE)	Output
H	X (X)	Normal Operation
L	0 and (L)	Tri-Sate
L	1 or (H)	Gated(1)

NOTE:
1. OMODE and its corresponding Bit 59 selects whether the outputs are gated LOW/ HIGH or tri-stated. When OMODE is HIGH or the corresponding Bit 59 is 1, the outputs' disable state will be gated. Bit 58 determines the level at which the outputs stop. When Bit 58 is 0/ 1, the $nQ_{[1:0]}$ and QFB are stopped in a HIGH/LOW state, while the $\overline{QFB}$ is stopped in a LOW/HIGH state. When OMODE is LOW and its corresponding Bit 59 is 0, the outputs' disable state will be the tri-state.

JTAG/ I²C SERIAL CONFIGURATIONS: CLOCK INPUT INTERFACE SELECTION(1)

Bit 31, 33, 35	Bit 30, 32, 34	Interface
0	0	Differential(2)
0	1	2.5V LVTTL
1	1	1.8V LVTTL

NOTES:
1. All other states that are undefined in the table will be reserved.
2. Differential input interface for HSTL/eHSTL, LVEPECL (2.5V), and 2.5V/1.8V LVTTL.

JTAG/ I²C SERIAL CONFIGURATIONS: OUTPUT DRIVE STRENGTH SELECTION(1)

Bit 37, 39, 41, 43, 45, 47	Bit 36, 38, 40, 42, 44, 46	Interface
0	0	2.5V LVTTL
0	1	1.8V LVTTL
1	0	HSTL/eHSTL

NOTE:
1. All other states that are undefined in the table will be reserved.

JTAG/ I²C SERIAL CONFIGURATIONS: SKEW OR FREQUENCY SELECT(1)

Bit 4, 9, 14, 19, 24, 29	Bit 3, 8, 13, 18, 23, 28	Bit 2, 7, 12, 17, 22, 27	Bit 1, 6, 11, 16, 21, 26	Bit 0, 5, 10, 15, 20, 25	Output Skew
0	0	0	0	0	Zero Skew
1	0	0	0	0	Inverted
1	0	0	0	1	Divide-by-2
1	0	0	1	0	Divide-by-4

NOTE:
1. All other states that are undefined in the table will result in zero skew.

JTAG/ I²C SERIAL CONFIGURATIONS: FB DIVIDE-BY-N(1)

Bit 51	Bit 50	Bit 49	Bit 48	Divide-by-N	Permitted Output Divide-by-N connected to FB and $\overline{FB}$/VREF2 (2)
0	0	0	0	1	1, 2, 4
0	0	0	1	2	1, 2
0	0	1	0	3	1
0	0	1	1	4	1, 2
0	1	0	0	5	1, 2
0	1	0	1	6	1, 2
0	1	1	0	8	1
0	1	1	1	10	1
1	0	0	0	12	1

NOTES:
1. All other states that are undefined in the table will be reserved.
2. Permissible output division ratios connected to FB and $\overline{FB}$/VREF2. The frequencies of the REF[1:0] and $\overline{REF}$ [1:0]/VREF[1:0] inputs will be Fvco/N when the parts are configured for frequency multiplication by using an undivided output for FB and $\overline{FB}$/VREF2 and setting N (N = 1-6, 8, 10, 12).

EXTERNAL DIFFERENTIAL FEEDBACK

By providing a dedicated external differential feedback, the IDT5T9820 gives users flexibility with regard to divide selection. The FB and $\overline{FB}$/ V_{REF2} signals are compared with the input REF[1:0] and $\overline{REF}$[1:0]/$V_{REF[1:0]}$ signals at the phase detector in order to drive the VCO. Phase differences cause the VCO of the PLL to adjust upwards or downwards accordingly.

An internal loop filter moderates the response of the VCO to the phase detector. The loop filter transfer function has been chosen to provide minimal jitter (or frequency variation) while still providing accurate responses to input frequency changes.

MASTER RESET FUNCTIONALITY

The IDT5T9820 performs a reset of the internal output divide circuitry when all five output banks are disabled by toggling the $\overline{nSOE}$ pins HIGH. When one or more banks of outputs are enabled by toggling the $\overline{nSOE}$ LOW (if the corresponding $\overline{nSOE}$ programming bits are also set LOW), the divide circuitry starts again from a known state. In the case that the FB output is selected for divide-by-2 or divide-by-4, the FB output will stop toggling while all five $\overline{nSOE}$ pins and bits are LOW, and loss of lock will occur.

INPUT/OUTPUT SELECTION(1)

Input	Output(2)
2.5V LVTTL SE	2.5V LVTTL,
1.8V LVTTL SE	1.8V LVTTL,
2.5V LVTTL DSE	HSTL,
1.8V LVTTL DSE	eHSTL
LVEPECL DSE	
eHSTL DSE	
HSTL DSE	
2.5V LVTTL DIF	
1.8V LVTTL DIF	
LVEPECL DIF	
eHSTL DIF	
HSTL DIF	

NOTES:
1. The INPUT/OUTPUT SELECTION Table describes the total possible combinations of input and output interfaces. Single-Ended (SE) inputs in a single-ended mode require the $\overline{REF}_{[1:0]}$ /$V_{REF[1:0]}$ and $\overline{FB}$/V_{REF2} pins to be left floating. Differential Single-Ended (DSE) is for single-ended operation in differential mode, requiring $V_{REF[1:0]}$ and V_{REF2}. Differential (DIF) inputs are used only in differential mode.
2. For each output bank.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions		Min.	Max	Unit
V_{IHH}	Input HIGH Voltage Level[1]	3-Level Inputs Only		V_{DD} – 0.4	—	V
V_{IMM}	Input MID Voltage Level[1]	3-Level Inputs Only		$V_{DD}/2$ – 0.2	$V_{DD}/2$ + 0.2	V
V_{ILL}	Input LOW Voltage Level[1]	3-Level Inputs Only		—	0.4	V
I_3	3-Level Input DC Current (ADDR0, ADDR1)	V_{IN} = V_{DD}	HIGH Level	—	200	µA
		V_{IN} = $V_{DD}/2$	MID Level	–50	+50	
		V_{IN} = GND	LOW Level	–200	—	
I_{PU}	Input Pull-Up Current	V_{DD} = Max., V_{IN} = GND		–100	—	µA

NOTE:

1. These inputs are normally wired to V_{DD}, GND, or left floating. Internal termination resistors bias unconnected inputs to $V_{DD}/2$. If these inputs are switched dynamically after powerup, the function and timing of the outputs may be glitched, and the PLL may require additional t_{LOCK} time before all datasheet limits are achieved.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR HSTL[1]

Symbol	Parameter	Test Conditions		Min.	Typ.[7]	Max	Unit
Input Characteristics							
I_{IH}	Input HIGH Current	V_{DD} = 2.7V	V_I = V_{DDQN}/GND	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V	V_I = GND/V_{DDQN}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA		—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage			- 0.3		+3.6	V
V_{DIF}	DC Differential Voltage[2,8]			0.2		—	V
V_{CM}	DC Common Mode Input Voltage[3,8]			680	750	900	mV
V_{IH}	DC Input HIGH[4,5,8]			V_{REF} + 100		—	mV
V_{IL}	DC Input LOW[4,6,8]			—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage[4,8]			—	750	—	mV
Output Characteristics							
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA		V_{DDQN} - 0.4		—	V
		I_{OH} = -100µA		V_{DDQN} - 0.1		—	
V_{OL}	Output LOW Voltage	I_{OL} = 8mA		—		0.4	V
		I_{OL} = 100µA		—		0.1	
V_{OX}	FB/$\overline{FB}$ Output Crossing Point			$V_{DDQN}/2$ - 150	$V_{DDQN}/2$	$V_{DDQN}/2$ + 150	mV

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation, in differential mode, $\overline{REF}_{[1:0]}$/$V_{REF[1:0]}$ is tied to the DC voltage $V_{REF[1:0]}$.
5. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
6. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
7. Typical values are at V_{DD} = 2.5V, V_{DDQN} = 1.5V, +25°C ambient.
8. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. (See Input/Output Selection table.)

POWER SUPPLY CHARACTERISTICS FOR HSTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	112	150	mA
I_{DDQQ}	Quiescent V_{DDQN} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	3	75	µA
I_{DDPD}	Power Down Current	V_{DD} = Max., $\overline{PD}$ = LOW, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH	0.7	3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	22	30	µA/MHz
I_{DDDQ}	Dynamic V_{DDQN} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	18	30	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current(4,5)	V_{DDQN} = 1.5V, F_{VCO} = 100MHz, C_L = 15pF	280	400	mA
		V_{DDQN} = 1.5V, F_{VCO} = 250MHz, C_L = 15pF	320	450	
I_{TOTQ}	Total Power V_{DDQN} Supply Current(4,5)	V_{DDQN} = 1.5V, F_{VCO} = 100MHz, C_L = 15pF	130	200	mA
		V_{DDQN} = 1.5V, F_{VCO} = 250MHz, C_L = 15pF	225	330	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
4. Bit 60 = 1.
5. All outputs are at the same interface level.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR HSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	1	V
V_X	Differential Input Signal Crossing Point(2)	750	mV
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	1	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 750mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR eHSTL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(7)	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current	V_{DD} = 2.7V V_I = V_{DDQN}/GND	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V V_I = GND/V_{DDQN}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		+3.6	V
V_{DIF}	DC Differential Voltage(2,8)		0.2		—	V
V_{CM}	DC Common Mode Input Voltage(3,8)		800	900	1000	mV
V_{IH}	DC Input HIGH(4,5,8)		V_{REF} + 100		—	mV
V_{IL}	DC Input LOW(4,6,8)		—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage(4,8)		—	900	—	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = -8mA	V_{DDQN} - 0.4		—	V
		I_{OH} = -100µA	V_{DDQN} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 8mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V
V_{OX}	FB/$\overline{FB}$ Output Crossing Point		V_{DDQN}/2 - 150	V_{DDQN}/2	V_{DDQN}/2 + 150	mV

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation, in a differential mode, $\overline{REF}_{[1:0]}$/$V_{REF[1:0]}$ is tied to the DC voltage $V_{REF[1:0]}$.
5. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
6. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
7. Typical values are at V_{DD} = 2.5V, V_{DDQN} = 1.8V, +25°C ambient.
8. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. (See Input/Output Selection table.)

POWER SUPPLY CHARACTERISTICS FOR eHSTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	112	150	mA
I_{DDQQ}	Quiescent V_{DDQN} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	3	75	µA
I_{DDPD}	Power Down Current	V_{DD} = Max., $\overline{PD}$ = LOW, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH	0.7	3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	22	30	µA/MHz
I_{DDDQ}	Dynamic V_{DDQN} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	22	30	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current(4,5)	V_{DDQN} = 1.8V, F_{VCO} = 100MHz, C_L = 15pF	280	400	mA
		V_{DDQN} = 1.8V, F_{VCO} = 250MHz, C_L = 15pF	320	450	
I_{TOTQ}	Total Power V_{DDQN} Supply Current(4,5)	V_{DDQN} = 1.8V, F_{VCO} = 100MHz, C_L = 15pF	160	250	mA
		V_{DDQN} = 1.8V, F_{VCO} = 250MHz, C_L = 15pF	280	400	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
4. Bit 60 = 1.
5. All outputs are at the same interface level.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR eHSTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	1	V
V_X	Differential Input Signal Crossing Point(2)	900	mV
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	1	V/ns

NOTES:

1. The 1V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR LVEPECL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(2)	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current	V_{DD} = 2.7V V_I = V_{DDQN}/GND	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V V_I = GND/V_{DDQN}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3	—	3.6	V
V_{CM}	DC Common Mode Input Voltage(3,5)		915	1082	1248	mV
V_{REF}	Single-Ended Reference Voltage(4,5)		—	1082	—	mV
V_{IH}	DC Input HIGH		1275	—	1620	mV
V_{IL}	DC Input LOW		555	—	875	mV

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. Typical values are at V_{DD} = 2.5V, +25°C ambient.
3. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
4. For single-ended operation while in differential mode, $\overline{REF}_{[1:0]}$/$V_{REF[1:0]}$ is tied to the DC voltage $V_{REF[1:0]}$.
5. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. (See Input/Output Selection table.)

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR LVEPECL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	732	mV
V_X	Differential Input Signal Crossing Point(2)	1082	mV
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	1	V/ns

NOTES:

1. The 732mV peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A 1082mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR 2.5V LVTTL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(8)	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current	V_{DD} = 2.7V V_I = V_{DDQN}/GND	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V V_I = GND/V_{DDQN}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		+3.6	V
Single-Ended Inputs(2)						
V_{IH}	DC Input HIGH		1.7		—	V
V_{IL}	DC Input LOW		—		0.7	V
Differential Inputs						
V_{DIF}	DC Differential Voltage(3,9)		0.2		—	V
V_{CM}	DC Common Mode Input Voltage(4,9)		1150	1250	1350	mV
V_{IH}	DC Input HIGH(5,6,9)		V_{REF} + 100		—	mV
V_{IL}	DC Input LOW(5,7,9)		—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage(5,9)		—	1250	—	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = -12mA	V_{DDQN} - 0.4		—	V
		I_{OH} = -100µA	V_{DDQN} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 12mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. For 2.5V LVTTL single-ended operation, Bits 35/34, 33/32, 31/30 = 0/1 or 1/0, and $\overline{REF}_{[1:0]}/V_{REF[1:0]}$ is left floating. If Bits 47 - 36 = 0, $\overline{FB}/V_{REF2}$ should be left floating.
3. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
4. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
5. For single-ended operation, in differential mode, $\overline{REF}_{[1:0]}/V_{REF[1:0]}$ is tied to the DC voltage $V_{REF[1:0]}$.
6. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
7. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
8. Typical values are at V_{DD} = 2.5V, V_{DDQN} = V_{DD}, +25°C ambient.
9. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. (See Input/Output Selection table.)

POWER SUPPLY CHARACTERISTICS FOR 2.5V LVTTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	112	150	mA
I_{DDQQ}	Quiescent V_{DDQN} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	20	75	µA
I_{DDPD}	Power Down Current	V_{DD} = Max., $\overline{PD}$ = LOW, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH	0.7	3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	19	30	µA/MHz
I_{DDDQ}	Dynamic V_{DDQN} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	32	40	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current(4,5)	V_{DDQN} = 2.5V., F_{VCO} = 100MHz, C_L = 15pF	275	400	mA
		V_{DDQN} = 2.5V., F_{VCO} = 250MHz, C_L = 15pF	315	450	
I_{TOTQ}	Total Power V_{DDQN} Supply Current(4,5)	V_{DDQN} = 2.5V., F_{VCO} = 100MHz, C_L = 15pF	215	320	mA
		V_{DDQN} = 2.5V., F_{VCO} = 250MHz, C_L = 15pF	355	530	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
4. Bit 60 = 1.
5. All outputs are at the same interface level.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR 2.5V LVTTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	V_{DD}	V
V_X	Differential Input Signal Crossing Point(2)	$V_{DD}/2$	V
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	2.5	V/ns

NOTES:

1. A nominal 2.5V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 1.25V crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 2.5V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

SINGLE-ENDED INPUT AC TEST CONDITIONS FOR 2.5V LVTTL

Symbol	Parameter	Value	Units
V_{IH}	Input HIGH Voltage	V_{DD}	V
V_{IL}	Input LOW Voltage	0	V
V_{THI}	Input Timing Measurement Reference Level(1)	$V_{DD}/2$	V
t_R, t_F	Input Signal Edge Rate(2)	2	V/ns

NOTES:

1. A nominal 1.25V timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
2. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE FOR 1.8V LVTTL(1)

Symbol	Parameter	Test Conditions	Min.	Typ.(8)	Max	Unit
Input Characteristics						
I_{IH}	Input HIGH Current	V_{DD} = 2.7V V_I = V_{DDQN}/GND	—	—	±5	µA
I_{IL}	Input LOW Current	V_{DD} = 2.7V V_I = GND/V_{DDQN}	—	—	±5	
V_{IK}	Clamp Diode Voltage	V_{DD} = 2.3V, I_{IN} = -18mA	—	- 0.7	- 1.2	V
V_{IN}	DC Input Voltage		- 0.3		V_{DDQN} + 0.3	V
Single-Ended Inputs(2)						
V_{IH}	DC Input HIGH		1.073(10)		—	V
V_{IL}	DC Input LOW		—		0.683(11)	V
Differential Inputs						
V_{DIF}	DC Differential Voltage(3,9)		0.2		—	V
V_{CM}	DC Common Mode Input Voltage(4,9)		825	900	975	mV
V_{IH}	DC Input HIGH(5,6,9)		V_{REF} + 100		—	mV
V_{IL}	DC Input LOW(5,7,9)		—		V_{REF} - 100	mV
V_{REF}	Single-Ended Reference Voltage(5,9)		—	900	—	mV
Output Characteristics						
V_{OH}	Output HIGH Voltage	I_{OH} = -6mA	V_{DDQN} - 0.4		—	V
		I_{OH} = -100µA	V_{DDQN} - 0.1		—	V
V_{OL}	Output LOW Voltage	I_{OL} = 6mA	—		0.4	V
		I_{OL} = 100µA	—		0.1	V

NOTES:

1. See RECOMMENDED OPERATING RANGE table.
2. For 1.8V LVTTL single-ended operation, Bits 35 - 30 = 0 and $\overline{REF}_{[1:0]}$/$V_{REF[1:0]}$ is left floating. If Bits 47/46, 45/44, 43/42, 41/40, 39/38, 37/36 = 0/1, $\overline{FB}$/V_{REF2} should be left floating.
3. V_{DIF} specifies the minimum input differential voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. Differential mode only. The DC differential voltage must be maintained to guarantee retaining the existing HIGH or LOW input. The AC differential voltage must be achieved to guarantee switching to a new state.
4. V_{CM} specifies the maximum allowable range of (V_{TR} + V_{CP}) /2. Differential mode only.
5. For single-ended operation in differential mode, $\overline{REF}_{[1:0]}$/$V_{REF[1:0]}$ is tied to the DC voltage $V_{REF[1:0]}$. The input is guaranteed to toggle within ±200mV of $V_{REF[1:0]}$ when $V_{REF[1:0]}$ is constrained within +600mV and V_{DDI}-600mV, where V_{DDI} is the nominal 1.8V power supply of the device driving the $REF_{[1:0]}$ input. To guarantee switching in voltage range specified in the JEDEC 1.8V LVTTL interface specification, $V_{REF[1:0]}$ must be maintained at 900mV with appropriate tolerances.
6. Voltage required to maintain a logic HIGH, single-ended operation in differential mode.
7. Voltage required to maintain a logic LOW, single-ended operation in differential mode.
8. Typical values are at V_{DD} = 2.5V, V_{DDQN} = 1.8V, +25°C ambient.
9. The reference clock input is capable of HSTL, eHSTL, LVEPECL, 1.8V or 2.5V LVTTL operation independent of the device output. (See Input/Output Selection table.)
10. This value is the worst case minimum V_{IH} over the specification range of the 1.8V power supply. The 1.8V LVTTL specification is V_{IH} = 0.65 * V_{DD} where V_{DD} is 1.8V ± 0.15V. However, the LVTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value (V_{IH} = 0.65 * [1.8 - 0.15V]) rather than reference against a nominal 1.8V supply.
11. This value is the worst case maximum V_{IL} over the specification range of the 1.8V power supply. The 1.8V LVTTL specification is V_{IL} = 0.35 * V_{DD} where V_{DD} is 1.8V ± 0.15V. However, the LVTTL translator is supplied by a 2.5V nominal supply on this part. To ensure compliance with the specification, the translator was designed to accept the calculated worst case value (V_{IL} = 0.35 * [1.8 + 0.15V]) rather than reference against a nominal 1.8V supply.

POWER SUPPLY CHARACTERISTICS FOR 1.8V LVTTL OUTPUTS(1)

Symbol	Parameter	Test Conditions(2)	Typ.	Max	Unit
I_{DDQ}	Quiescent V_{DD} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	112	150	mA
I_{DDQQ}	Quiescent V_{DDQN} Power Supply Current(3)	V_{DDQN} = Max., REF = LOW, $\overline{PD}$ = HIGH, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH, Outputs enabled, All outputs unloaded	3	75	µA
I_{DDPD}	Power Down Current	V_{DD} = Max., $\overline{PD}$ = LOW, $\overline{nSOE}$ = LOW, $\overline{PLL\_EN}$ = HIGH	0.7	3	mA
I_{DDD}	Dynamic V_{DD} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	18	30	µA/MHz
I_{DDDQ}	Dynamic V_{DDQN} Power Supply Current per Output	V_{DD} = Max., V_{DDQN} = Max., C_L = 0pF	19	30	µA/MHz
I_{TOT}	Total Power V_{DD} Supply Current(4,5)	V_{DDQN} = 1.8V., F_{VCO} = 100MHz, C_L = 15pF	275	400	mA
		V_{DDQN} = 1.8V., F_{VCO} = 250MHz, C_L = 15pF	310	450	
I_{TOTQ}	Total Power V_{DDQN} Supply Current(4,5)	V_{DDQN} = 1.8V., F_{VCO} = 100MHz, C_L = 15pF	135	200	mA
		V_{DDQN} = 1.8V., F_{VCO} = 250MHz, C_L = 15pF	200	300	

NOTES:

1. These power consumption characteristics are for all the valid input interfaces and cover the worst case input and output interface combinations.
2. The termination resistors are excluded from these measurements.
3. If the differential input interface is used, the true input is held LOW and the complementary input is held HIGH.
4. Bit 60 = 1.
5. All outputs are at the same interface level.

DIFFERENTIAL INPUT AC TEST CONDITIONS FOR 1.8V LVTTL

Symbol	Parameter	Value	Units
V_{DIF}	Input Signal Swing(1)	V_{DDI}	V
V_X	Differential Input Signal Crossing Point(2)	$V_{DDI}/2$	mV
V_{THI}	Input Timing Measurement Reference Level(3)	Crossing Point	V
t_R, t_F	Input Signal Edge Rate(4)	1.8	V/ns

NOTES:

1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input. A nominal 1.8V peak-to-peak input pulse level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_{DIF} (AC) specification under actual use conditions.
2. A nominal 900mV crossing point level is specified to allow consistent, repeatable results in an automatic test equipment (ATE) environment. This device meets the V_X specification under actual use conditions.
3. In all cases, input waveform timing is marked at the differential cross-point of the input signals.
4. The input signal edge rate of 1.8V/ns or greater is to be maintained in the 20% to 80% range of the input waveform.

SINGLE-ENDED INPUT AC TEST CONDITIONS FOR 1.8V LVTTL

Symbol	Parameter	Value	Units
V_{IH}	Input HIGH Voltage(1)	V_{DDI}	V
V_{IL}	Input LOW Voltage	0	V
V_{THI}	Input Timing Measurement Reference Level(2)	$V_{DDI}/2$	mV
t_R, t_F	Input Signal Edge Rate(3)	2	V/ns

NOTES:

1. V_{DDI} is the nominal 1.8V supply (1.8V ± 0.15V) of the part or source driving the input.
2. A nominal 900mV timing measurement reference level is specified to allow constant, repeatable results in an automatic test equipment (ATE) environment.
3. The input signal edge rate of 2V/ns or greater is to be maintained in the 10% to 90% range of the input waveform.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

All outputs at the same interface level

Symbol	Parameter		Min.	Typ.	Max	Unit
F_{NOM}	VCO Frequency Range	see JTAG/I²C Serial Configurations: VCO Frequency Range table				
t_{RPW}	Reference Clock Pulse Width HIGH or LOW		1	—	—	ns
t_{FPW}	Feedback Input Pulse Width HIGH or LOW		1	—	—	ns
$t_{SK(B)}$	Output Matched Pair Skew(1,2,4)		—	—	50	ps
$t_{SK(O)}$	Output Skew (Rise-Rise, Fall-Fall, Nominal)(1,3)		—	—	100	ps
$t_{SK1(\omega)}$	Multiple Frequency Skew (Rise-Rise, Fall-Fall, Nominal-Divided, Divided-Divided)(1,3,4)		—	—	100	ps
$t_{SK2(\omega)}$	Multiple Frequency Skew (Rise-Fall, Nominal-Divided, Divided-Divided)(1,3,4)		—	—	400	ps
$t_{SK1(INV)}$	Inverting Skew (Nominal-Inverted)(1,3)		—	—	400	ps
$t_{SK2(INV)}$	Inverting Skew (Rise-Rise, Fall-Fall, Rise-Fall, Inverted-Divided)(1,3,4)		—	—	400	ps
$t_{SK(PR)}$	Process Skew(1,3,5)		—	—	300	ps
$t(\phi)$	REF Input to FB Static Phase Offset(6)		-100	—	100	ps
t_{ODCV}	Output Duty Cycle Variation from 50%(7)	HSTL / eHSTL / 1.8V LVTTL	-375	—	375	ps
		2.5V LVTTL	-275	—	275	
t_{ORISE}	Output Rise Time(8)	HSTL / eHSTL / 1.8V LVTTL	—	—	1.2	ns
		2.5V LVTTL	—	—	1	
t_{OFALL}	Output Fall Time(8)	HSTL / eHSTL / 1.8V LVTTL	—	—	1.2	ns
		2.5V LVTTL	—	—	1	
t_L	Power-up PLL Lock Time(9)		—	—	4	ms
$t_{L(\omega)}$	PLL Lock Time After Input Frequency Change(9)		—	—	1	ms
$t_{L(REFSEL1)}$	PLL Lock Time After Change in REF_SEL (9,11)		—	—	100	µs
$t_{L(REFSEL2)}$	PLL Lock Time After Change in REF_SEL (REF_1 and REF_0 are different frequency)(9)		—	—	1	ms
$t_{L(PD)}$	PLL Lock Time After Asserting $\overline{PD}$ Pin(9)		—	—	1	ms
$t_{JIT(CC)}$	Cycle-to-Cycle Output Jitter (peak-to-peak)(10)		—	50	75	ps
$t_{JIT(PER)}$	Period Jitter (peak-to-peak)(10)		—	—	75	ps
$t_{JIT(HP)}$	Half Period Jitter (peak-to-peak, QFB/$\overline{QFB}$ only)(10, 12)		—	—	125	ps
$t_{JIT(DUTY)}$	Duty Cycle Jitter (peak-to-peak)(10)		—	—	100	ps
V_{OX}	HSTL and eHSTL Differential True and Complementary Output Crossing Voltage Level QFB/$\overline{QFB}$ only(12)		$V_{DDQN}/2$ - 150	$V_{DDQN}/2$	$V_{DDQN}/2$ + 150	mV

NOTES:

1. Skew is the time between the earliest and latest output transition among all outputs when all outputs are loaded with the specified load.
2. $t_{SK(B)}$ is the skew between a pair of outputs (nQ0 and nQ1) when all outputs are selected as the same class.
3. The measurement is made at $V_{DDQN}/2$.
4. There are three classes of outputs: nominal (zero delay), inverted, and divided (divide-by-2 or divide-by-4 mode).
5. $t_{SK(PR)}$ is the output to corresponding output skew between any two devices operating under the same conditions (V_{DD} and V_{DDQN}, ambient temperature, air flow, etc.).
6. $t(\phi)$ is measured with REF and FB the same type of input, the same rise and fall times. For 1.8V / 2.5V LVTTL input and output, the measurement is taken from V_{THI} on REF to V_{THI} on FB. For HSTL / eHSTL input and output, the measurement is taken from the crosspoint of REF/$\overline{REF}$ to the crosspoint of FB/$\overline{FB}$. All outputs are set to zero delay, FB input divider set to divide-by-one, and Bit 60 = 1.
7. t_{ODCV} is measured with all outputs selected for zero delay.
8. Output rise and fall times are measured between 20% to 80% of the actual output voltage swing.
9. t_L, $t_{L(\omega)}$, $t_{L(REFSEL1)}$, $t_{L(REFSEL2)}$, and $t_{L(PD)}$ are the times that are required before the synchronization is achieved. These specifications are valid only after V_{DD}/V_{DDQN} is stable and within the normal operating limits. These parameters are measured from the application of a new signal at REF or FB, or after $\overline{PD}$ is (re)asserted until $t(\phi)$ is within specified limits.
10. The jitter parameters are measured with all outputs selected for zero delay, FB input divider is set to divide-by-one, and Bit 60 = 1.
11. Both REF inputs must be the same frequency, but up to ±180° out of phase.
12. For HSTL/eHSTL outputs only.

AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

All outputs at the different interface levels

Symbol	Parameter		Min.	Typ.	Max	Unit
F_{NOM}	VCO Frequency Range	see JTAG/I²C Serial Configurations: VCO Frequency Range table				
t_{RPW}	Reference Clock Pulse Width HIGH or LOW		1	—	—	ns
t_{FPW}	Feedback Input Pulse Width HIGH or LOW		1	—	—	ns
$t_{SK(B)}$	Output Matched Pair Skew(1,2,4)		—	—	200	ps
$t_{SK(O)}$	Output Skew (Rise-Rise, Fall-Fall, Nominal)(1,3)		—	—	250	ps
$t_{SK1(\omega)}$	Multiple Frequency Skew (Rise-Rise, Fall-Fall, Nominal-Divided, Divided-Divided)(1,3,4)		—	—	500	ps
$t_{SK2(\omega)}$	Multiple Frequency Skew (Rise-Fall, Nominal-Divided, Divided-Divided)(1,3,4)		—	—	500	ps
$t_{SK1(INV)}$	Inverting Skew (Nominal-Inverted)(1,3)		—	—	500	ps
$t_{SK2(INV)}$	Inverting Skew (Rise-Rise, Fall-Fall, Rise-Fall, Inverted-Divided)(1,3,4)		—	—	500	ps
$t_{SK(PR)}$	Process Skew(1,3,5)		—	—	400	ps
$t(\phi)$	REF Input to FB Static Phase Offset(6)		-200	—	200	ps
t_{ODCV}	Output Duty Cycle Variation from 50%(7)	HSTL / eHSTL / 1.8V LVTTL	-475	—	475	ps
		2.5V LVTTL	-375	—	375	
t_{ORISE}	Output Rise Time(8)	HSTL / eHSTL / 1.8V LVTTL	—	—	1.2	ns
		2.5V LVTTL	—	—	1	
t_{OFALL}	Output Fall Time(8)	HSTL / eHSTL / 1.8V LVTTL	—	—	1.2	ns
		2.5V LVTTL	—	—	1	
t_L	Power-up PLL Lock Time(9)		—	—	4	ms
$t_{L(\omega)}$	PLL Lock Time After Input Frequency Change(9)		—	—	1	ms
$t_{L(REFSEL1)}$	PLL Lock Time After Change in REF_SEL (9,11)		—	—	100	µs
$t_{L(REFSEL2)}$	PLL Lock Time After Change in REF_SEL (REF_1 and REF_0 are different frequency)(9)		—	—	1	ms
$t_{L(PD)}$	PLL Lock Time After Asserting $\overline{PD}$ Pin(9)		—	—	1	ms
$t_{JIT(CC)}$	Cycle-to-Cycle Output Jitter (peak-to-peak)(10)		—	—	100	ps
$t_{JIT(PER)}$	Period Jitter (peak-to-peak)(10)		—	—	150	ps
$t_{JIT(HP)}$	Half Period Jitter (peak-to-peak, QFB/$\overline{QFB}$ only)(10, 12)		—	—	200	ps
$t_{JIT(DUTY)}$	Duty Cycle Jitter (peak-to-peak)(10)		—	—	150	ps
V_{OX}	HSTL and eHSTL Differential True and Complementary Output Crossing Voltage Level QFB/$\overline{QFB}$ only(12)		$V_{DDQN}/2$ - 150	$V_{DDQN}/2$	$V_{DDQN}/2$ + 150	mV

NOTES:

1. Skew is the time between the earliest and latest output transition among all outputs when all outputs are loaded with the specified load.
2. $t_{SK(B)}$ is the skew between a pair of outputs (nQ0 and nQ1) when all outputs are selected as the same class.
3. The measurement is made at $V_{DDQN}/2$.
4. There are three classes of outputs: nominal (zero delay), inverted, and divided (divide-by-2 or divide-by-4 mode).
5. $t_{SK(PR)}$ is the output to corresponding output skew between any two devices operating under the same conditions (V_{DD} and V_{DDQN}, ambient temperature, air flow, etc.).
6. $t(\phi)$ is measured with REF and FB the same type of input, the same rise and fall times. For 1.8V / 2.5V LVTTL input and output, the measurement is taken from V_{THI} on REF to V_{THI} on FB. For HSTL / eHSTL input and output, the measurement is taken from the crosspoint of REF/$\overline{REF}$ to the crosspoint of FB/$\overline{FB}$. All outputs are set to zero delay, FB input divider set to divide-by-one, and Bit 60 = 1.
7. t_{ODCV} is measured with all outputs selected for zero delay.
8. Output rise and fall times are measured between 20% to 80% of the actual output voltage swing.
9. t_L, $t_{L(\omega)}$, $t_{L(REFSEL1)}$, $t_{L(REFSEL2)}$, and $t_{L(PD)}$ are the times that are required before the synchronization is achieved. These specifications are valid only after V_{DD}/V_{DDQN} is stable and within the normal operating limits. These parameters are measured from the application of a new signal at REF or FB, or after $\overline{PD}$ is (re)asserted until $t(\phi)$ is within specified limits.
10. The jitter parameters are measured with all outputs selected for zero delay, FB input divider is set to divide-by-one, and Bit 60 = 1.
11. Both REF inputs must be the same frequency, but up to ±180° out of phase.
12. For HSTL/eHSTL outputs only.

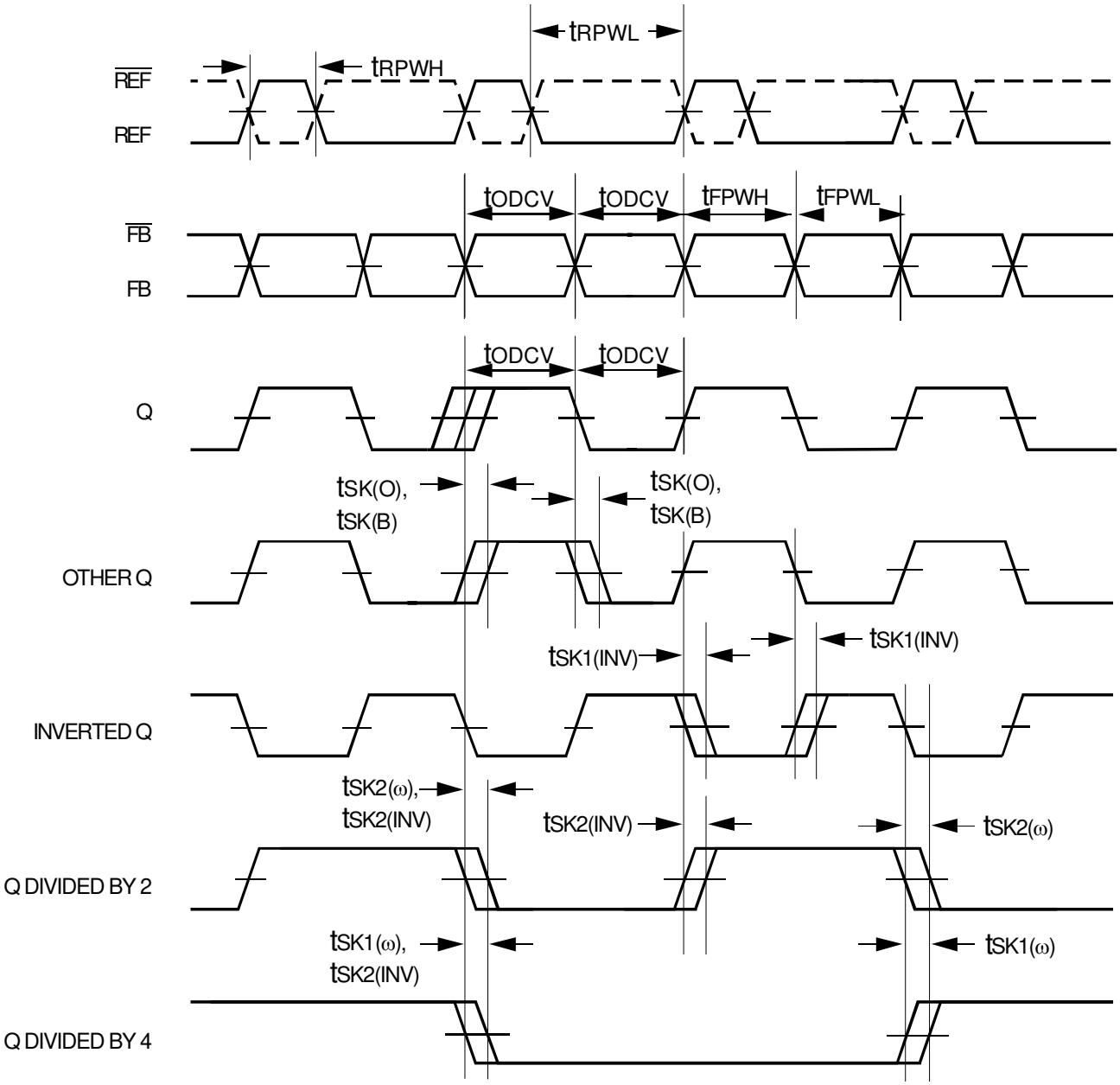
AC DIFFERENTIAL INPUT SPECIFICATIONS(1)

Symbol	Parameter	Min.	Typ.	Max	Unit
t_W	Reference/Feedback Input Clock Pulse Width HIGH or LOW (HSTL/eHSTL outputs)(2)	1	—	—	ns
	Reference/Feedback Input Clock Pulse Width HIGH or LOW (2.5V / 1.8V LVTTL outputs)(2)	1	—	—	
HSTL/eHSTL/1.8V LVTTL/2.5V LVTTL					
V_{DIF}	AC Differential Voltage(3)	400	—	—	mV
V_{IH}	AC Input HIGH(4,5)	Vx + 200	—	—	mV
V_{IL}	AC Input LOW(4,6)	—	—	Vx - 200	mV
LVEPECL					
V_{DIF}	AC Differential Voltage(3)	400	—	—	mV
V_{IH}	AC Input HIGH(4)	1275	—	—	mV
V_{IL}	AC Input LOW(4)	—	—	875	mV

NOTES:

1. For differential input mode, Bits 35 - 30 = 1.
2. Both differential input signals should not be driven to the same level simultaneously. The input will not change state until the inputs have crossed and the voltage range defined by V_{DIF} has been met or exceeded.
3. Differential mode only. V_{DIF} specifies the minimum input voltage (V_{TR} - V_{CP}) required for switching where V_{TR} is the "true" input level and V_{CP} is the "complement" input level. The AC differential voltage must be achieved to guarantee switching to a new state.
4. For single-ended operation, $\overline{REF}_{[1:0]}/V_{REF[1:0]}$ is tied to the DC voltage $V_{REF[1:0]}$. Refer to each input interface's DC specification for the correct $V_{REF[1:0]}$ range.
5. Voltage required to switch to a logic HIGH, single-ended operation only.
6. Voltage required to switch to a logic LOW, single-ended operation only.

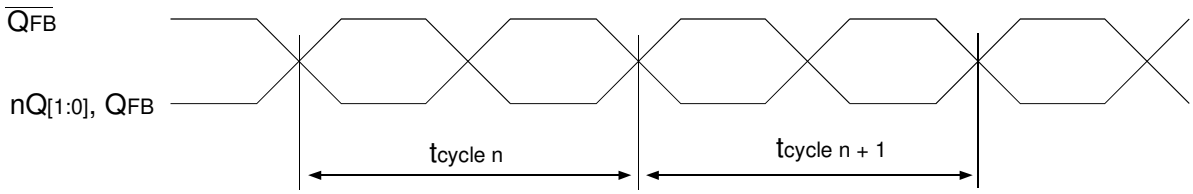
AC TIMING DIAGRAM(1)



NOTE:

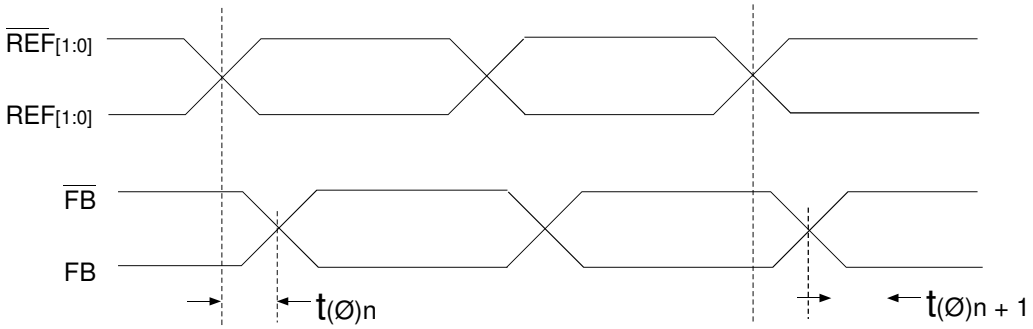
1. The AC TIMING DIAGRAM applies to Bit 58 = 1. For Bit 58 = 0, the negative edge of FB aligns with the negative edge of $REF_{[1:0]}$, divided outputs change on the negative edge of $REF_{[1:0]}$, and the positive edges of the divide-by-2 and divide-by-4 signals align.

JITTER AND OFFSET TIMING WAVEFORMS



$$t_{jit(cc)} = \left| t_{cycle\ n} - t_{cycle\ n+1} \right|$$

Cycle-to-Cycle jitter

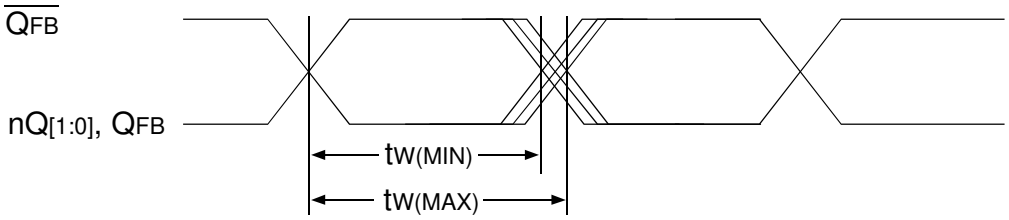


$$t_{(Ø)} = \frac{\sum_{1}^{n=N} t_{(Ø)n}}{N}$$

(N is a large number of samples)

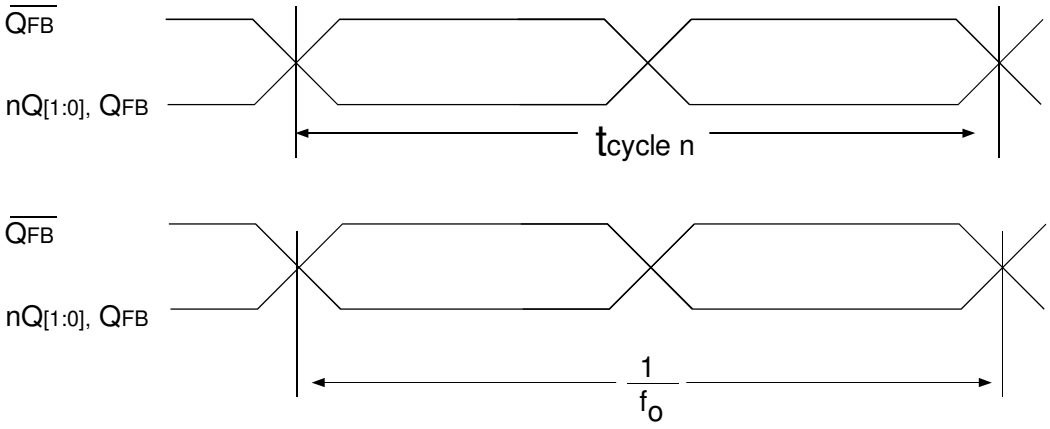
Static Phase Offset

NOTE:
1. Diagram for Bit 58 = 1 and HSTL / eHSTL input and output.



$$t_{JIT(DUTY)} = \left| t_{W(MAX)} - t_{W(MIN)} \right|$$

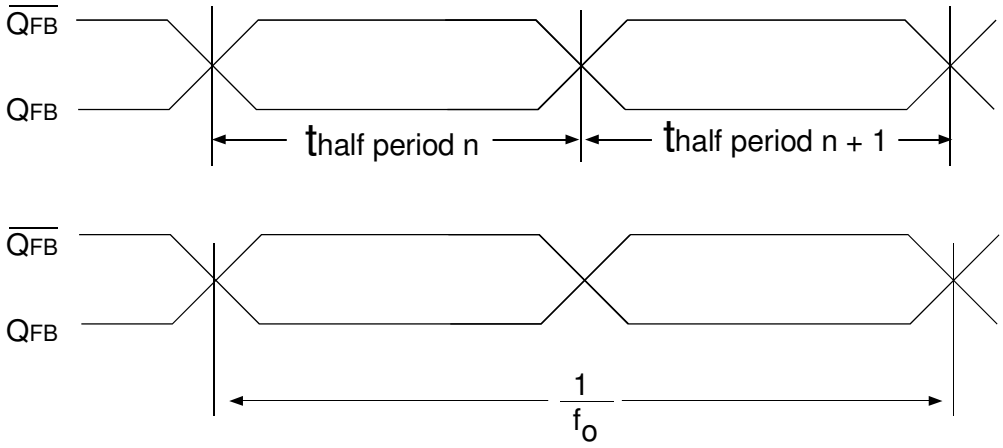
Duty-Cycle Jitter



$$t_{jit(per)} = \left| t_{cycle\ n} - \frac{1}{f_o} \right|$$

Period jitter

NOTE:
1. 1/fo = average period.

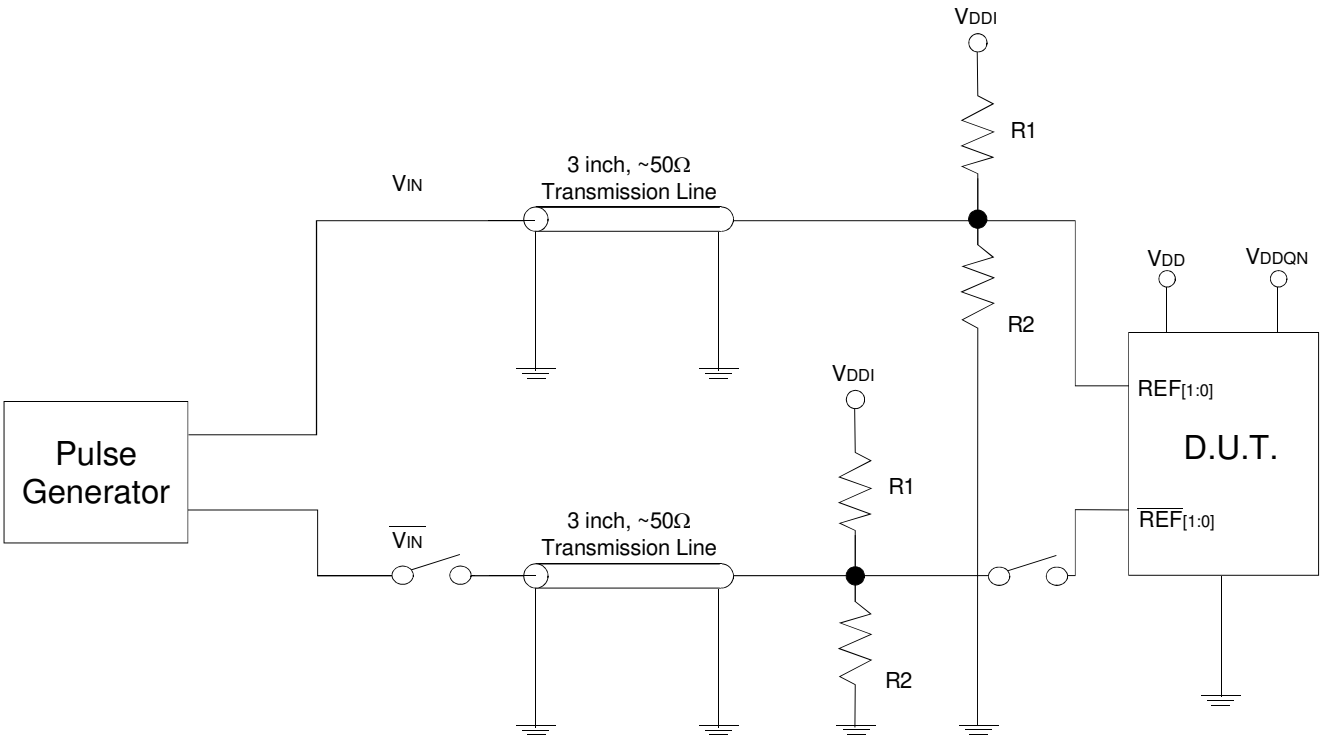


$$t_{jit(hper)} = \left| t_{half\ period\ n} - \frac{1}{2*f_o} \right|$$

Half-Period jitter

NOTE:
1. 1/fo = average period.

TEST CIRCUITS AND CONDITIONS



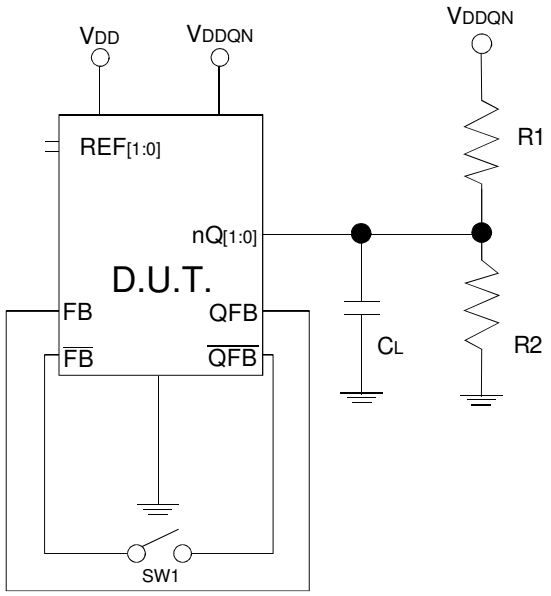
Test Circuit for Differential Input *(1)*

DIFFERENTIAL INPUT TEST CONDITIONS

Symbol	V_{DD} = 2.5V ± 0.2V	Unit
R1	100	Ω
R2	100	Ω
V_{DDI}	V_{CM}*2	V
V_{THI}	HSTL: Crossing of REF[1:0] and $\overline{REF}$[1:0] eHSTL: Crossing of REF[1:0] and $\overline{REF}$[1:0] LVEPECL: Crossing of REF[1:0] and $\overline{REF}$[1:0] 1.8V LVTTL: V_{DDI}/2 2.5V LVTTL: V_{DD}/2	V

NOTE:

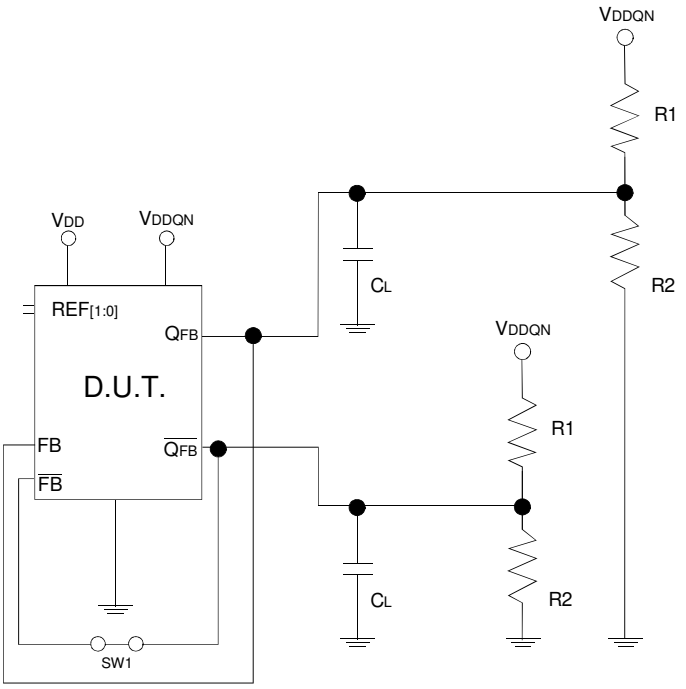
1. This input configuration is used for all input interfaces. For single-ended testing, the $\overline{REF}$[1:0] must be left floating. For testing single-ended in differential input mode, the $\overline{V_{IN}}$ should be floating.



Test Circuit for Outputs

OUTPUT TEST CONDITIONS

Symbol	V_{DD} = 2.5V ± 0.2V V_{DDQN} = Interface Specified	Unit
C_L	15	pF
R1	100	Ω
R2	100	Ω
V_{THO}	$V_{DDQN}/2$	V
SW1	1.8V/2.5V LVTTL	Open
	HSTL/eHSTL	Closed



Test Circuit for Differential Feedback

DIFFERENTIAL FEEDBACK TEST CONDITIONS

Symbol	V_{DD} = 2.5V ± 0.2V V_{DDQN} = Interface Specified	Unit
C_L	15	pF
R1	100	Ω
R2	100	Ω
V_{OX}	HSTL: Crossing of Q_{FB} and $\overline{Q_{FB}}$ eHSTL: Crossing of Q_{FB} and $\overline{Q_{FB}}$	V
V_{THO}	1.8V LVTTL: $V_{DDQN}/2$ 2.5V LVTTL: $V_{DDQN}/2$	V
SW1	1.8V/2.5V LVTTL	Open
	HSTL/eHSTL	Closed