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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# QUAD OUTPUT CLOCK GENERATOR

**IDT5V927**

## FEATURES:

- 3V to 3.6V operating voltage
- 50MHz to 160MHz output frequency range
- Input from fundamental crystal oscillator or external source
- Internal PLL feedback (loading feedback output relative to other outputs, adjusts propagation delay between REF inputs and outputs)
- Select inputs ($S_{[1:0]}$) for FB divide selection (multiply ratio of 2, 3, 4, 4.25, 5, 6, 6.25, and 8)
- Low jitter
- PLL bypass for testing and power-down control (S1 = H, S0 = H, powers part down <500µA)
- Available in TSSOP package

## APPLICATIONS:

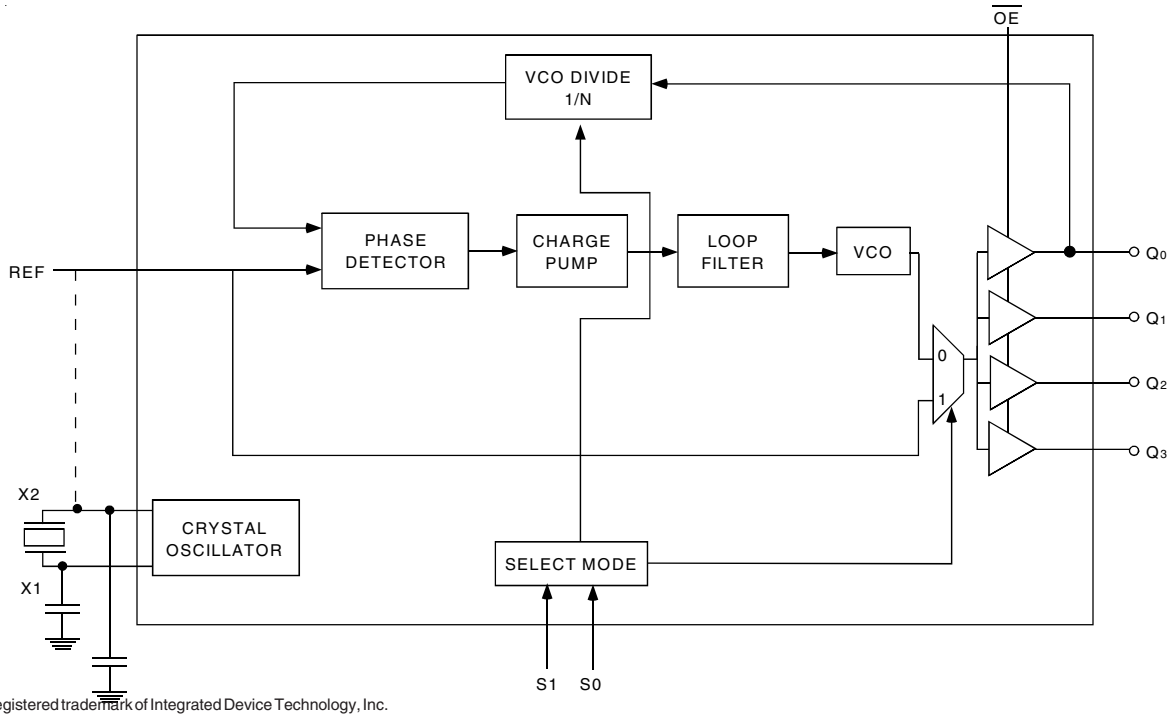
- Gigabit ethernet
- Router
- Network switches
- SAN
- Instrumentation
- Fibre channel

## DESCRIPTION:

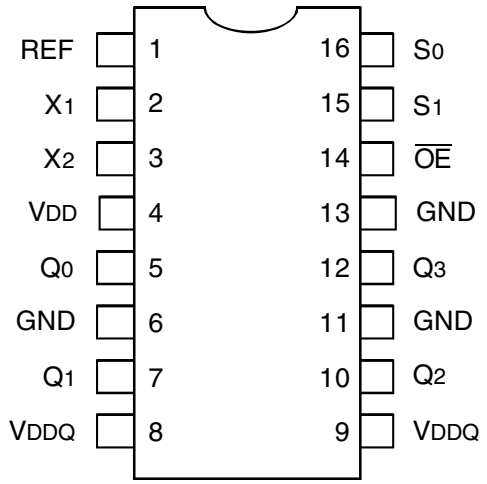
The IDT5V927 is a low-cost, low skew, low jitter, and high-performance clock synthesizer. It has been specially designed to interface with Gigabit Ethernet (125MHz), Fibre Channel (106.25MHz), and OC-3 (155.52MHz) applications. It can be programmed to provide output frequencies ranging from 50MHz to 160MHz, with input frequencies ranging from 6.25MHz to 80MHz.

The IDT5V927 includes an internal RC filter that provides excellent jitter characteristics and eliminates the need for external components. When using the optional crystal input, the chip accepts a 10 - 40MHz fundamental mode crystal with a maximum equivalent series resistance of 50Ω.

## FUNCTIONAL BLOCK DIAGRAM



## PIN CONFIGURATION




**TSSOP**
**TOP VIEW**

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Description | Max. | Unit |
|---|---|---|---|
| $V_{DD}/V_{DDQ}$ | Supply Voltage to Ground | – 0.5 to +4.6 | V |
| $V_I$ | Input Voltage | – 0.5 to +4.6 | V |
| $I_O$ | Output Current | ±50 | mA |
| $T_{STG}$ | Storage Temperature | – 65 to +150 | °C |
| $T_J$ | Junction Temperature | 150 | °C |

**NOTE:**
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## PIN DESCRIPTION

| Pin Name | Type | Description |
|---|---|---|
| $S_{[1:0]}$ | I | Three level divider/mode select pins. Float to MID. |
| $\overline{OE}$ | I | Output enable bar. $\overline{OE}$ has a pull-down. Output $Q_{[1:3]}$ tristated when HIGH. Output $Q_0$ remains running when in PLL mode and tri-states when in TEST mode. |
| $X_1$ | I | Crystal oscillator input. Connect to GND if oscillator not required. |
| $X_2$ | I | Crystal oscillator output. Leave unconnected for clock input. |
| REF | I | Input clock. Connect to $X_2$ if crystal oscillator is used. |
| $Q_{[1:3]}$ | O | Output at N*REF frequency |
| $Q_0$ | O | Output at N*REF internally connected for PLL feedback |
| $V_{DDQ}$ | PWR | Power supply for the device outputs. Connect to $V_{DD}$ on PCB. |
| $V_{DD}$ | PWR | Power supply for the device core and inputs. Connect to $V_{DD}$ on PCB. |
| GND | PWR | Ground supply |

## CRYSTAL SPECIFICATION

The crystal oscillators should be fundamental mode quartz crystals: overtone crystals are not suitable. Crystal frequency should be specified for parallel resonance with 50Ω maximum equivalent series resonance. Crystal tuning capacitors should be connected from $X_2$/REF to GND and from $X_1$ to GND.

## DIVIDE SELECTION TABLE(1)

| S1 | S0 | Divide-by-N Value | Mode |
|---|---|---|---|
| L | L | 2 | PLL |
| L | M | 3 | PLL |
| L | H | 4 | PLL |
| M | L | 4.25 | PLL |
| M | M | 5 | PLL |
| M | H | 6 | PLL |
| H | L | 6.25 | PLL |
| H | M | 8 | PLL |
| H | H | TEST | TEST(2) |

**NOTES:**
1. H = HIGH
   M = MEDIUM
   L = LOW
2. Test mode for low frequency testing. In this mode, REF clock bypasses the VCO (VCO powered down) and the crystal oscillator is powered down.

## COMMON OUTPUT FREQUENCY EXAMPLES (MHz)

| Output | 50 | 60 | 64 | 72 | 75 | 80 | 90 | 100 |
|---|---|---|---|---|---|---|---|---|
| Input | 25 | 10 | 16 | 12 | 25 | 10 | 15 | 20 |
| FB Divide Selection S[1:0] | LL | MH | LH | MH | LM | HM | MH | MM |

| Output | 106.25 | 106.25 | 120 | 125 | 125 | 125 | 150 | 155.52 |
|---|---|---|---|---|---|---|---|---|
| Input | 17 | 25 | 15 | 20 | 25 | 62.5 | 25 | 19.44 |
| FB Divide Selection S[1:0] | HL | ML | HM | HL | MM | LL | MH | HM |

## OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}/V_{DDQ}$ | Power Supply Voltage | 3 | 3.3 | 3.6 | V |
| $T_A$ | Operating Temperature | -40 | 25 | +85 | °C |
| $C_L$ | Output Load Capacitance | — | — | 15 | pF |
| $C_{IN}$ | Input Capacitance, OE, F = 1MHz, $V_{IN}$ = 0V, $T_A$ = 25°C | — | 5 | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:
Industrial: $T_A$ = –40°C to +85°C, $V_{DD}/V_{DDQ}$ = 3.3V ±0.3V

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage | | | — | — | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2 | — | — | V |
| $V_{IHH}$ | Input HIGH Voltage | 3-level input only | | $V_{DD}$ - 0.6 | — | — | V |
| $V_{IMM}$ | Input MID Voltage | 3-level input only | | $V_{DD}/2$ - 0.3 | — | $V_{DD}/2$ + 0.3 | V |
| $V_{ILL}$ | Input LOW Voltage | 3-level input only | | — | — | 0.6 | V |
| $I_{IN}$ | Input Leakage Current (REF input only) | $V_{IN}$ = $V_{DD}$ or GND, $V_{DD}$ = Max. | | -5 | — | +5 | µA |
| $I_3$ | 3-Level Input DC Current, S[1:0] | $V_{IN}$ = $V_{DD}$ | HIGH Level | — | — | +200 | µA |
| | | $V_{IN}$ = $V_{DD}/2$ | MID Level | -50 | — | +50 | |
| | | $V_{IN}$ = GND | LOW Level | -200 | — | — | |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | $\overline{OE}$ | — | — | 100 | µA |
| | | $V_{IN}$ = $V_{DD}$, S[1:0] = HH | $X_1$ | — | 2 | 4 | mA |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 12mA | | — | — | 0.4 | V |
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = -12mA | | 2.4 | — | — | V |

## POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions (1) | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_PD}$ | Power Down Current | $V_{DD}$ = Max.<br>$S_{[1:0]}$ = HH<br>$\overline{OE}$ = L; REF = L; $X_1$ = L<br>All outputs unloaded | — | — | 500 | µA |
| $\Delta I_{DD}$ | Supply Current per Input | $V_{DD}$ = Max., $V_{IN}$ = 3V | — | — | 30 | µA |
| $I_{DD}$ | Dynamic Supply Current | $V_{DD}$ = 3.6V<br>$S_{[1:0]}$ = LL<br>$\overline{OE}$ = L<br>$F_{OUT}$ = 150MHz<br>All outputs unloaded | — | — | 130 | mA |

**NOTE:**
1. For conditions shown as Min. or Max., use the appropriate values specified under DC Electrical Characteristics.

## AC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

| Symbol | Parameter | Test Conditions | | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|---|
| $t_R, t_F$ | Rise Time, Fall Time | 0.8V to 2V | | — | 0.7 | 1.5 | ns |
| $d_T$ | Output/Duty Cycle | $V_T = V_{DDQ}/2$ | | 45 | 50 | 55 | % |
| $t_{PD}$ | REF to $Q_0$(1) | $V_T = V_{DDQ}/2$ | $f_{OUT} \geq$ 100MHz, all N | -200 | — | 200 | ps |
| | | | 50 < $f_{OUT}$ < 160MHz, N ≤ 4 | -200 | — | 200 | |
| | | | 50 < $f_{OUT}$ < 160MHz, N ≥ 4.25 | -350 | — | 350 | |
| $t_{SK}$ | Output to Output Skew ($Q_0$ to $Q_{1:3}$) | Equal loads | | — | — | 150 | ps |
| $t_J$ | Cycle - Cycle Jitter | $f_{OUT} \geq$ 100MHz | | -155 | — | 155 | ps |
| $f_{OUT}$ | Output Frequency | | | 50 | — | 160 | MHz |

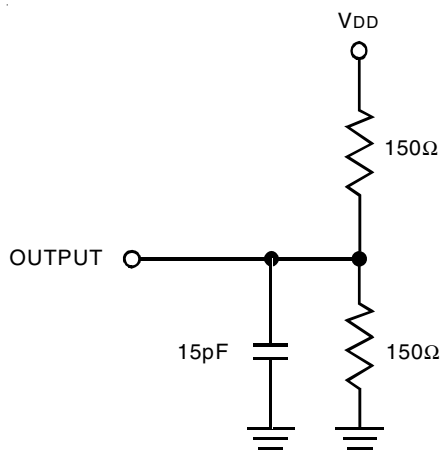
**NOTE:**
1. When using a clock input.

## INPUT TIMING REQUIREMENTS

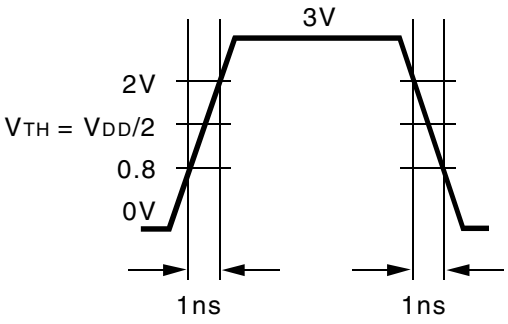
| Symbol | Description(1) | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_R, t_F$ | Maximum input rise and fall time, 0.8V to 2V(2) | — | 10 | ns/V |
| $t_{PWC}$ | Input clock pulse, HIGH or LOW(2) | 2 | — | ns |
| $D_H$ | Input duty cycle(2) | 10 | 90 | % |
| $f_{OSC}$ | XTAL oscillator frequency | — | 40 | MHz |
| $f_{IN}$ | Input frequency(2) | 50/N | 160/N | MHz |

**NOTES:**
1. Where pulse width implied by $D_H$ is less than the $t_{PWC}$ limit, $t_{PWC}$ limit applies,
2. When using a clock input.

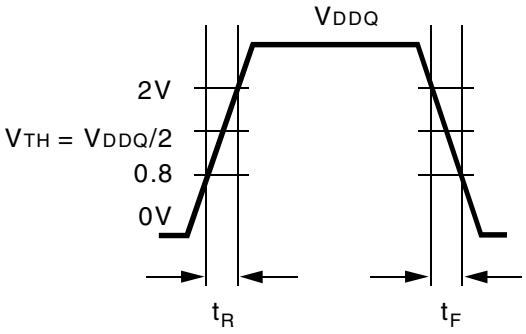
## AC TEST LOADS AND WAVEFORMS




*AC Test Load*

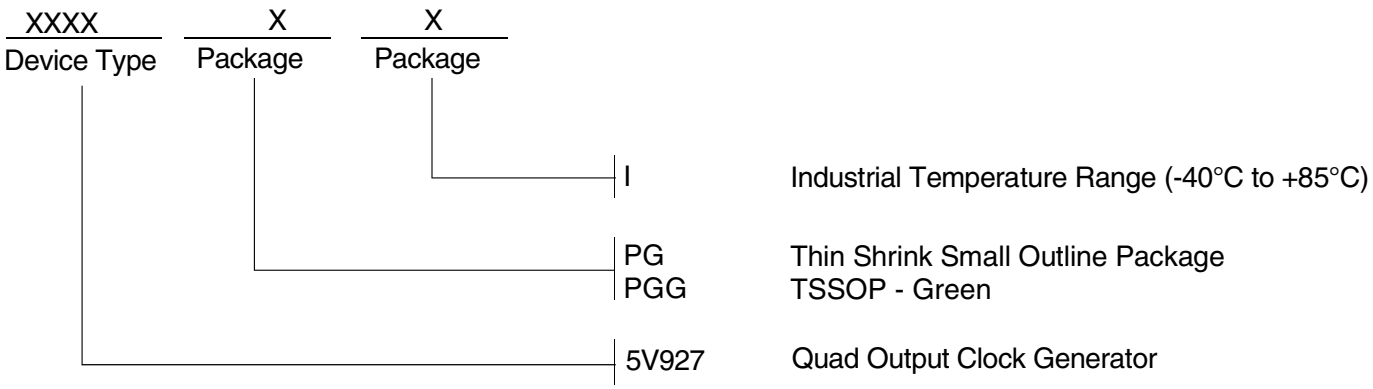



*Input Test Waveform*




*Output Waveform*

## ORDERING INFORMATION




*CORPORATE HEADQUARTERS*
6024 Silver Creek Valley Road
San Jose, CA 95138

*for SALES:*
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

*for Tech Support:*
clockhelp@idt.com