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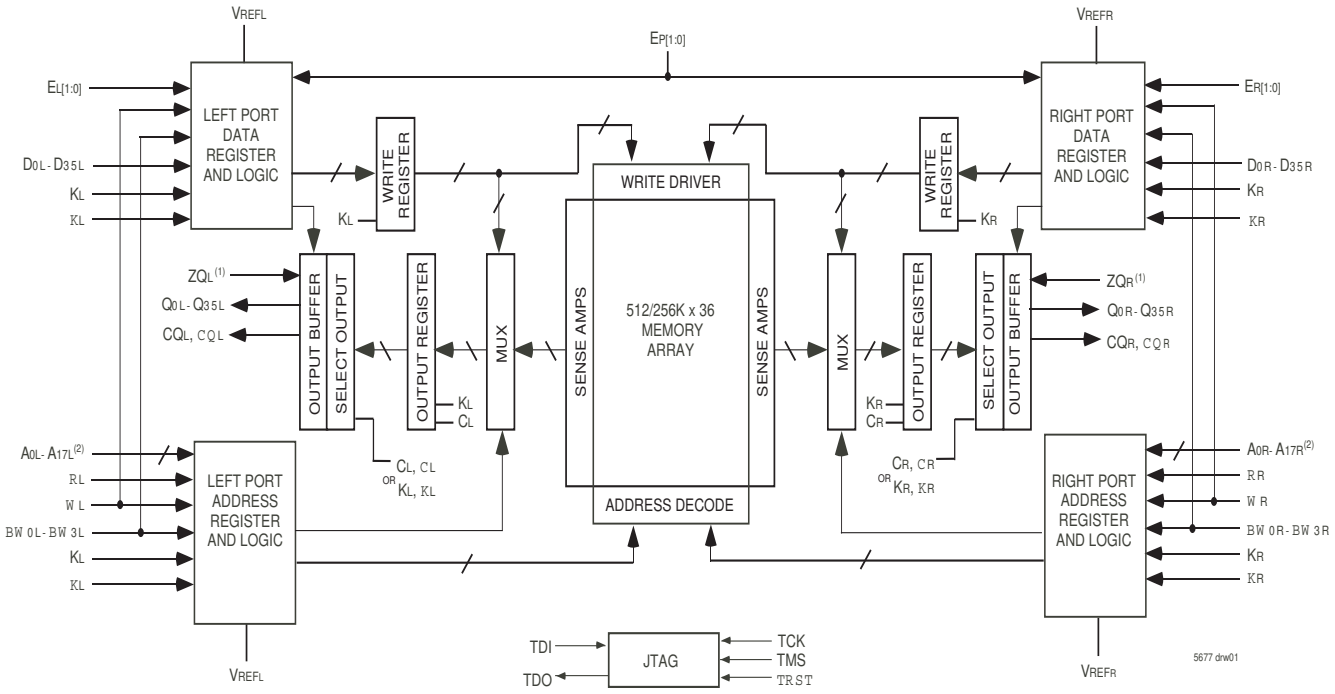
512K/256K x36 SYNCHRONOUS DUAL QDR-II™

PRELIMINARY DATASHET
IDT70P3537
IDT70P3517

Features

- **18Mb Density (512K x 36)**
  - *Also available 9Mb Density* (256K x 36)
- ***QDR-II x 36 Burst-of-2 Interface***
  - *Commercial: 233MHz, 250MHz*
- **Two independent ports**
  - *True Dual-Port Access to common memory*
- **Separate, Independent Read and Write Data Buses on each Port**
  - *Supports concurrent transactions*
- **Two-Word Burst on all DPRAM accesses**
- **DDR (Double Data Rate) Multiplexed Address Bus**
  - *One Read and One Write request per clock cycle*
- **DDR (Double Data Rate) Data Buses**
  - *Four word burst data (Two Read and Two Write) per clock on each port*
  - *Four word transfers each of Read & Write per clock cycle per port (four word bursts on 2 ports)*
- **Octal Data Rate**
- **Port Enable pins (E_0,E_1) for depth expansion**
- **Dual Echo Clock Output with DLL-based phase alignment**
- **High Speed Transceiver Logic inputs**
  - *scaled to receive signals from 1.4V to 1.9V*
- **Scalable output drivers**
  - *Drives HSTL, 1.8V TTL or any voltage level from 1.4V to 1.9V*
  - *Output impedance adjustable from 35 ohms to 70 ohms*
- **1.8V Core Voltage (V_{DD})**
- **576-ball Flip Chip BGA (25mm x 25mm, 1.0mm ball pitch)**
- **JTAG Interface - IEEE 1149.1 Compliant**

Functional Block Diagram

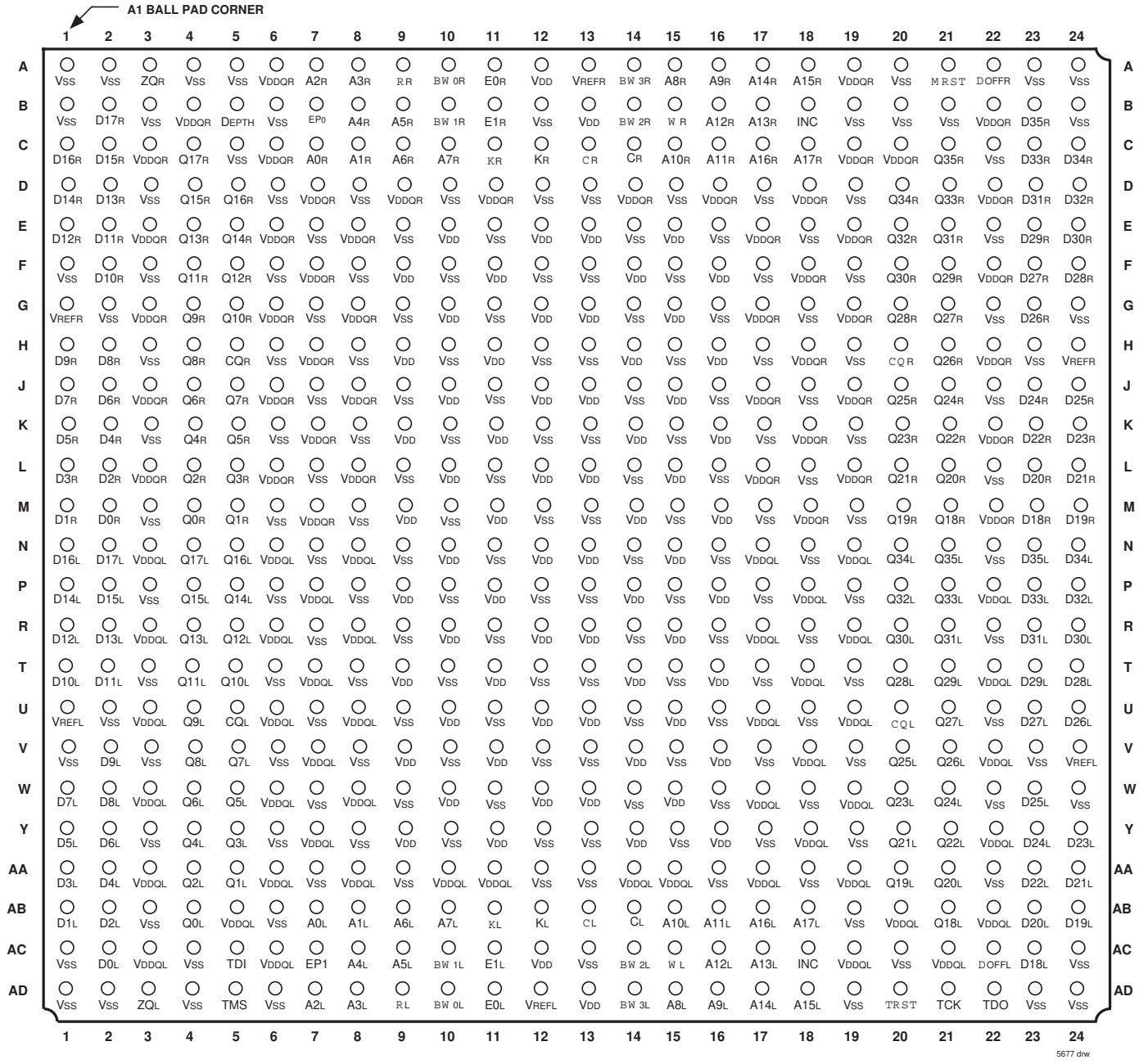


NOTES:

1. Input pin to adjust the device outputs to the system data bus impedance.
2. Address A17 is a INC for IDT70P3517. Disabled input pin (Diode tied to V_{DD} and V_{SS}).

Pin Configuration

70P3537
70P3517
RM-576 Ball Flip Chip BGA
Top View



NOTE:

1. The package is 25mm x 25mm x 2.55mm with 1.0mm ball pitch; the customer will have to provide external airflow of 100LFM (0.5m/s) or higher at 250MHz.

Functional Description

As a memory standard, the (Quad Data Rate) QDR-II SRAM interface has become increasingly common in high performance networking systems. With the QDR-II interface/configuration, memory throughput is increased without increasing the clock rate via the use of two unidirectional buses on each of providing 2 ports of QDR-II makes this a Dual-QDRII Static Ram two ports to transfer data without the need for bus turnaround.

Dual QDR-II Static RAMs are high speed synchronous memories supporting two independent double-data-rate (DDR) read and write data ports. This scheme allows simultaneous read and write access for the maximum device throughput - two data items are passed with each read or write. Four data word transfers occur per clock cycle, providing quad-data-rate (QDR) performance on each port. Comparing this with standard SRAM common I/O single data rate (SDR) devices, a four to one increase in data access is achieved at equivalent clock speeds. IDT70P3537/70P3517 Dual QDR-II Static RAM devices, are capable of sustaining full bandwidth on both the input and output buses simultaneously. Using independent buses for read and write data access simplifies design by eliminating the need for bidirectional buses. And all data are in two word bursts, (with addressing capability to the burst level).

Devices with QDR-II interfaces include network processor units (NPUs) and field programmable gate arrays (FPGAs).

IDT70P3537/70P3517 Dual QDR-II Static RAMs support unidirectional 36-bit read and write interfaces. These data inputs and outputs operate simultaneously, thus eliminating the need for high-speed bus turnarounds (i.e. no dead cycles are present). Access to each port is accomplished using a common 18-bit address bus (17 bits for IDT70P3517). Addresses for reads and writes are latched on rising edges of the K and $\overline{K}$ input clocks, respectively.The K and $\overline{K}$ clocks are offset by 90 degrees or half a clock cycle. Each address location is associated with two 36-bit data words that burst sequentially into or out of the device. Since data can be transferred into and out of the device on every rising edge of the K and $\overline{K}$ clocks, memory bandwidth is maximized while simplifying overall design through the elimination of bus turnaround(s). IDT70P3537/70P3517 Dual QDR-II Static RAMs can support devices in a multi-drop configuration (i.e. multiple devices connected to the same interface). Through this capability, system designers can support compatible devices such as NPUs and FPGAs on the same bus at the same time.

Using independent ports for read and write access simplifies design by eliminating the need for bidirectional buses. All buses associated with Dual QDR-II Static RAMs are unidirectional and can be optimized for signal integrity at very high bus speeds. The Dual QDR-II Static RAM has scalable output impedance on its data output bus and echo clocks allowing the user to tune the bus for low noise and high performance.

IDT70P3537/70P3517 Dual QDR-II Static RAMs have a single DDR address bus per port with multiplexed read and write addresses. All read addresses are received on the first half of the clock cycle and all write addresses are received on the second half of the clock cycle. The byte write signals are received on both halves of the clock cycle simultaneously with the data they are controlling on the data input bus.

The Dual QDR-II Static RAM device has echo clocks, which provide the user with a clock that is precisely timed to the data output and tuned with matching impedance and signal quality. The user can use the echo clock for downstream clocking of the data. For the user, echo clocks eliminate the need to produce alternate clocks with precise timing, positioning, and signal qualities to guarantee data capture. Since the echo clocks are generated by the same source that drives the data output, the relationship to the data is NOT significantly affected by external parameters such as voltage, temperature, and process as would be the case if the clock were generated by an outside source.Thus the echo clocks are guaranteed to be synchronized with the data.

All interfaces of Dual QDR-II Static RAMs are HSTL, allowing speeds beyond SRAM devices that use any form of TTL interface. The interface can be scaled to higher voltages (up to 1.9V) to interface with 1.8V systems, if necessary. The device has VDDQ pins and a separate Vref, allowing the user to designate the interface operational voltage independent of the device core voltage of 1.8V VDD. Output impedance control pins allow the user to adjust the drive strength to adapt to a wide range of loads and transmission lines.

Clocking

The IDT70P3537/3517 has two sets of input clocks for both the input and output, the K, $\overline{K}$ clocks and the C, $\overline{C}$ clocks. In addition, the IDT70P3537/3517 has an output "echo" clock pair, CQ and $\overline{CQ}$.

The K and $\overline{K}$ clocks are the primary device input clocks. The K clock is used to clock in the control signals ($\overline{R}$, $\overline{W}$, E[1:0], $\overline{BW}$0-3), the read address, and the first word of the data burst (D[35:0]) during a write operation. The $\overline{K}$ clock is used to clock in the control signals ($\overline{BW}_{0\text{-}3}$, E[1:0]), write address and the second word of the data burst during a write operation (D[35:0]). In the event that the user disables the C and $\overline{C}$ clocks, the K and $\overline{K}$ clocks will also be used to clock the data out of the output register and generate the echo clocks. The K and $\overline{K}$, C and $\overline{C}$,CQ and $\overline{CQ}$, pairs are offset by half a clock cycle from each other.

The C and $\overline{C}$ clocks may be used to clock the data out of the output register during read operations and to generate the echo clocks. C and $\overline{C}$ must be presented to the memory within the timing tolerances as shown in the AC Electrical Characteristics Table (Page 12). The output data from the IDT70P3537/70P3517 will be closely aligned to the C and $\overline{C}$ input, through the use of an internal DLL. When $\overline{C}$ is presented to the IDT70P3537/70P3517 the DLL will have already internally clocked the data to arrive at the device output simultaneously with the arrival of the $\overline{C}$ clock. The C and second data item of the burst will also correspond.

Single Clock Mode

The IDT70P3537/70P3517 may be operated with a single clock pair. C and $\overline{C}$ may be disabled by tying both signals high, forcing the outputs and echo clocks to be controlled instead by the K and $\overline{K}$ clocks.

DLL Operation

The DLL in the output structure of the IDT70P3537/70P3517 can be used to closely align the incoming clocks C and $\overline{C}$ with the output of the data, generating very tight tolerances between the

two. The user may disable the DLL by holding $\overline{D}_{OFF}$ low. With the DLL off, the C and $\overline{C}$ (or K and $\overline{K}$, if C and $\overline{C}$ are not used) will directly clock the output register of the IDT70P3537/70P3517. With the DLL off, there will be a propagation delay from the time the clock enters the device until the data appears at the output. QDR-II becomes QDRI™ with DLL off. First data out is referenced to C instead of $\overline{C}$.

Echo Clock

The echo clocks, CQ and $\overline{CQ}$, are generated by the C and $\overline{C}$ clocks (or K, $\overline{K}$ if C, $\overline{C}$ are disabled). The rising edge of C generates the rising edge of CQ, and the falling edge of $\overline{CQ}$. The rising edge of $\overline{C}$ generates the rising edge of $\overline{CQ}$ and the falling edge of CQ. This scheme improves the correlation of the rising and falling edges of the echo clock and will improve the duty cycle of the individual signals.

The echo clock is very closely aligned with the data, guaranteeing that the echo clock will remain closely correlated with the data, within the tolerances designated.

Normal QDR-II Read and Write Operations

The IDT70P3537/70P3517 Dual QDR-II Static RAM supports QDR-II burst-of-two read/write operations. Read operations are initiated by holding the read port select ($\overline{R}$) low, and presenting the read address to the address port during the rising edge of K which will latch the address. Data is delivered after the next rising edge of the next $\overline{K}$ (t + 1), using C and $\overline{C}$ as the output timing references; or K and $\overline{K}$, if C and $\overline{C}$ are tied high.

The write operation is a standard QDR-II burst-of-two write operation, except the data is not available to be read until the next clock cycle (this is one cycle later than standard QDR-II SRAM). Normal QDR write cycles are initiated by holding the write port select ($\overline{W}$) low at K rising edge. Also, the Byte Write inputs ($\overline{BW}_{0\text{-}3}$), designating which bytes are to be written, need to be held low for both the K and $\overline{K}$ clocks. On the rising edge of K the first word of the data must also be present on the data input bus D[35:0] observing the designated set up times. Upon the rising edge of K the first word of the burst will be latched into the input register. After K has risen, and the designated hold times observed, the second half of the clock cycle is initiated by presenting the write address to the address bus A[X:0], the $\overline{BW}$0-3 inputs for the second data word of the burst, and the second data item of the burst to the data bus D[35:0]. Upon the rising edge of $\overline{K}$, the second word of the burst will be latched, along with the designated address. Both the first and second words of the burst will be written into memory as designated by the address and byte write enables. The addresses for the write cycles is provided at the $\overline{K}$ rising edge, and data is expected at the rising edge of K and $\overline{K}$, beginning at the same K that initiated the cycle.

Programmable Impedance

An external resistor, RQ, must be connected between the ZQ pin on the IDT70P3537/70P3517 and tied to V_{SS} to allow the IDT70P3537/70P3517 to adjust its output drive impedance. The value of RQ must be 5X the value of the intended drive impedance of the IDT70P3537/70P3517. The allowable range of RQ to guarantee impedance matching with a tolerance of +/- 15% is 175 ohms to 350 ohms. The output impedance is adjusted every 1024 clock cycles to correct for drifts in supply voltage and temperature. If the user wishes to drive the output impedance of the IDT70P3537/70P3517 to its lowest value, the ZQ pin may be tied to V_{DDQ}.

Pin Definitions

Symbol[1]	Pin Function	Description
D[35:0]x	Input Synchronous	Data input signals, sampled on the rising edge of K and $\overline{K}$ clocks during valid write operations
$\overline{BW}_{0x}$, $\overline{BW}_{1x}$, $\overline{BW}_{2x}$, $\overline{BW}_{3x}$	Input Synchronous	Byte Write Selects active LOW. Sampled on the rising edge of the K and again on the rising edge of $\overline{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes not written remain unaltered. All byte writes are sampled on the same edge as the data. Deselecting a Byte Write Select will cause the corresponding byte of data to be ignored and not written in to the device. $\overline{BW}_0$ controls D[8:0], $\overline{BW}_1$ controls D[17:9], $\overline{BW}_2$ controls D[26:18], and $\overline{BW}_3$ controls D[35:27].
A[17:0]x[2]	Input Synchronous	Address Inputs. Read addresses are sampled on the rising edge of K clock during active read operations. Write addresses are sampled on the rising edge of $\overline{K}$ clock during active write operations. These address inputs are multiplxed, so that both a read and write operation can occur on the same clock cycle. These inputs are ignored when the appropriate port is deselected.
Q[35:0]x	Output Synchronous	Data Output signals. These pins drive out the requested data during a Read operation. Valid data is driven out on the rising edge of both the C and $\overline{C}$ clocks during Read operations or K and $\overline{K}$ when operating in single clock mode. When the Read port is deselected, Q[35:0] are automatically tri-stated.
$\overline{W}_x$	Input Synchronous	Write Control Logic, active LOW. Sampled on the rising edge of the positive input clock (K). When asserted active, a write operation in initiated. Deasserting will deselect the Write port. Deselecting the Write port will cause D[35:0] to be ignored.
$\overline{R}_x$	Input Synchronous	Read Control Logic, active LOW. Sampled on the rising edge of Positive Input Clock (K). When active, a Read operation is initiated. Deasserting will cause the Read port to be deselected. When deselected, the pending access is allowed to complete and the output drivers are automatically tri-stated following the next rising edge of the $\overline{C}$ clock. ($\overline{D}_{OFFx}$ = 1). Each read access consists of a burst of two sequential transfers.
Cx	Input Clock	Positive Output Clock Input. C is used in conjunction with $\overline{C}$ to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
$\overline{C}_x$	Input Clock	Negative Output Clock Input. $\overline{C}$ is used in conjunction with C to clock out the Read data from the device. C and $\overline{C}$ can be used together to deskew the flight times of various devices on the board back to the controller. See application example for further details.
Kx	Input Clock	Positive Input Clock Input. The rising edge of K is used to capture synchronous inputs to the device. Drives out data through Q[35:0] when in single clock mode. All accesses are initiated on the rising edge of K.
$\overline{K}_x$	Input Clock	Negative Input Clock Input. $\overline{K}$ is used to capture synchronous inputs being presented to the device. Drives out data through Q[35:0] when in single clock mode.
CQx	Output Clock	Synchronous Echo clock output. The rising edge of CQ is tightly matched to the synchronous data outputs and can be used as a data valid indication. CQ is free running and does not stop when the output data is tri-stated.
$\overline{CQ}_x$	Output Clock	Synchronous Echo Clock output. The rising edge of $\overline{CQ}$ is tightly matched to the synchronous data outputs and can be used as a data valid indication. $\overline{CQ}$ is free running and does not stop wehen the output data is tri-stated.
ZQx	Input	Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. Q[35:0] output impedance is set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternately, this pin can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.
EP[1:0]	Input	EP[1:0] are used to program the Port Enable pins E[1:0]. EP[1:0] are programmed by tying the pins high or low on the board. If a customer does not want to use Pins EP[1:0], then these pins should be tied low. Refer to Truth Table III for Port Enable pins.
Ex[1:0]	Input Syncronous	Two Port Enable pins E[1:0] are provided to connect to the two MSB bits on the memory controller in order to cascade up to four IDT70P3537 devices. If a customer does not want to use Pins E[1:0], then these pins should be tied low. Refer to Truth Table III for Port Enable pins. Also refer to Figure 1 showing cascade/multi-drop using port-enable (E[1:0]) pins. E[1:0] are sampled on the rising edge of K for read operations and again on rising edge of $\overline{K}$ for write operations.
$\overline{D}_{OFFx}$	Input	DLL Turn Off. When low this input will turn off the DLL inside the device. The AC timings with the DLL turned off will be different from those listed in this data sheet. There will be an increased propagation delay from the incidence of C and $\overline{C}$ to Q, or K and $\overline{K}$ to Q as configured.
$\overline{MRST}$	Input Asynchronous	Master Reset pin. When held low will reset the device.
DEPTH	Input	Connect to V_{DDQ} for 9Mb. Connect to V_{SS} for 18Mb.
TDO	Output	TDO pin for JTAG.
TCK	Input	TCK pin for JTAG.
TDI	Input	TDI pin for JTAG.
TMS	Input	TMS pin for JTAG.
$\overline{TRST}$	Input Asynchronous	Reset pin for JTAG.
INC		Should be tied to V_{CC} or V_{SS} only, or can be left as a floating pin.
V_{REFx}	Input Reference	Reference Voltage input. Static input used to set the reference level for HSTL inputs as well as AC measurement points.
V_{DD}	Power Supply	Power supply inputs to the core of the device. Should be connected to a 1.8V power supply.
V_{SS}	Ground	Ground for the device. Should be connected to ground of the system.
V_{DDQx}	Power Supply	Power supply for the outputs of the device. Should be connected to a 1.5V power supply for HSTL or scaled to the desired output voltage.

5677 tbl 01

NOTE:

1. "x" = "L" for the Left Port pins and "x" = "R" for the Right Port pins.
2. A[16:0]x for IDT70P3517.

Truth Table I - Synchronous Port Control(1)

						D(3,4)				Q(3,4)		OPERATION
K	$\overline{K}$	$\overline{R}$	$\overline{W}$	$E0^{(2)}$	$E1^{(2)}$	D(A+0)	D(A+1)	$\overline{C}$	C	Q(A+0)	Q(A+1)	
Stopped		X	X	X	X	X		Stopped		Previous state		Clock stopped
	Stopped			X	X		X		Stopped		Previous state	Clock stopped
↑		H	H	X	X	X		↑		High - Z		No operation
	↑			X	X		X		↑		High - Z	No operation
↑		X	X	F	X	X		↑		High - Z		No operation
	↑			F	X		X		↑		High - Z	No operation
↑		X	X	X	F	X		↑		High - Z		No operation
	↑			X	F		X		↑		High - Z	No operation
↑		L	X	T	T	X		↑		D_{OUT} at $\overline{C}$ (t+1)		Read
	↑			X	X		X		↑		D_{OUT} at C (t+2)	Read
↑		X	L	X	X	D_{IN} at K(t)		↑		X		Write
	↑			T	T		D_{IN} at $\overline{K}$(t)		↑		X	Write

5677 tbl 03

NOTES:

1. x = "Don't Care", H = Logic High, L = Logic Low, ↑ represents rising edge.
2. T (True) = E and EP have some polarity (device selected) on the rising edge of the appropriate clock. F (False) =E and EP have opposite polarity (device de-selected) on the rising edge of the appropriate clock. See Truth Table III.
3. "A" represents address location latched by the device when operation was initiated. A+0, A+1 represents the internal address sequence in the burst.
4. "t" represents the cycle at which a read/write operation is started. t+1 and t+2 are the first and second clock cycles respectively following clock cycle t.

Truth Table II - Write Port Enable Control(2,3)

K	$\overline{K}$	$\overline{BW}0^{(1)}$	$\overline{BW}1^{(1)}$	$\overline{BW}2^{(1)}$	$\overline{BW}3^{(1)}$	Mode
Input	Input	Input	Input	Input	Input	
↑		H	H	H	H	Write function disabled all bytes
	↑	H	H	H	H	Write function disabled all bytes
↑		L	H	H	H	Write data inputs to Byte 0 Only
	↑	L	H	H	H	Write data inputs to Byte 0 Only
↑		H	L	H	H	Write data inputs to Byte 1 Only
	↑	H	L	H	H	Write data inputs to Byte 1 Only
↑		H	H	L	H	Write data inputs to Byte 2 Only
	↑	H	H	L	H	Write data inputs to Byte 2 Only
↑		H	H	H	L	Write data inputs to Byte 3 Only
	↑	H	H	H	L	Write data inputs to Byte 3 Only
↑		L	L	L	L	Write data inputs to all Bytes
	↑	L	L	L	L	Write data inputs to all Bytes

5677 tbl 03a

NOTES:

1. $\overline{BW}0$ controls D[8:0], $\overline{BW}1$ controls D[17:9], $\overline{BW}2$ controls D[26:18], $\overline{BW}3$ controls D[35:27].
2. For this table: W is Low on the rising edge of K; E0 and E1 are true on the rising edge of $\overline{K}$. See Truth Tables I and III. Addresses for Writes are qualified on rising edge of $\overline{K}$.
3. This table represents a subset of the potential write scenarios based upon $\overline{BW}0$ - $\overline{BW}3$ inputs and is meant to illustrate basic device functionality.

Truth Table III - Port Enable Pins(1) Normal Read and Writes

Device Selected	EP[0]	EP[1]	E[0]	E[1]
Bank 0	VSS	VSS	L	L
Bank 1	VDD	VSS	H	L
Bank 2	VSS	VDD	L	H
Bank 3	VDD	VDD	H	H

5677 tbl05

NOTES:
1. EP [1:0] - Port Enable Programming Polarity (see pin description for the entire device).
2. Ex[1:0] - Port Enable (see pin description assigned for each port).

Cascade/Multi-Drop using Port Enable (E0 & E1) Pins

As shown below in Figure 1 upto four devices can be cascaded using the Port Enable (E0,E1) pins scheme. The port enable pins are subject to the same DC characteristics as the QDR interface. Refer to Pin Definitions table for pin descriptions. This diagram illustrates one port of a QDR-II dual port

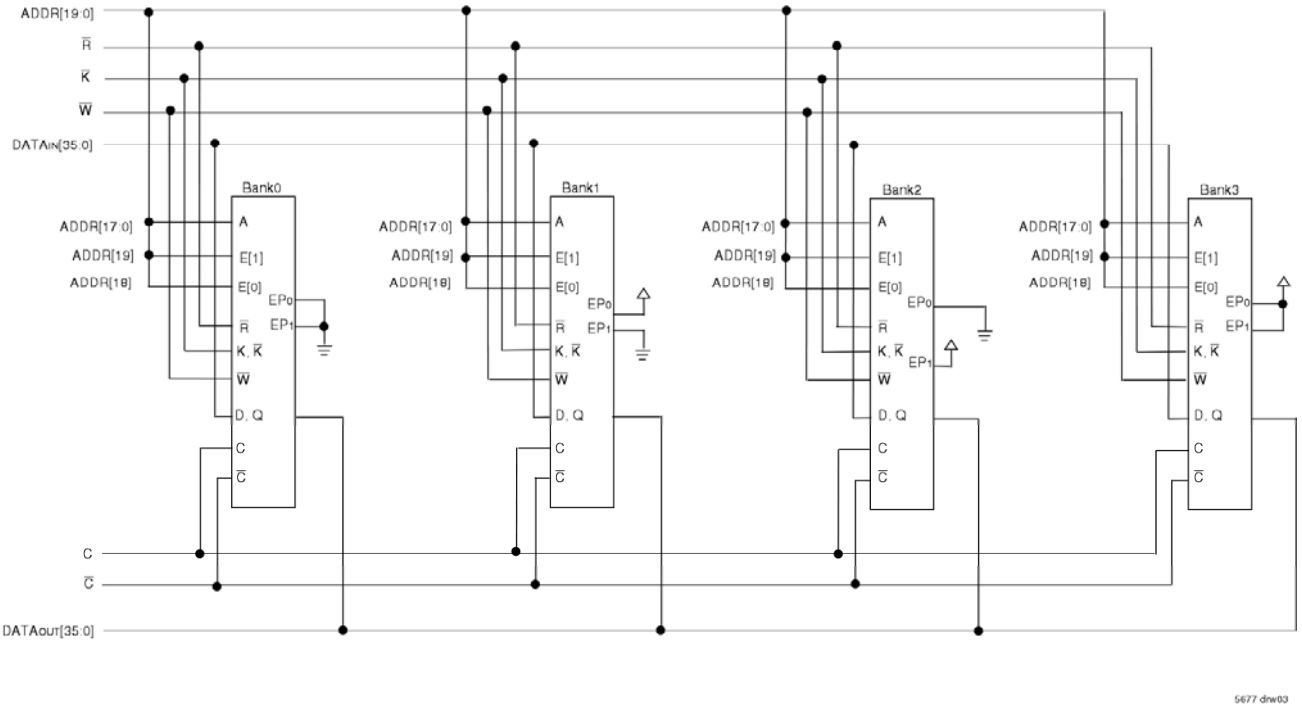


Figure 1. Multi-drop Cascading using the Chip Enable E[1:0] Pins

Absolute Maximum Ratings(1,2,3)

Symbol	Rating	Value	Unit
V_{DD}	Supply Voltage on V_{DD} with Respect to GND	–0.5 to +2.2	V
V_{DDQ}	Supply Voltage on V_{DDQ} with Respect to GND	–0.5 to V_{DD}	V
V_{TERM}	Voltage on Input, Output and I/O terminals with respect to GND	–0.3 to V_{DD}+0.3	V
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–65 to +150	°C
I_{OUT}	Continuous Current into Outputs	± 20	mA

5677 tbl 07

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{DDQ} must not exceed V_{DD} during normal operation.
3. VTerm(MAX) = minimum of V_{DD} +0.3V and 2.2V.

Thermal Resistance

Parameter	Symbol	Typ.	Unit
Junction to Ambient	θ_{JA}	12.5	°C/W
Junction to Case	θ_{JC}	0.1	°C/W

5677 tbl 10

NOTE:
1. Junction temperature is a function of on-chip power dissipation, package thermal impedance, mounting site temperature and mounting site thermal impedance. $T_J = T_A + P_D \times \theta_{JA}$.

Recommended Operating Temperature and Supply Voltage

Grade	Ambient Temperature	GND	V_{DD}
Commercial	0°C to +70°C	0V	1.8V ± 100mV
Industrial	-40°C to +85°C	0V	1.8V ± 100mV

5677 tbl06

Capacitance (T_A = +25°C, f = 1.0MHz)(1)

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	5	pF
C_O	Output Capacitance	V_{OUT} = 0V	7	pF

5677 tbl 08

NOTE:
1. Tested at characterization and retested after any design or process change that may affect these parameters.
2. V_{DD} = 1.8V, V_{DDQ} = 1.5V

Recommended DC Operating and Temperature Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Power Supply Voltage	1.7	1.8	1.9	V
V_{DDQ}	I/O Supply Voltage	1.4	1.5	1.9	V
V_{SS}	Ground	0	0	0	V
V_{REF}	Input Reference Voltage	0.68	$V_{DDQ/2}$	0.95	V
V_{IH}	Input High Voltage	V_{REF}+0.1	–	V_{DDQ}+0.3	V
V_{IL}	Input Low Voltage	–0.3	–	V_{REF}–0.1	V
T_A	Ambient Temperature(1)	0	25	+70	°C

5677 tbl 09

NOTE:
1. During production testing, the case temperature equals the ambient temperature.

DC Electrical Characteristics Over the Operating Temperature and Supply Voltage (V_{DD} = 1.8V ±100mV, V_{DDQ} = 1.4V to 1.9V, T_A = 0 to 70°C)

Parameter	Symbol	Test Conditions		Min	Max	Unit	Note
Input Leakage Current	I_{IL}	V_{DD} = Max V_{IN} = V_{SS} to V_{DDQ}		-10	+10	µA	8
Output Leakage Current	I_{OL}	Output Disabled		-10	+10	µA	8
Active Operating Current	I_{DD}	V_{DD} = Max, I_{OUT} = 0mA (outputs open), Cycle Time ≥ t_{KHKH} Min	250MHz	-	1636	mA	1
			233MHz	-	1542		
2 Port Read	I_{DD1}	V_{DD} = Max, I_{OUT} = 0mA (outputs open), Cycle Time ≥ t_{KHKH} Min	250MHz	-	1432	mA	1
			233MHz	-	1351		
2 Port Write	I_{DD2}	V_{DD} = Max, I_{OUT} = 0mA (outputs open), Cycle Time ≥ t_{KHKH} Min	250MHz	-	1212	mA	1
			233MHz	-	1147		
Standby Current	I_{SB}	Device Deselected I_{OUT} = 0mA (outputs open), f=Max, All Inputs ≤ 0.2V or > V_{DDQ} - 0.2V W_{EN}=R_{EN}=High	250MHz	-	1007	mA	2
			233MHz	-	956		
Output High Voltage	V_{OH1}	Z_Q = 250Ω, I_{OH} = -(V_{DDQ}/2)/(R_Q/5)		V_{DDQ}/2 -0.12	V_{DDQ}/2 +0.12	V	3,7
Output Low Voltage	V_{OL1}	Z_Q = 250Ω, I_{OL} = (V_{DDQ}/2)/(R_Q/5)		V_{DDQ}/2 -0.12	V_{DDQ}/2 +0.12	V	4,7
Output High Voltage	V_{OH2}	I_{OH} = -0.1mA		V_{DDQ} -0.2	V_{DDQ}	V	5
Output Low Voltage	V_{OL2}	I_{OL} = 0.1mA		V_{SS}	0.2	V	6
Output Impedance Control	| I_{OH} | | I_{OL} |	V_{OUT} = V_{DDQ}/2 V_{OUT} = V_{DDQ}/2		-(I_{OH}o-15%) (I_{OL}o-15%)	-(I_{OH}o+15%) (I_{OL}o+15%)	V	3 4

5677 tbl12

NOTES:

1. Operating Current is measured at 100% bus utilization on the active port.
2. Standby Current is only after all pending read and write burst operations are completed.
3. Outputs are impedance-controlled. I_{OHO} = (V_{DDQ}/2)/(R_Q/5) = @Vout = V_{DDQ}/2 and is guaranteed by device characterization for 175Ω ≤ Z_Q < 350Ω. This parameter is tes at Z_Q = 250Ω, which gives a nominal 50Ω output impedance.
4. Outputs are impedance-controlled. I_{OLO} = (V_{DDQ}/2)/(R_Q/5) = @Vout = V_{DDQ}/2 and is guaranteed by device characterization for 175Ω ≤ Z_Q < 350Ω. This parameter is tes at Z_Q = 250Ω, which gives a nominal 50Ω output impedance.
5. This measurement is taken to ensure that the output has the capability of pullling to the V_{DDQ} rail, and is not intended to be used as an impedance measurement point.
6. This measurement is taken to ensure that the output has the capability of pulling to V_{SS}, and is not intended to be used as an impedance measure point.
7. Programmable Impedance Mode.
8. ± 30µA for JTAG input pins.

Input Electrical Characteristics Over the Operating Temperature and Supply Voltage (V_{DD} = 1.8V ±100mV, V_{DDQ} = 1.4V to 1.9V, T_A = 0 to 70°C)

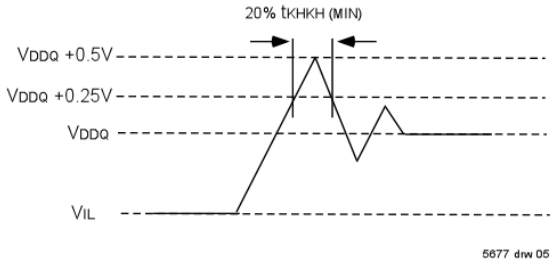
Parameter	Symbol	Min	Max	Unit	Notes
Input High Voltage, DC	$V_{IH\ (DC)}$	V_{REF} +0.1	V_{DDQ} +0.3	V	1,2
Input Low Voltage, DC	$V_{IL\ (DC)}$	-0.3	V_{REF} -0.1	V	1,3
Input High Voltage, AC	$V_{IH\ (AC)}$	V_{REF} +0.2	-	V	4,5
Input Low Voltage, AC	$V_{IL\ (AC)}$	-	V_{REF} -0.2	V	4,5

5677 tbl 13

NOTES:

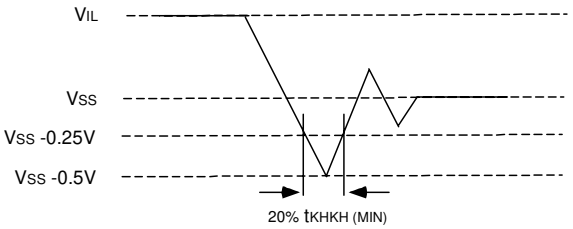
1. These are DC test criteria. DC design criteria is V_{REF} ± 50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max) DC = V_{DDQ} +0.3V, V_{IH} (Max) AC = V_{DDQ} +0.5V (pulse width ≤ 20% t_{KHKH} (min)).
3. V_{IL} (MIN) DC = -0.3V, V_{IL} (MIN) AC = -0.5V (pulse width ≤ 20% t_{KHKH} (min)).
4. This condition is for AC function test only, not for AC parameter test.
5. To maintain a valid level, the transitioning edge of the input must:
   Sustain a constant slew rate from the current AC level through the target AC level, V_{IL} (AC) or V_{IH} (AC)
   Reach at least the target AC level
   After the AC target level is reached, continue to maintain at least the target DC level, V_{IL} (DC) or V_{IH} (DC)

Overshoot Timing



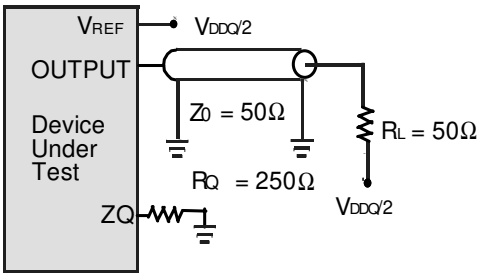
5677 drw 05

Undershoot Timing



5677 drw 06

AC Test Loads



5677 drw 07

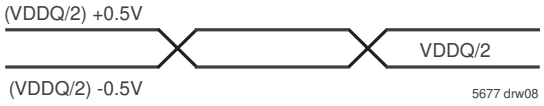
AC Test Conditions

Parameter	Symbol	Value	Unit
Core Power Supply Voltage	VDD	1.7-1.9	V
Output Power Supply Voltage	VDDQ	1.4-1.9	V
Input High Level	VIH	(VDDQ/2) +0.5	V
Input Low Level	VIL	(VDDQ/2) -0.5	V
Input Reference Level	VREF	VDDQ/2	V
Input Rise/Fall Time	TR/TF	0.3/0.3	ns
Output Timing Reference Level		VDDQ/2	V

5677 tbl 14

NOTE:

1. Parameters are tested with RQ=250Ω.



5677 drw08

AC Electrical Characteristics

(V_{DD} = 1.8V ±100mV, V_{DDQ} = 1.4V to 1.9V, T_A[8] = 0 to 70°C)

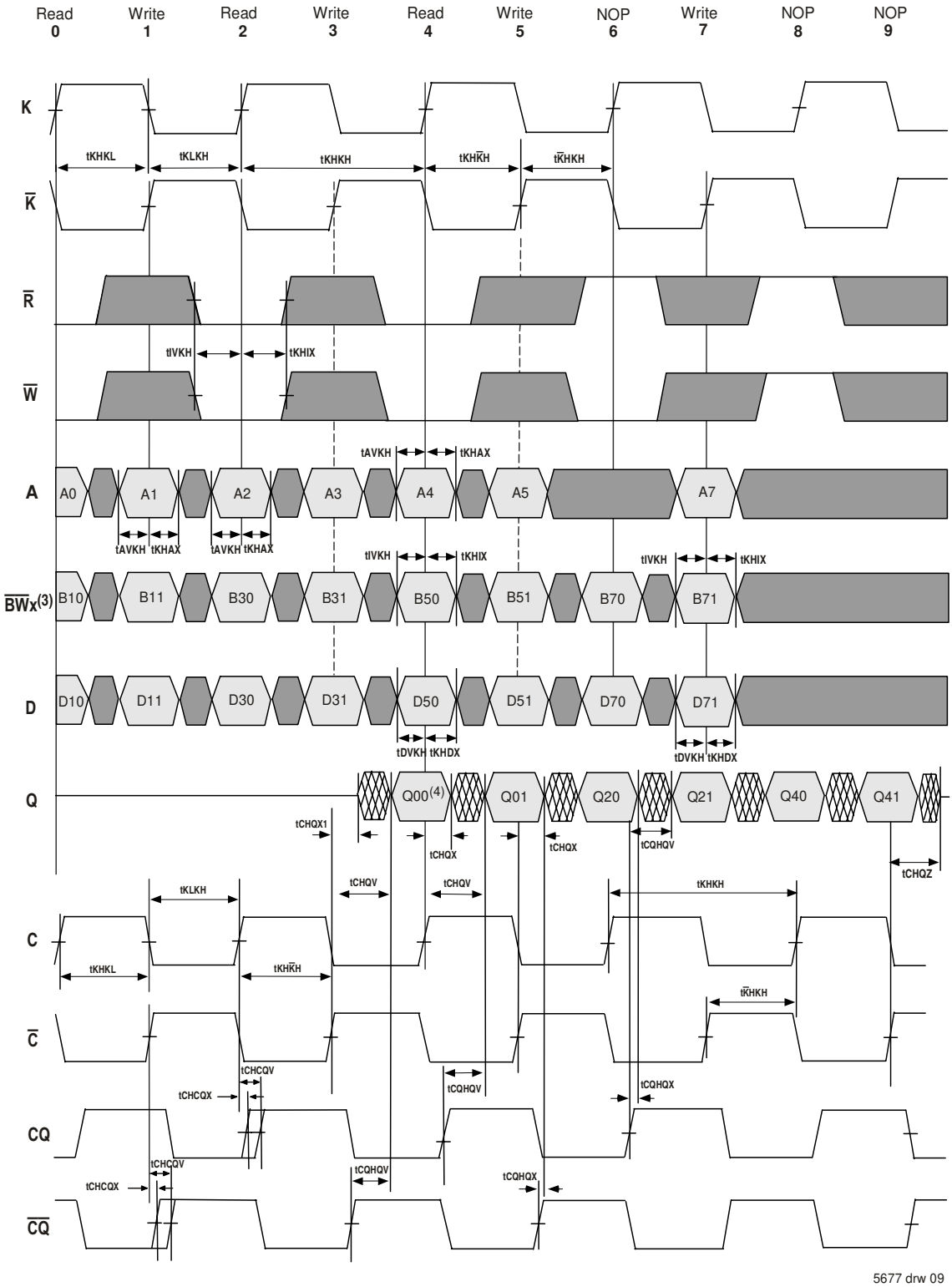
		Commercial					
		250MHz		233MHz			
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit	Notes
Clock Parameters							
t_{KHKH}	Average clock cycle time (K,$\overline{K}$,C,$\overline{C}$)	4.00	6.30	4.30	7.20	ns	
$t_{KC\ var}$	Clock Phase Jitter (K,$\overline{K}$,C,$\overline{C}$)	—	0.20	—	0.20	ns	1,5
t_{KHKL}	Clock High Time (K,$\overline{K}$,C,$\overline{C}$)	1.60	—	1.80	—	ns	9
t_{KLKH}	Clock LOW Time (K,$\overline{K}$,C,$\overline{C}$)	1.60	—	1.80	—	ns	9
$t_{KH\overline{K}H}$	Clock to $\overline{clock}$ (K→$\overline{K}$,C→$\overline{C}$)	1.80	—	2.00	—	ns	10
$t_{\overline{K}HKH}$	$\overline{Clock}$ to clock ($\overline{K}$→K,$\overline{C}$→C)	1.80	—	2.00	—	ns	10
t_{KHCH}	Clock to data clock (K→C,$\overline{K}$→$\overline{C}$)	0.00	1.80	0.00	2.00	ns	
$t_{KC\ lock}$	DLL lock time (K, C)	1024	—	1024	—	cycles	2
$t_{KC\ reset}$	K static to DLL reset	30	—	30	—	ns	
Output Parameters							
t_{CHQV}	C,$\overline{C}$ HIGH to output valid	—	0.45	—	0.45	ns	3
t_{CHQX}	C,$\overline{C}$ HIGH to output hold	-0.45	—	-0.45	—	ns	3
t_{CHCQV}	C,$\overline{C}$ HIGH to echo clock valid	—	0.45	—	0.45	ns	3
t_{CHCQX}	C,$\overline{C}$ HIGH to echo clock hold	-0.45	—	-0.45	—	ns	3
t_{CQHQV}	CQ,$\overline{CQ}$ HIGH to output valid	—	0.30	—	0.32	ns	
t_{CQHQX}	CQ,$\overline{CQ}$ HIGH to output hold	-0.30	—	-0.32	—	ns	
t_{CHQZ}	C HIGH to output High-Z	—	0.45	—	0.45	ns	3,4,5
t_{CHQX1}	C HIGH to output Low-Z	-0.45	—	-0.45	—	ns	3,4,5
Set-Up Times							
t_{AVKH}	Address valid to K,$\overline{K}$ rising edge	0.35	—	0.37	—	ns	6
t_{IVKH}	Control inputs valid to K,$\overline{K}$ rising edge	0.35	—	0.37	—	ns	7
t_{DVKH}	Date-in valid to K, $\overline{K}$ rising edge	0.35	—	0.37	—	ns	
Hold Times							
t_{KHAX}	K,$\overline{K}$ rising edge to address hold	0.35	—	0.37	—	ns	6
t_{KHIX}	K,$\overline{K}$ rising edge to control inputs hold	0.35	—	0.37	—	ns	7
t_{KHDX}	K,$\overline{K}$ rising edge to data-in hold	0.35	—	0.37	—	ns	
Port-to-Port Delay							
t_{CO}	Clock-to-Clock Offset	4.00	—	4.30	—	ns	

5677 tbl 15

NOTES:

1. Cycle to cycle period jitter is the variance from clock rising edge to the next expected clock rising edge, as defined per JEDEC Standard No. 65 (EIA/JESD65) page.
2. V_{DD} slew rate must be less than 0.1V DC per 50ns for DLL lock retention. DLL lock time begins once V_{DD}, V_{DDQ} and input clock are stable.
3. If C, $\overline{C}$ are tied High, K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters.
4. To avoid bus contention, at a given voltage and temperature t_{CHQX1} is bigger than t_{CHQZ}.
   The specs as shown do not imply bus contention because t_{CHQX1} is a MIN parameter that is worst case at 0°C and 1.9V t_{CHQZ}, is a MAX parameter that is worst case at 70°C and 1.7V.
5. This parameter is guaranteed by device characterization, but not production tested.
6. All address inputs must meet the specified setup and hold times for all latching clock edges.
7. Control signals are $\overline{R}$, $\overline{W}$, $\overline{BW_0}$, $\overline{BW_1}$, $\overline{BW_2}$, $\overline{BW_3}$,E_0, E_1.
8. During production testing, the case temperature equals T_A.
9. Clock High Time (t_{KHKL}) and Clock Low Time (t_{KLKH}) should be within 40% to 60%of the cycle time (t_{KHKH}).
10. Clock to $\overline{Clock}$ time ($t_{KH\overline{K}H}$) and $\overline{Clock}$ to Clock time ($t_{\overline{K}HKH}$) should be within 45% to 55% of the cycle time (t_{KHKH}).

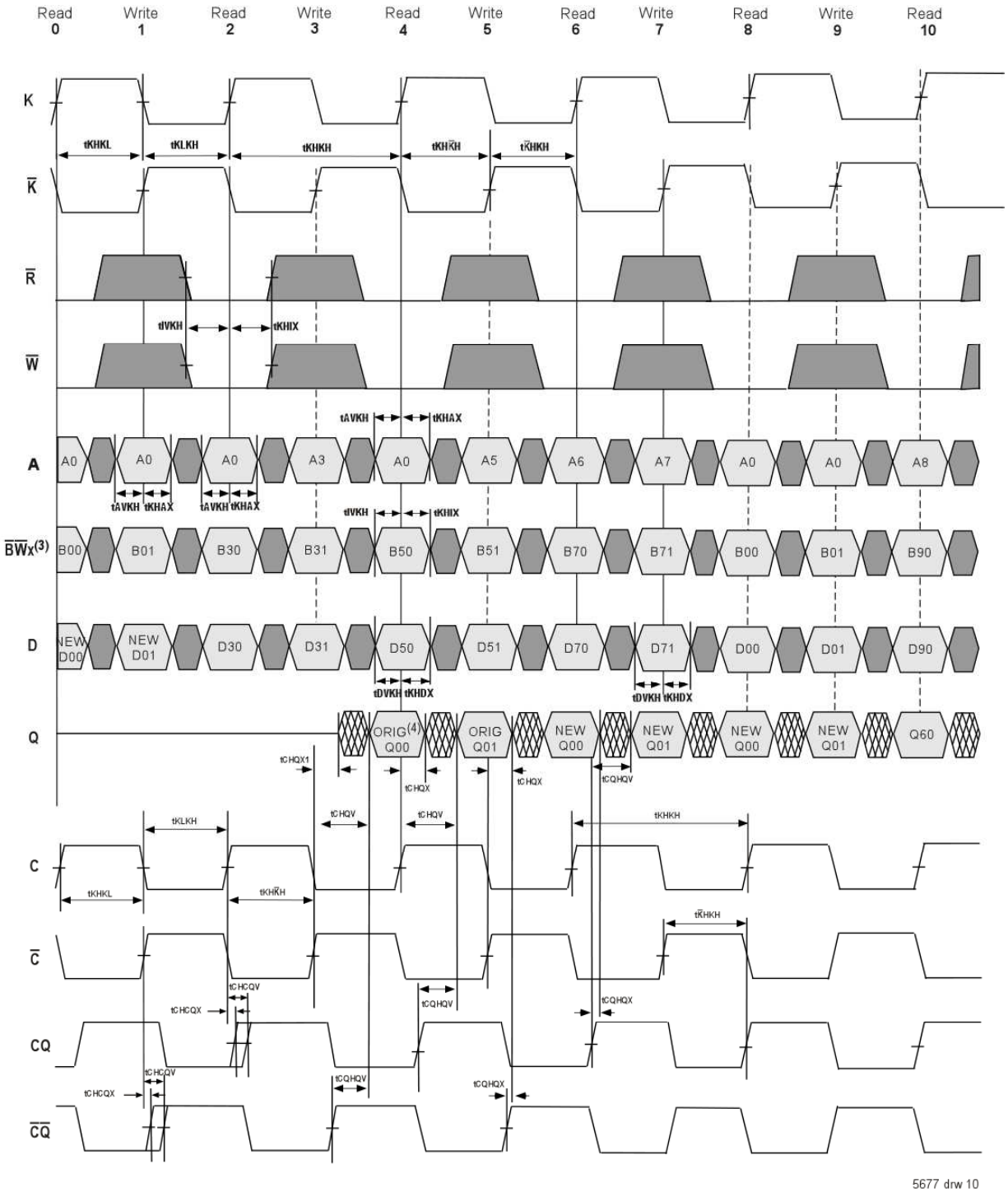
Timing Waveform for Alternating Read and Write Operations(1,2)



NOTES:

1. Device is selected per E[0] and E[1] as defined in Truth Table II, and $\overline{MRST}$ = V_{IH}.
2. This waveform represents operation when DLL is ON.
3. To perform a valid write operation, both $\overline{W}$ and the appropriate $\overline{BW}$0-3 must be low.
4. Q_{00} refers to the output from A_0, and Q_{01} refers to the output from the next internal address following A_0.

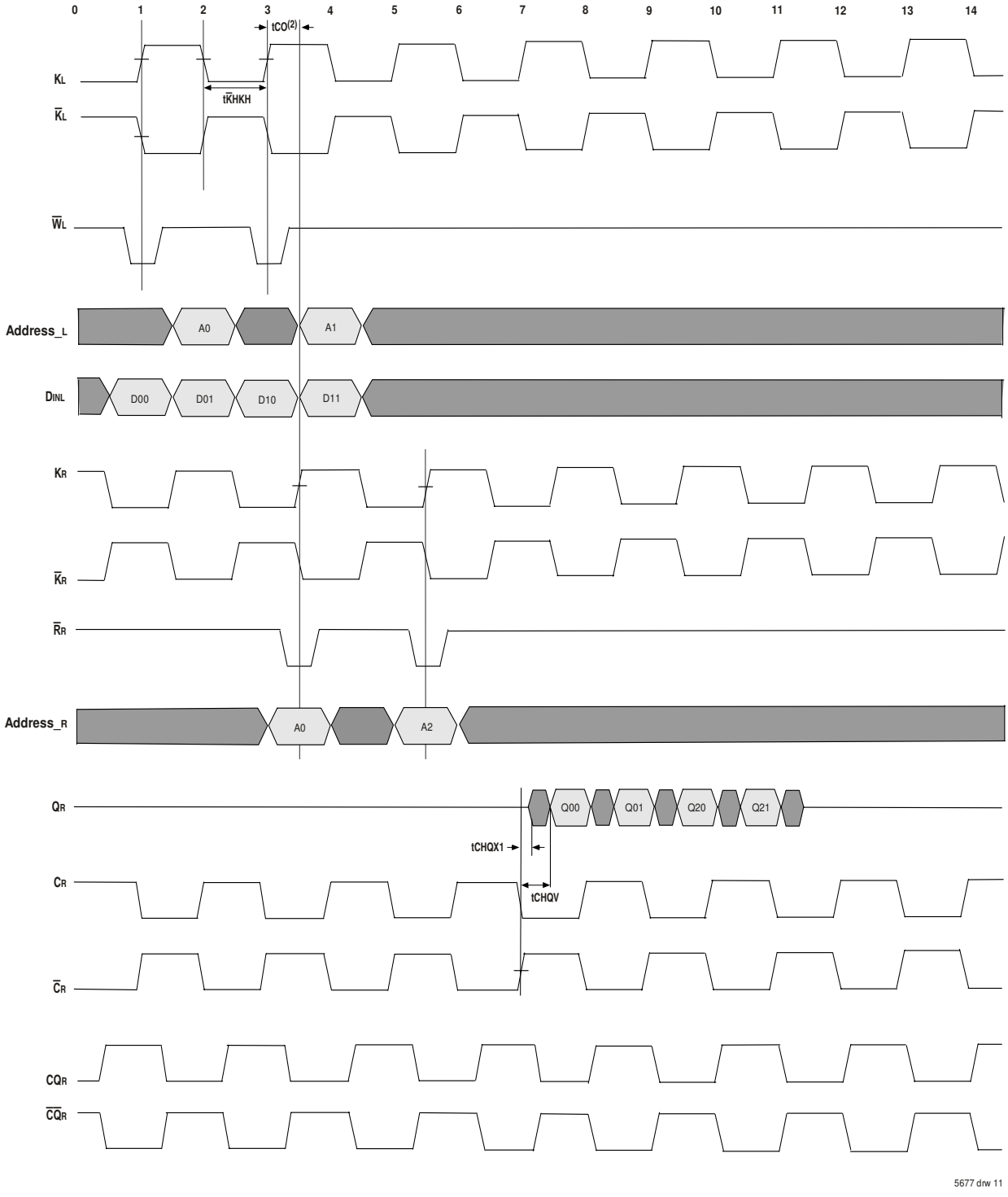
Timing Waveform of Back-to-Back Read-Write-Read to Same Address(1,2)



NOTES:

1. Device is selected per E[0] and E[1] as defined in Truth Table II, and $\overline{MRST}$ = VIH.
2. This waveform represents operation when DLL is ON.
3. To perform a valid write operation, both $\overline{W}$ and the appropriate $\overline{BW}$0-3 must be low.
4. ORIG Q_{00} represents the existing data in the memory. New Q_{00} represents the data written into the memory in the first cycle of the waveform.

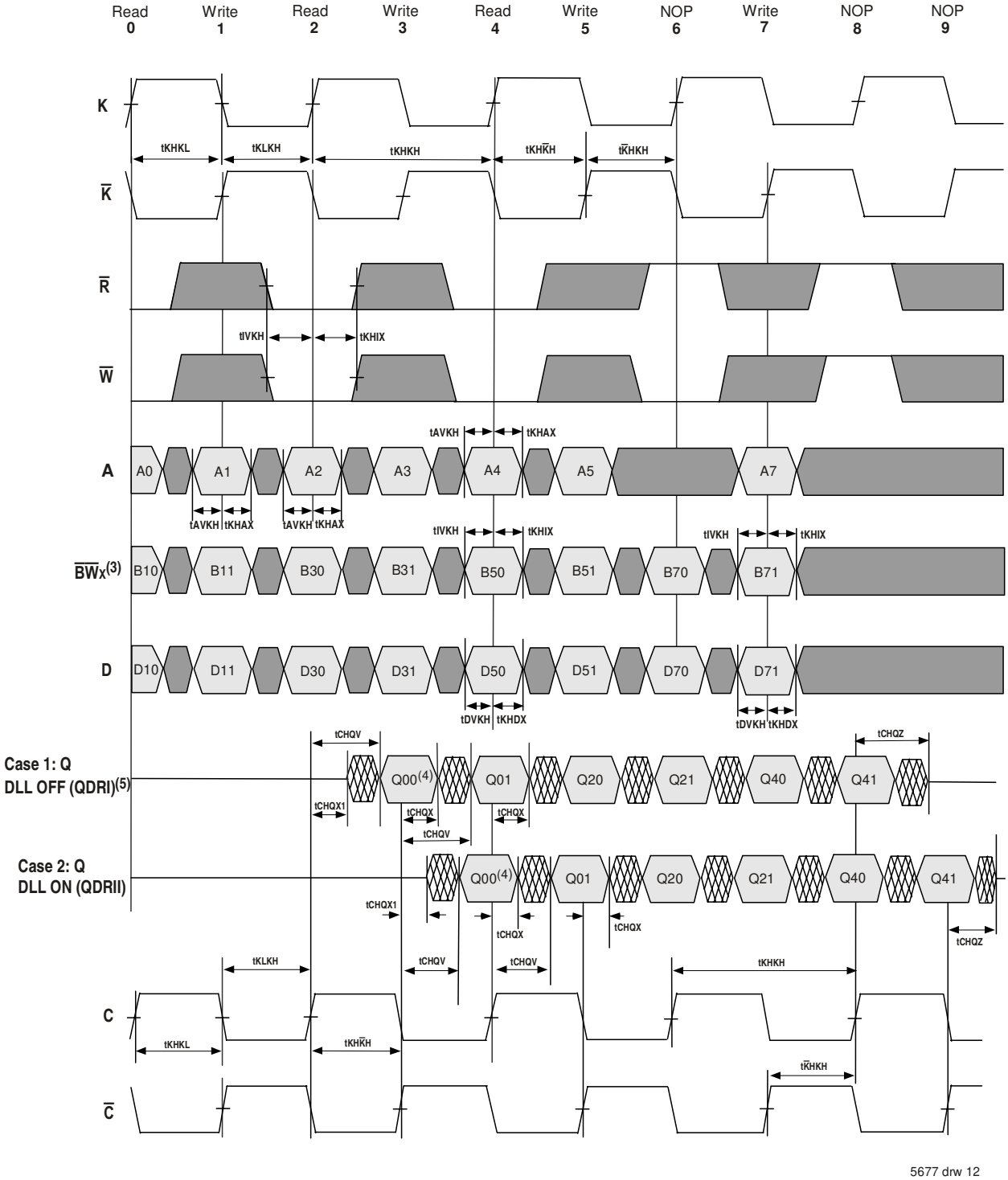
Timing Waveform for Left Port Write to Right Port Read(1)



NOTES:

1. Device is selected per E[0] and E[1] as defined inTruth Table III. $\overline{MRST}$ = VIH. $\overline{BW}$0L, $\overline{BW}$1L, $\overline{BW}$2L, and $\overline{BW}$3L = VIL
2. If tco < specified minimum, data read from right port is not valid until the next KR cycle. If tco ≥ specified minimum, data read from right port is available on the first KR cycle as shown.

Timing Waveforms for DLL Operation (On/Off)(1,2)

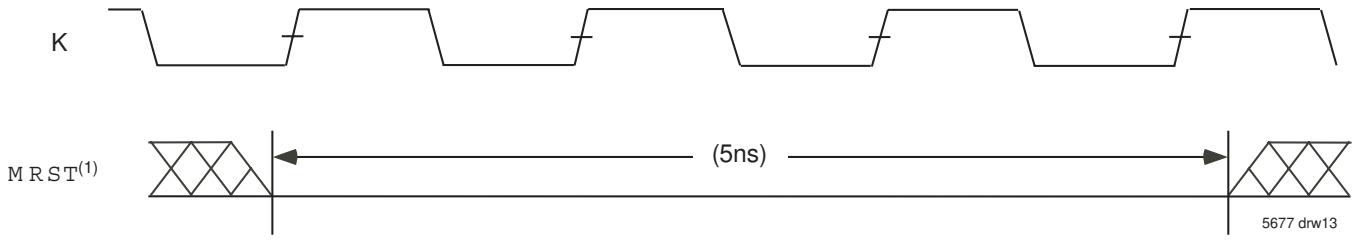


5677 drw 12

NOTES:

1. Device is selected per E[0] and E[1] as defined in Truth Table II, and $\overline{MRST}$ = VIH.
2. With DLL OFF ($\overline{D}_{OFFX} \leq V_{IL}$) device behaves as a QDRI device. With DLL ON ($\overline{D}_{OFFX} \geq V_{IH}$) device behaves as a QDR-II device.
3. To perform a valid write operation, both $\overline{W}$ and the appropriate $\overline{BW}$0-3 must be low on the rising edge of $\overline{K}$.
4. Q_{00} refers to the output from A_0, and Q_{01} refers to the output from the next internal address following A_0.
5. With DLL off ($\overline{D}_{OFF}$ = VIL) the propagation delays will be increased and the AC timing parameters will be different values from those specified in this data sheet.

Master Reset Timing Waveform



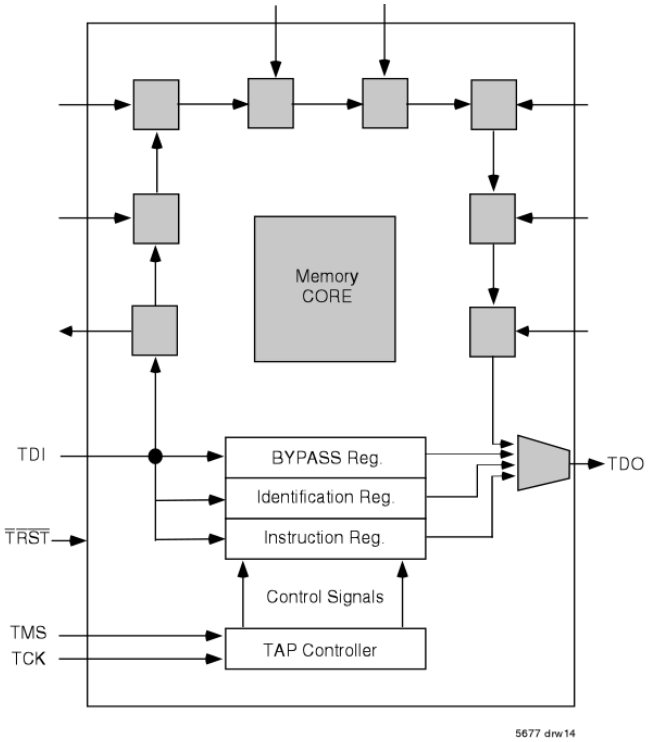
NOTE:

1. $\overline{\text{MRST}}$ must be held LOW for a minimum of (5ns) after power supply is stable.

IEEE 1149.1 Test Access Port and Boundary SCAN-JTAG

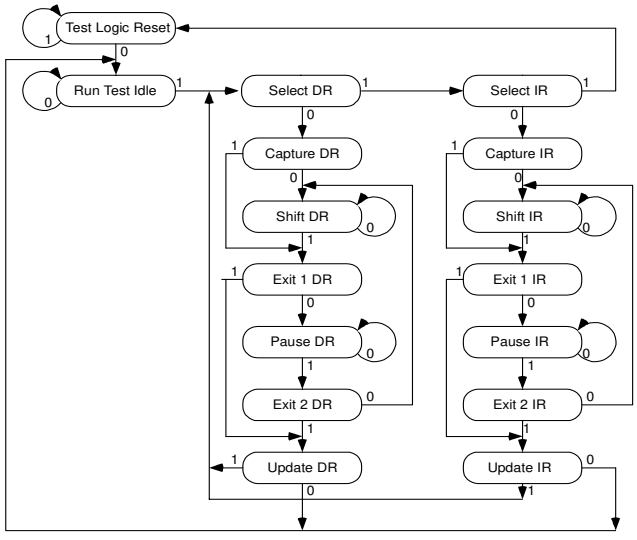
This part contains an IEEE standard 1149.1 Compatible Test Access Port (TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. In conformance with IEEE 1149.1, the QDR-II Dual-Port Static RAM contains a TAP controller, Instruction Register, Bypass Register and ID Register. The TAP controller has a standard 16-state machine that resets internally upon power-up. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the QDR-II Dual-Port Static RAM TCK must be tied to Vss to preclude a mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected, but they may also be tied to Vdd through a resistor. TDO should be left unconnected.

JTAG Block Diagram



5677 drw14

TAP Controller State Diagram



5677 drw 15

Identification Register Definitions

Instruction Field	Value	Description
Revision Number (31:28)	0x0	Reserved for version number
IDT Device ID (27:12)	0x355(1)	Defines IDT part number (IDT70P3537)
IDT JEDEC ID (11:1)	0x33	Allows unique identification of device vendor as IDT
ID Register Indicator Bit (Bit 0)	1	Indicates the presence of an ID register

5677 tbl 16

NOTE:
1. Device ID for IDT70P3517 is 0x356.

Scan Register Sizes

Register Name	Bit Size
Instruction (IR)	4
Bypass (BYR)	1
Identification (IDR)	32
Boundary Scan (BSR)	Note 1

5677 tbl 17

NOTE:
1. The Boundary Scan Descriptive Language (BSDL) file for this device is available on the IDT website (www.idt.com), or by contacting your local IDT sales representative.

System Interface Parameters

Instruction	Code	Description
EXTEST	0000	Forces contents of the boundary scan cells onto the device outputs(1). Places the boundary scan register (BSR) between TDI and TDO.
BYPASS	1111	Places the bypass register (BYR) between TDI and TDO.
IDCODE	0010	Loads the ID register (IDR) with the vendor ID code and places the register between TDI and TDO.
HIGHZ	0100	Places the bypass register (BYR) between TDI and TDO. Forces all device output drivers to a High-Z state except $\overline{COL}$x & $\overline{INT}$x outputs.
CLAMP	0011	Uses BYR. Forces contents of the boundary scan cells onto the device outputs. Places the bypass register (BYR) between TDI and TDO.
SAMPLE/PRELOAD	0001	Places the boundary scan register (BSR) between TDI and TDO. SAMPLE allows data from device inputs(2) to be captured in the boundary scan cells and shifted serially through TDO. PRELOAD allows data to be input serially into the boundary scan cells via the TDI.
RESERVED	0101, 0111, 1000, 1001, 1010, 1011, 1100	Several combinations are reserved. Do not use codes other than those identified above.
PRIVATE	0110,1110,1101	For internal use only.

5677 tbl 18

NOTES:
1. Device outputs = All device outputs except TDO.
2. Device inputs = All device inputs except TDI, TMS, and $\overline{TRST}$.

JTAG DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage (I/P + O/P)	V_{DD}	1.7	1.8	1.9	V	
Input High Level	V_{IH}	1.3	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.5	V	
Output High Voltage (I_{OH} = -1mA)	V_{OH}	V_{DD} - 0.2	-	V_{DD}	V	
Output Low Voltage (I_{OL} = 1mA)	V_{OL}	V_{SS}	-	0.2	V	

5677 tbl 19

JTAG AC Test Conditions

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.8/0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		$V_{DD}/2$	V	1

NOTE:

5677 tbl 20

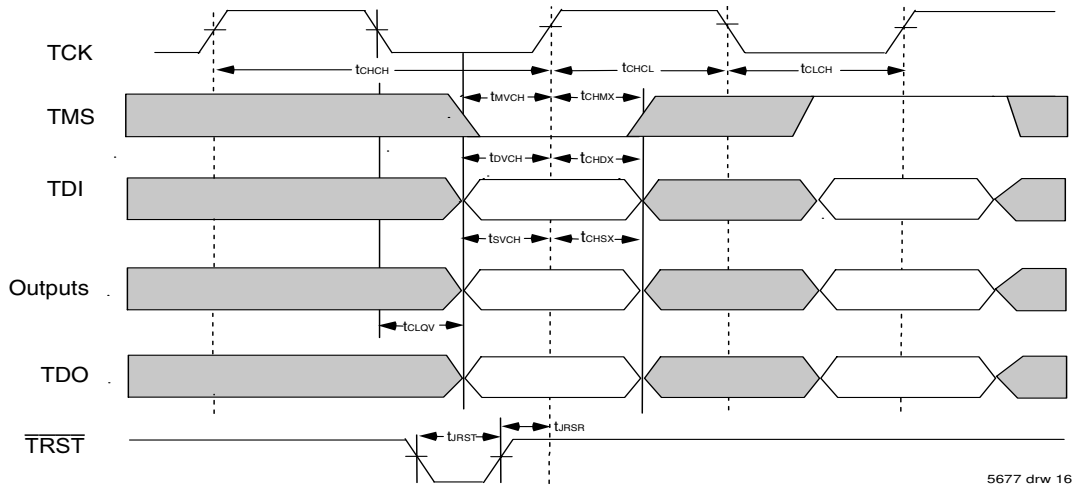
1. For outputs see AC test loads on page 10.

JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	100	-	ns	
TCK High Pulse Width	t_{CHCL}	40	-	ns	
TCK Low Pulse Width	t_{CLCH}	40	-	ns	
TMS Input Setup Time	t_{MVCH}	10	-	ns	
TMS Input Hold Time	t_{CHMX}	10	-	ns	
TDI Input Setup Time	t_{DVCH}	10	-	ns	
TDI Input Hold Time	t_{CHDX}	10	-	ns	
Input Setup Time	t_{SVCH}	10	-	ns	
Input Hold Time	t_{CHSX}	10	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	20	ns	
$\overline{TRST}$ Low to Reset JTAG	t_{JRST}	50	-	ns	
$\overline{TRST}$ High to TCK HIGH	t_{JRSR}	50	-	ns	

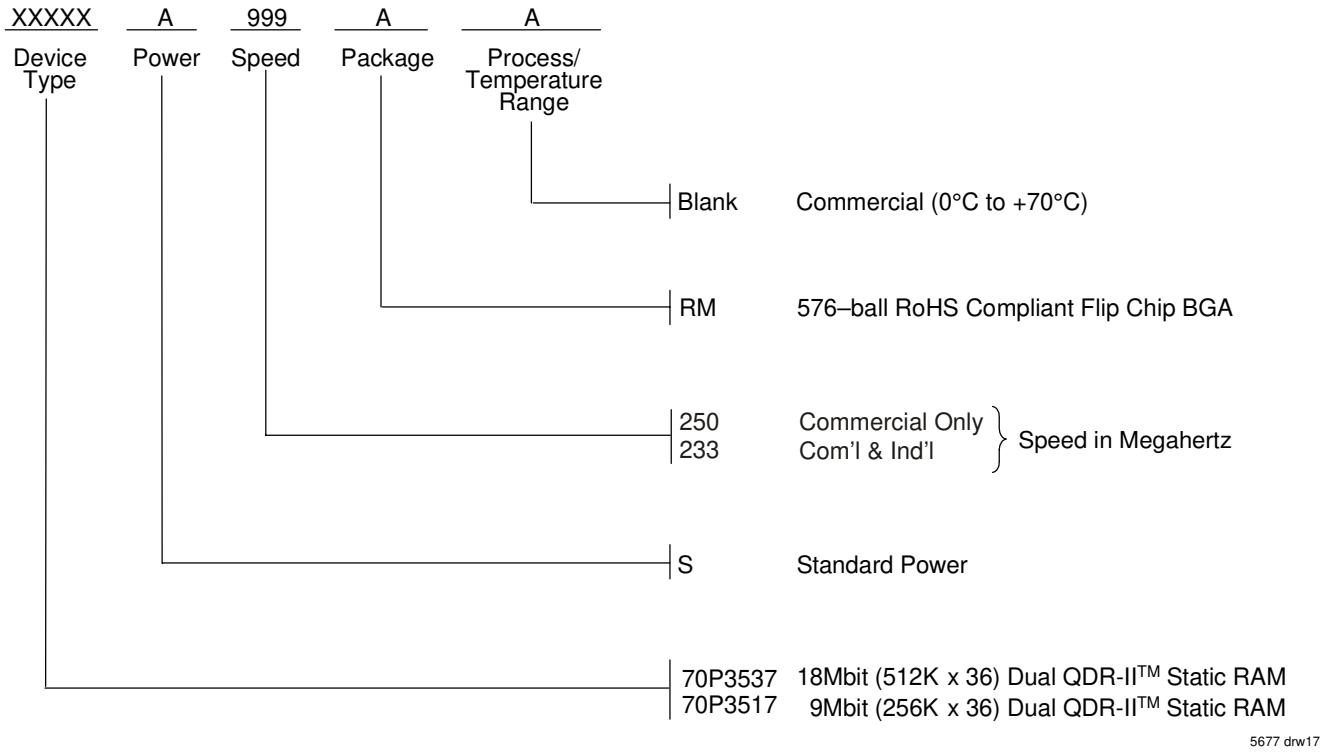
5677 tbl 21

JTAG Timing Diagram



5677 drw 16

Ordering Information



Preliminary Datasheet: Description

"PRELIMINARY" datasheets contain descriptions for products that are in early release.

Datasheet Document History

7/11/2007: Initial release of Preliminary Datasheet
8/05/2008: Page 9 Corrected a typo in DC Chars table
01/19/09: Page 20 Removed "IDT" from orderable part number

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