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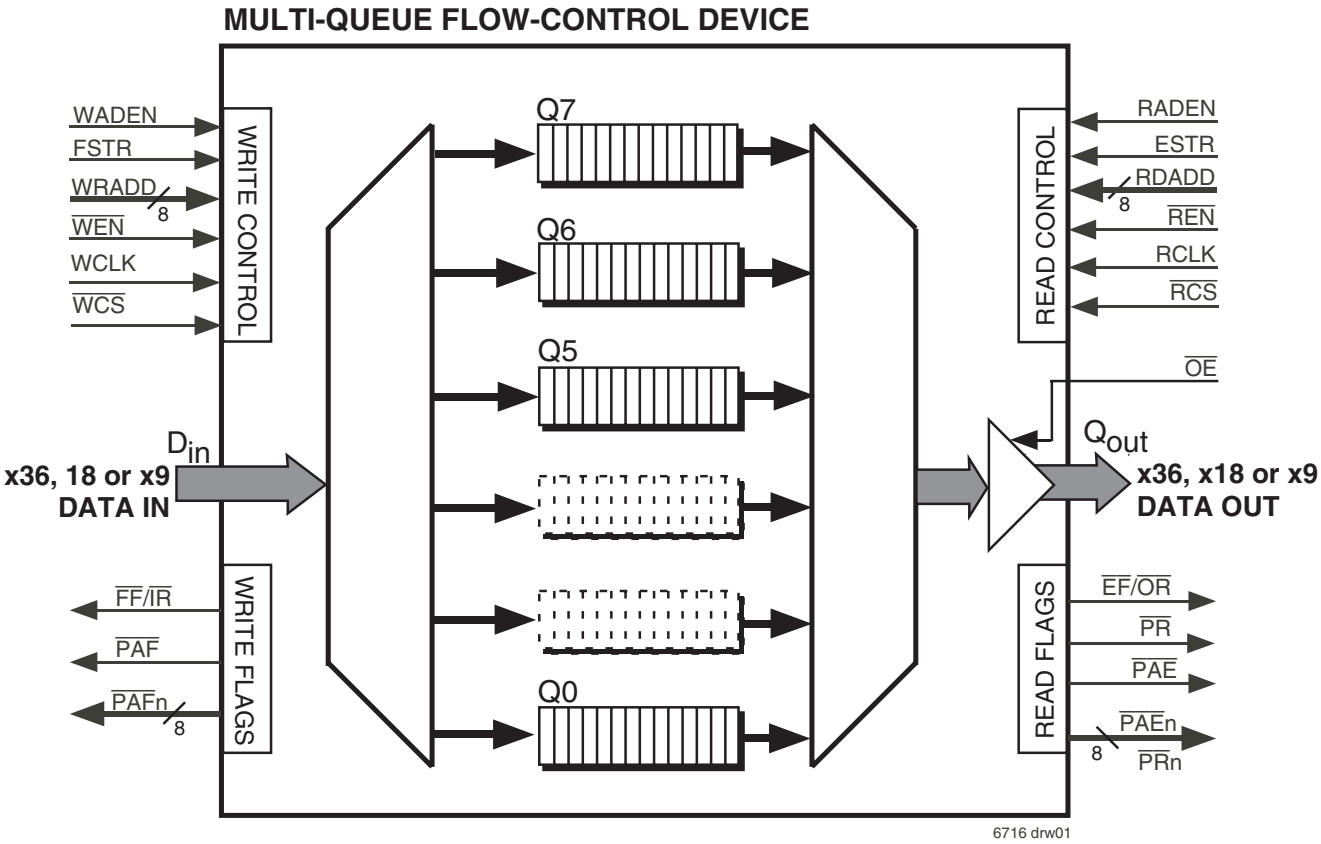
1.8V MULTI-QUEUE FLOW-CONTROL DEVICES (8 QUEUES) 36 BIT WIDE CONFIGURATION

589,824 bits — *IDT72P51339*
1,179,648 bits — *IDT72P51349*
2,359,296 bits — *IDT72P51359*
4,718,592 bits — *IDT72P51369*

FEATURES

- Choose from among the following memory density options:
  - IDT72P51339 — Total Available Memory = 589,824 bits
  - IDT72P51349 — Total Available Memory = 1,179,648 bits
  - IDT72P51359 — Total Available Memory = 2,359,296 bits
  - IDT72P51369 — Total Available Memory = 4,718,592 bits
- Configurable from 1 to 8 Queues
- Default configuration of 8 or 4 symmetrical queues
- Default multi-queue device configurations
  - *IDT72P51339: 2,048 x 36 x 8Q*
  - *IDT72P51349: 4,096 x 36 x 8Q*
  - *IDT72P51359: 8,192 x 36 x 8Q*
  - *IDT72P51369: 16,384 x 36 x 8Q*
- Default configuration can be augmented via the queue address bus
- Number of queues and individual queue sizes may be configured at master reset though serial programming
- 200 MHz High speed operation (5ns cycle time)
- 3.6ns access time
- Independent Read and Write access per queue
- User Selectable Bus Matching Options:
  - *x36 in to x36 out*
  - *x36in to x18out*
  - *x36in to x9out*
  - *x18 in to x36 out*
  - *x18 in to x18 out*
  - *x18 in to x9 out*
  - *x9 in to x36 out*
  - *x9 in to x18 out*
  - *x9 in to x9 out*
- User selectable I/O: 1.5V HSTL, 1.8V eHSTL, or 2.5V LVTTL
- 100% Bus Utilization, Read and Write on every clock cycle
- Selectable First Word Fall Through (FWFT) or IDT standard mode of operation
- Ability to operate on packet or word boundaries
- Mark and Re-Write operation
- Mark and Re-Read operation
- Individual, Active queue flags ($\overline{OR}$ / $\overline{EF}$, $\overline{IR}$ / $\overline{FF}$, $\overline{PAE}$, $\overline{PAF}$, $\overline{PR}$)
- 8 bit parallel flag status on both read and write ports
- Direct or polled operation of flag status bus
- Expansion of up to 64 queues and/or 32Mb logical configuration using up to 8 multi-queue devices in parallel
- JTAG Functionality (Boundary Scan)
- Available in a 256-pin PBGA, 1mm pitch, 17mm x 17mm
- HIGH Performance submicron CMOS technology
- Industrial temperature range (-40°C to +85°C) is available
- Green parts available, see Ordering Information

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION

The IDT72P51339/72P51349/72P51359/72P51369 multi-queue flow-control devices are single chips with up to 32 discrete configurable FIFO queues. All queues within the device have a common data input bus, (write port) and a common data output bus, (read port). Data written into the write port is directed to a specific queue via an internal de-multiplex operation, addressed by the write address bus (WRADD). Data read from the read port is accessed from a specific queue via an internal multiplex operation, addressed by the read address bus (RDADD). Data writes and reads can be performed at high speeds up to 200MHz, with access times of 3.6ns. Data write and read operations are totally independent of each other, a queue maybe selected on the write port and a different queue on the read port or both ports may select the same queue simultaneously.

The device provides Full flag and Empty flag status for the queue selected for write and read operations respectively. Also a Programmable Almost Full and Programmable Almost Empty flag for each queue is provided. Two 8 bit programmable flag busses are available, providing status of queues not selected for write or read operations. When 8 or less queues are configured in the device these flag busses provide an individual flag per queue, when more than 8 queues are used, either a Polled or Direct mode bus operation provides the flag busses with all queues status.

Bus Matching is available on this device, either port can be 9 bits, 18 bits or 36 bits wide. When Bus Matching is used the device ensures the logical transfer of data throughput in a Little Endian manner.

A packet mode of operation is also provided. Packet mode provides a packet ready flag output ($\overline{PR}$) indicating when at least one (or more) packets of data within a queue is available for reading. The Packet Ready indicator is generated upon detection of the start and end of packet demarcation bits. The multi-queue device then provides the user with an internally generated packet ready status per queue.

The user has full flexibility configuring queues within the device, being able to program the total number of queues between 1 and 32, the individual queue depths being independent of each other. The programmable flag positions are also user programmable. All programming is done via a dedicated serial port. If the user does not wish to program the multi-queue device, a default option is available that configures the device in a predetermined manner.

A Master Reset must be provided to the device. A Master Reset latches in configuration/setup pins and must be performed before further programming of the device can take place. On the rising edge of master reset the device operating mode is set, the device programming mode (serial, parallel or default) is set and the expansion configuration device type (master or slave) is set.

The multi-queue flow-control device has the capability of operating its I/O in either 2.5V LVTTL, 1.5V HSTL or 1.8V eHSTL mode. The type of I/O is selected via the IOSEL input. The core supply voltage (V_{DD}) to the multi-queue is 1.8V, however the output levels can be set independently via a separate supply, V_{DDQ}.

A JTAG test port is provided, here the multi-queue flow-control device has a fully functional Boundary Scan feature, compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

See Figure 1, *Multi-Queue Flow-Control Device Block Diagram* for an outline of the functional blocks within the device.

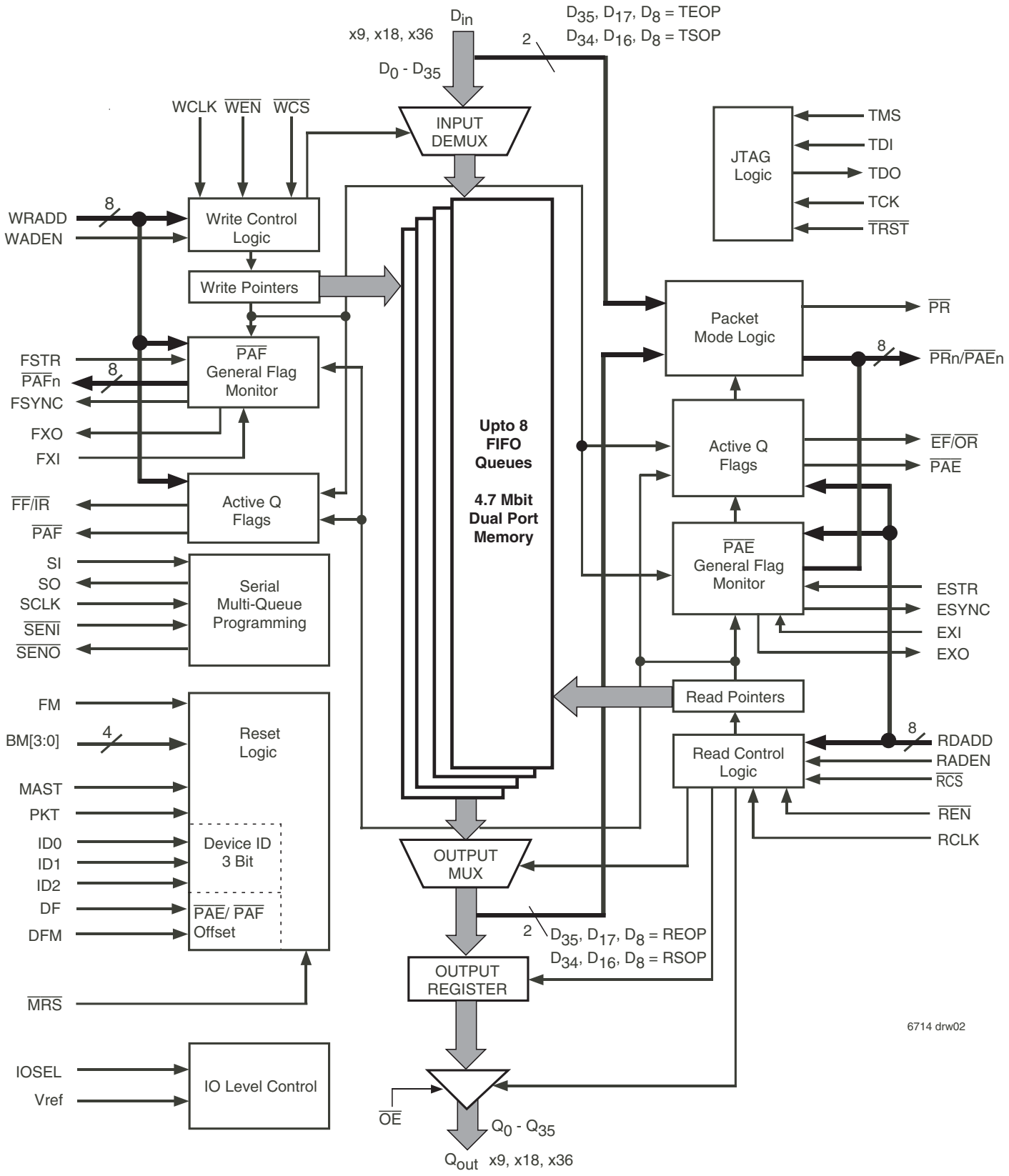
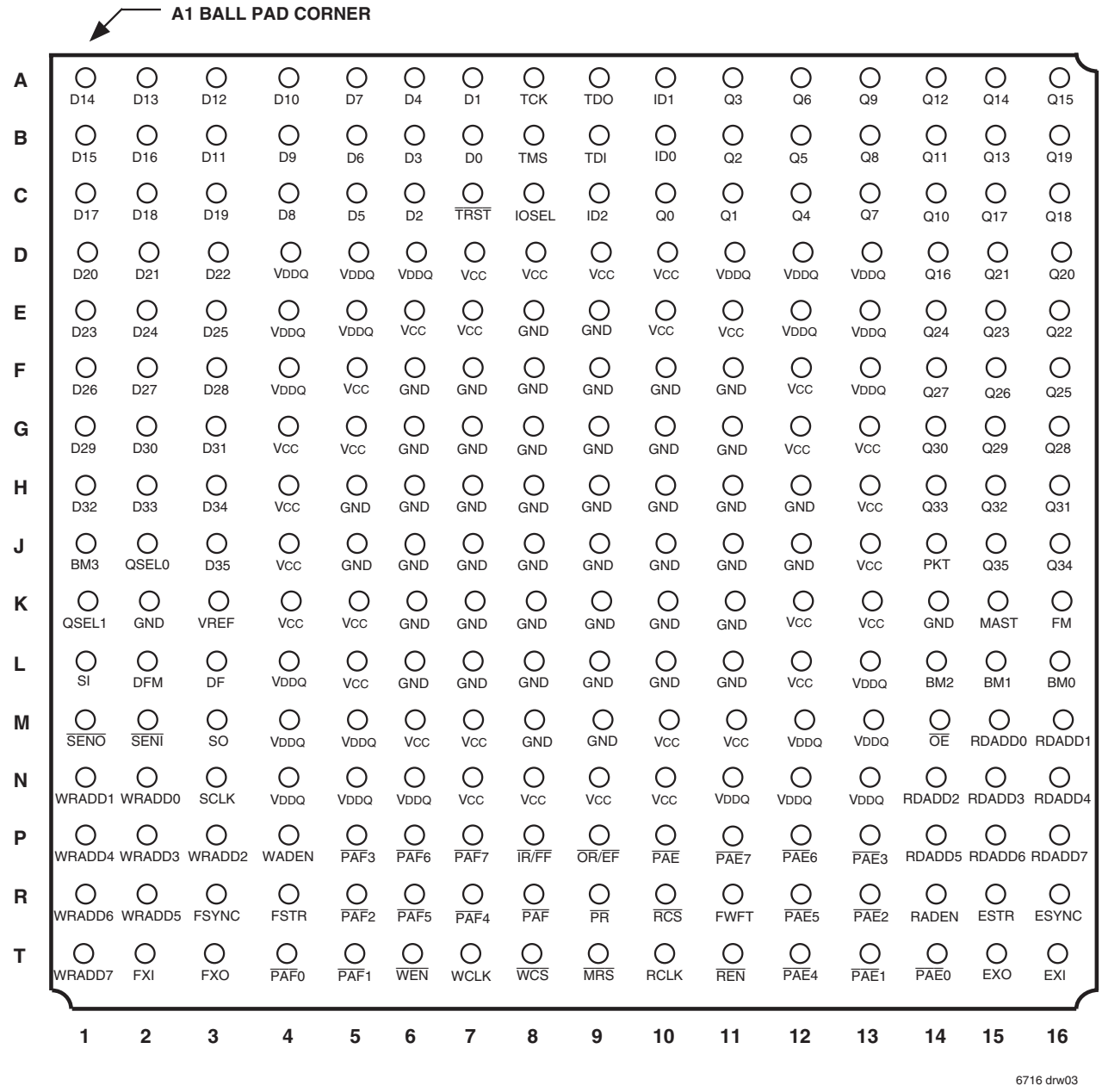


Figure 1. Multi-Queue Flow-Control Device Block Diagram

PIN CONFIGURATION



6716 drw03

PBGA (BB256-1, order code: BB)
TOP VIEW

DETAILED DESCRIPTION

MULTI-QUEUE STRUCTURE

The IDT multi-queue flow-control device has a single data input port and single data output port with up to 32 FIFO queues in parallel buffering between the two ports. The user can setup between 1 and 8 queues within the device. These queues can be configured to utilize the total available memory, providing the user with full flexibility and ability to configure the queues to be various depths, independent of one another.

MEMORY ORGANIZATION/ ALLOCATION

The memory is organized into what is known as "blocks", each block being 256 x36 bits. When the user is configuring the number of queues and individual queue sizes the user must allocate the memory to respective queues, in units of blocks, that is, a single queue can be made up from 0 to m blocks, where m is the total number of blocks available within a device. Also the total size of any given queue must be in increments of 256 x36. For the IDT72P51339, IDT72P51349, IDT72P71759 and IDT72P51369 the Total Available Memory is 128, 256, and 512 blocks respectively (a block being 256 x36). Queues can be built from these blocks to make any size queue desired and any number of queues desired.

BUS WIDTHS

The input port is common to all queues within the device, as is the output port. The device provides the user with Bus Matching options such that the input port and output port can be either x9, x18 or x36 bits wide, the read and write port widths can be set independently of one another. Because a ports are common to all queues the width of the queues is not individually set. The input width of all queues are the same and the output width of all queues are the same.

WRITING TO AND READING FROM THE MULTI-QUEUE

Data being written into the device via the input port is directed to a discrete queue via the write queue address input. Conversely, data being read from the device read port is read from a queue selected via the read queue address input. Data can be simultaneously written into and read from the same queue or different queues. Once a queue is selected for data writes or reads, the writing and reading operation is performed in the same manner as a conventional IDT synchronous FIFO, utilizing clocks and enables, there is a single clock and enable per port. When a specific queue is addressed on the write port, data placed on the data inputs is written to that queue sequentially based on the rising edge of a write clock provided setup and hold times are met. Conversely, data is read on to the output port after an access time from a rising edge on a read clock.

The operation of the write port is comparable to the function of a conventional FIFO operating in standard IDT mode. Write operations can be performed on the write port provided that the queue currently selected is not full, a full flag output provides status of the selected queue. The operation of the read port is comparable to the function of a conventional FIFO operating in FWFT mode. When a queue is selected on the output port, the next word in that queue will automatically fall through to the output register. All subsequent words from that queue require an enabled read cycle. Data cannot be read from a selected queue if that queue is empty, the read port provides an Empty flag indicating when data read out is valid. If the user switches to a queue that is empty, the last word from the previous queue will remain on the output bus. In addition to First Word Fall Through (FWFT) the device can operate in IDT Standard mode or packet mode. In IDT Standard mode the read port provides a word to the output bus (Qout) for each clock cycle that $\overline{REN}$ is asserted. Refer to Figure 48, *Read Queue Select, Read Operation (IDT Mode)*. In packet mode the device asserts a packet ready status flag to indicate one or more packets are available for reading.

As mentioned, the write port has a full flag, providing full status of the selected queue. Along with the full flag a dedicated almost full flag is provided, this almost full flag is similar to the almost full flag of a conventional IDT FIFO. The device provides a user programmable almost full flag for all 8 queues and when a respective queue is selected on the write port, the almost full flag provides status for that queue. Conversely, the read port has an Empty flag, providing status of the data being read from the queue selected on the read port. As well as the Empty flag the device provides a dedicated almost empty flag. This almost empty flag is similar to the almost empty flag of a conventional IDT FIFO. The device provides a user programmable almost empty flag for each 8 queues and when a respective queue is selected on the read port, the almost empty flag provides status for that queue.

PROGRAMMABLE FLAG BUSSES

In addition to these dedicated flags, full & almost full on the write port and Output Ready & almost empty on the read port, there are two flag status busses. An almost full flag status bus is provided, this bus is 8 bits wide. Also, an almost empty flag status bus is provided, again this bus is 8 bits wide. The purpose of these flag busses is to provide the user with a means by which to monitor the data levels within queues that may not be selected on the write or read port. As mentioned, the device provides almost full and almost empty registers (programmable by the user) for each of the 8 queues in the device.

In the IDT72P51339/72P51349/72P51359/72P51369 multi-queue flow-control devices the user has the option of utilizing anywhere between 1 and 8 queues, therefore the 8 bit flag status busses are multiplexed between the 8 queues, a flag bus can only provide status for 2 of the 8 queues at any moment, this is referred to as a "Status Word", such that when the bus is providing status of queues 1 through 8, this is status word 1, when it is queues 9 through 16, this is status word 2 and so on up to status word 16. If less than 8 queues are setup in the device, there are still 4 status words, such that in "Polled" mode of operation the flag bus will still cycle through 4 status words. If for example only 22 queues are setup, status words 1 and 2 will reflect status of queues 1 through 8 and 9 through 16 respectively. Status word 3 will reflect the status of queues 17 through 22 on the least significant 6 bits, the most significant 2 bits of the flag bus are don't care. The remaining status words are not used as there are no queues to report.

The flag busses are available in two user selectable modes of operation, "Polled" or "Direct". When operating in polled mode a flag bus provides status of each status word sequentially, that is, on each rising edge of a clock the flag bus is updated to show the status of each status word in order. The rising edge of the write clock will update the almost full bus and a rising edge on the read clock will update the almost empty bus. The mode of operation is always the same for both the almost full and almost empty flag busses. When operating in direct mode, the status word on the flag bus is selected by the user. So the user can actually address the status word to be placed on the flag status busses, these flag busses operate independently of one another. Addressing of the almost full flag bus is done via the write port and addressing of the almost empty flag bus is done via the read port.

PACKET READY

The multi-queue flow-control device also offers a "Packet Mode" operation. Packet Mode is user selectable. In packet mode with a x36 bit word length, users can define the length of packets or frame by using the two most significant bits of the word. In a 36-bit word, bit 34 is used to mark the Start of Packet (SOP) and bit 35 is used to mark the End of Packet (EOP) as shown in Table 10. When writing data into a given queue , the first word being written is marked, by the user setting bit 34 as the "Start of Packet" (SOP) and the last word written is marked as the "End of Packet" (EOP) with all words written between the Start of Packet (SOP) marker (bit 34) and the End of packet (EOP) packet marker

(bit 35) constituting the entire packet. A packet can be any length the user desires, up to the total available memory in the multi-queue device. The device monitors the SOP (bit 34) and looks for the word that contains the EOP (bit 35). The read port is supplied with an additional status flag, "Packet Ready". The Packet Ready ($\overline{PR}$) flag in conjunction with Empty Flag or Output Ready flag ($\overline{EF}$/$\overline{OR}$) indicates when at least one packet is available to read. When in packet mode the almost empty flag status , provides packet ready flag status for individual queues.

EXPANSION (IDT STANDARD MODE)

Expansion of multi-queue devices is also possible. Up to 8 devices can be connected in a parallel bus configuration as indicated in Figure 67, *Expansion using ID codes*, and Figure 68, *Expansion using $\overline{WCS}$/$\overline{RCS}$* providing both depth expansion and/or queue expansion. Expansion of devices is supported only in IDT Standard mode. Depth Expansion means expanding the depths of individual queues. Queue expansion means increasing the total number of queues available. Depth expansion is possible by virtue of the fact that more memory blocks within a multi-queue device can be allocated to a fewer number of queues to increase the depth of each queue. For example, depth expansion of 8 devices provides the possibility of 8 queues of 4096K bits, each queue being setup within a single device utilizing all memory blocks available to produce a single queue. This is the deepest queue that can setup within a device.

For queue expansion a maximum number of 256 queues (32 x 8 queues) may be setup, with a average of each queue being 16,384K x36 deep using 8 devices, each with 8 queues. If fewer queues are desired, then more memory blocks will be available to increase queue depths if desired. When connecting multi-queue devices in expansion configuration all respective input pins (data & control) and output pins (data & flags), should be "connected" together between individual devices. Refer to Figure 67, *Expansion using ID codes*, and Figure 68, *Expansion using $\overline{WCS}$/$\overline{RCS}$* for device connection details.

PIN DESCRIPTIONS

Symbol & (Pin No.)	Name	I/O TYPE	Description
BM [3:0] (J1, L14,15,16)	Bus Matching	HSTL-LVTTL INPUT	These pins define the bus width of the input write port and the output read port of the device. The bus widths are set during a Master Rest cycle. The BM[3:0] signals must meet the setup and hold time requirements of Master Reset and must not toggle/change state after a Master Reset cycle.
D[35:0] Din (See Pin No. table for details)	Data Input Bus	HSTL-LVTTL INPUT	These are the 36 data input pins. Data is written into the device via these input pins on the rising edge of WCLK provided that $\overline{WEN}$ is LOW. Note, that in Packet mode D32-D35 may be used as packet markers, please see packet ready functional discussion for more detail. Due to bus matching not all inputs may be used, any unused inputs should be tied LOW. D[35] Transmit End of Packet (TEOP) D[34] Transmit Start of Packet (TSOP) D[33:32] User definable bits D[31:0] Data input bits
DF[1] (L3)	Default Flag	HSTL-LVTTL INPUT	If the user requires default programming of the multi-queue device, this pin must be setup before Master Reset and must not toggle during any device operation. The state of this input at master reset determines the value of the $\overline{PAE}$/$\overline{PAF}$ flag offsets. If DF is LOW the value is 8, if DF is HIGH the value is 128.
DFM[1] (L2)	Default Mode	HSTL-LVTTL INPUT	The multi-queue device requires programming after master reset. The user can do this serially via the serial port, or via parallel programming or by the default programming option The default programming option provides a pre-defined configuration. If DFM is LOW at master reset then serial mode will be selected, if HIGH then default mode is selected.
$\overline{EF}$/$\overline{OR}$ (P9)	Empty Flag/ Output Ready	HSTL-LVTTL OUTPUT	This signal is bi-modal. When IDT Standard mode is selected the pin provides Empty Flag ($\overline{EF}$) status. When FWFT mode is selected the pin provides output ready ($\overline{OR}$) status. This output flag provides Output Ready status for the data word present on the multi-queue flow-control device data output bus, Qout in FWFT mode. This flag is a 2-stage delayed to match the data output path delay. There is a 3 RCLK cycle delay in IDT Standard mode and a 4 cycle delay for FWFT mode from the time a given queue is selected for reads, to the time the $\overline{OR}$ flag represents the data in that queue. When a selected queue on the read port is read to empty, the $\overline{OR}$ flag will go HIGH, indicating that data on the output bus is not valid. The $\overline{OR}$ flag also has High-Impedance capability, required when multiple devices are used and the $\overline{OR}$ flags are tied together.
ESTR (R15)	$\overline{PAE}$n Flag Bus Strobe	HSTL-LVTTL INPUT	If direct operation of the $\overline{PAE}$n bus has been selected, the ESTR input is used in conjunction with RCLK and the RDADD bus to select a status word of queues to be placed on to the $\overline{PAE}$n bus outputs. A status word addressed via the RDADD bus is selected on the rising edge of RCLK provided that ESTR is HIGH. If Polled operations has been selected, ESTR should be tied inactive, LOW. Note, that a $\overline{PAE}$n flag bus selection cannot be made, (ESTR must NOT go active) until programming of the part has been completed and $\overline{SENO}$ has gone LOW.
ESYNC (R16)	$\overline{PAE}$n Bus Sync	HSTL-LVTTL OUTPUT	ESYNC is an output from the multi-queue device that provides a synchronizing pulse for the $\overline{PAE}$n bus during Polled operation of the $\overline{PAE}$n bus. During Polled operation each status word of queue status flags is loaded on to the $\overline{PAE}$n bus outputs sequentially based on RCLK. The first RCLK rising edge loads status word 1 on to $\overline{PAE}$n, the second RCLK rising edge loads status word 2 and so on. The fifth RCLK rising edge will again load status word 1. During the RCLK cycle that status word 1 of a selected device is placed on to the $\overline{PAE}$n bus, the ESYNC output will be HIGH. For all other status words of that device, the ESYNC output will be LOW.
EXI (T16)	$\overline{PAE}$n Bus Expansion In	HSTL-LVTTL INPUT	The EXI input is used when multi-queue devices are connected in expansion configuration and Polled $\overline{PAE}$n bus operation has been selected . EXI of device 'N' connects directly to EXO of device 'N-1'. The EXI receives a token from the previous device in a chain. In single device mode the EXI input must be tied LOW if the $\overline{PAE}$n bus is operated in direct mode. If the $\overline{PAE}$n bus is operated in polled mode the EXI input must be connected to the EXO output of the same device. In expansion configuration the EXI of the first device should be tied LOW, when direct mode is selected.
EXO (T15)	$\overline{PAE}$n Bus Expansion Out	HSTL-LVTTL OUTPUT	EXO is an output that is used when multi-queue devices are connected in expansion configuration and Polled $\overline{PAE}$n bus operation has been selected . EXO of device 'N' connects directly to EXI of device 'N+1'. This pin pulses when device N has placed its final (4th) status word on to the $\overline{PAE}$n bus with respect to RCLK. This pulse (token) is then passed on to the next device in the chain 'N+1' and on the next RCLK rising edge the first status word of device N+1 will be loaded on to the $\overline{PAE}$n bus. This continues through the chain and EXO of the last device is then looped back to EXI of the first device. The ESYNC output of each device in the chain provides synchronization to the user of this looping event.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
$\overline{FF}/\overline{IR}$ (P8)	Full Flag/ Input Ready	HSTL-LVTTL OUTPUT	This pin provides the full flag output for the active Queue, that is, the queue selected on the input port for write operations, (selected via WCLK, WRADD bus and WADEN). On the 3rd WCLK cycle after a queue selection, this flag will show the status of the newly selected queue. Data can be written to this queue on the next cycle provided $\overline{FF}$ is HIGH. This flag has High-Impedance capability, this is important during expansion of devices, when the $\overline{FF}$ flag output of up to 8 devices may be connected together on a common line. The device with a queue selected takes control of the $\overline{FF}$ bus, all other devices place their $\overline{FF}$ output into High-Impedance. When a queue selection is made on the write port this output will switch from High-Impedance control on the next WCLK cycle. This flag is synchronized to WCLK.
FM[1] (K16)	Flag Mode	HSTL-LVTTL INPUT	This pin is setup before a master reset and must not toggle during any device operation. The state of the FM pin during Master Reset will determine whether the $\overline{PAF}$n and $\overline{PAE}$n flag busses operate in either Polled or Direct mode. If this pin is HIGH the mode is Polled, if LOW then it will be Direct.
FSTR (R4)	$\overline{PAF}$n Flag Bus Strobe	HSTL-LVTTL INPUT	If direct operation of the $\overline{PAF}$n bus has been selected, the FSTR input is used in conjunction with WCLK and the WRADD bus to select a status word of queues to be placed on to the $\overline{PAF}$n bus outputs. A status word addressed via the WRADD bus is selected on the rising edge of WCLK provided that FSTR is HIGH. If Polled operations has been selected, FSTR should be tied inactive, LOW. Note, that a $\overline{PAF}$n flag bus selection cannot be made, (FSTR must NOT go active) until programming of the part has been completed and $\overline{SENO}$ has gone LOW.
FSYNC (R3)	$\overline{PAF}$n Bus Sync	HSTL-LVTTL OUTPUT	FSYNC is an output from the multi-queue device that provides a synchronizing pulse for the $\overline{PAF}$n bus during Polled operation of the $\overline{PAF}$n bus. During Polled operation each status word of queue status flags is loaded on to the $\overline{PAF}$n bus outputs sequentially based on WCLK. The first WCLK rising edge loads status word 1 on to $\overline{PAF}$n, the second WCLK rising edge loads status word 2 and so on. The fifth WCLK rising edge will again load status word 1. During the WCLK cycle that status word 1 of a selected device is placed on to the $\overline{PAF}$n bus, the FSYNC output will be HIGH. For all other status words of that device, the FSYNC output will be LOW.
FWFT (R11)	First Word Fall Through	HSTL-LVTTL INPUT	First word fall through (FWFT) or IDT Standard mode is selected during a Master Reset cycle. To select FWFT mode assert the FWFT signal = HIGH, if FWFT = LOW during the master reset then IDT Standard mode is selected.
FXI (T2)	$\overline{PAF}$n Bus Expansion In	HSTL-LVTTL INPUT	The FXI input is used when multi-queue devices are connected in expansion configuration and Polled $\overline{PAF}$n bus operation has been selected . FXI of device 'N' connects directly to FXO of device 'N-1'. The FXI receives a token from the previous device in a chain. In single device mode the FXI input must be tied LOW if the $\overline{PAF}$n bus is operated in direct mode. If the $\overline{PAF}$n bus is operated in polled mode the FXI input must be connected to the FXO output of the same device. In expansion configuration the FXI of the first device should be tied LOW, when direct mode is selected.
FXO (T3)	$\overline{PAF}$n Bus Expansion Out	HSTL-LVTTL OUTPUT	FXO is an output that is used when multi-queue devices are connected in expansion configuration and Polled $\overline{PAF}$n bus operation has been selected . FXO of device 'N' connects directly to FXI of device 'N+1'. This pin pulses when device N has placed its final (4th) status word on to the $\overline{PAF}$n bus with respect to WCLK. This pulse (token) is then passed on to the next device in the chain 'N+1' and on the next WCLK rising edge the first status word of device N+1 will be loaded on to the $\overline{PAF}$n bus. This continues through the chain and FXO of the last device is then looped back to FXI of the first device. The FSYNC output of each device in the chain provides synchronization to the user of this looping event.
ID[2:0][1] (ID2-C9 ID1-A10 ID0-B10)	Device ID Pins	HSTL-LVTTL INPUT	For the 8Q multi-queue device the WRADD and RDADD address busses are 8 bits wide. When a queue selection takes place the 3 MSb's (bits 7, 6, 5) of this 8 bit address bus are used to address the specific device (the 5-7 LSb's are used to address the queue within that device). During write/read operations the 3 MSb's of the address are compared to the device ID pins. In an eight device expansion configuration, the first device in a chain of multi-queue's (connected in expansion configuration), may be setup as '000' (this is referred to as the Master Device), the second as '001' and so on through to device 8 which is '111', however the ID does not have to match the device order. In single device mode these pins should be setup as '000' and the 3 MSb's of the WRADD and RDADD address busses should be tied LOW. The ID[2:0] inputs setup a respective devices ID during master reset. These ID pins must not toggle during any device operation. Note, the device selected as the 'Master' must be ID '000'. In serial programming, the master device (ID 000) must be programmed last.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
IOSEL (C8)	IO Select	LVTTL INPUT	This pin is used to select either HSTL or 2.5V LVTTL operation for the I/O. If HSTL or eHSTL I/O are required then IOSEL should be tied HIGH (V_{DDQ}). If LVTTL I/O are required then it should be tied LOW.
MAST[1] (K15)	Master Device	HSTL-LVTTL INPUT	The state of this input at Master Reset determines whether a given device (within a chain of devices), is the Master device or a Slave. If this pin is HIGH, the device is the master if it is LOW then it is a Slave. The master device is the first to take control of all outputs after a master reset, all slave devices go to High-Impedance, preventing bus contention. If a multi-queue device is being used in single device mode, this pin must be set HIGH.
$\overline{MRS}$ (T9)	Master Reset	HSTL-LVTTL INPUT	A master reset is performed by taking $\overline{MRS}$ from HIGH to LOW, to HIGH. Device programming is required after master reset.
$\overline{OE}$ (M14)	Output Enable	HSTL-LVTTL INPUT	The Output enable signal is an Asynchronous signal used to provide three-state control of the multi-queue data output bus, Qout. If a device has been configured as a "Master" device, the Qout data outputs will be in a Low Impedance condition if the $\overline{OE}$ input is LOW. If $\overline{OE}$ is HIGH then the Qout data outputs will be in High Impedance. If a device is configured a "Slave" device, then the Qout data outputs will always be in High Impedance until that device has been selected on the Read Port, at which point $\overline{OE}$ provides three-state of that respective device.
$\overline{PAE}$ (P10)	Programmable Almost-Empty Flag	HSTL-LVTTL OUTPUT	This pin provides the Almost-Empty flag status for the Queue that has been selected on the output port for read operations, (selected via RCLK, RDADD and RADEN). This pin is LOW when the selected Queue is almost-empty. This flag output may be duplicated on one of the $\overline{PAE}$n bus lines. This flag is synchronized to RCLK.
$\overline{PAE}$n/$\overline{PR}$n ($\overline{PAE}$7-P11 $\overline{PAE}$6-P12 $\overline{PAE}$5-R12 $\overline{PAE}$4-T12 $\overline{PAE}$3-P13 $\overline{PAE}$2-R13 $\overline{PAE}$1-T13 $\overline{PAE}$0-T14)	Programmable Almost-Empty Flag Bus/Packet Ready Flag Bus	HSTL-LVTTL OUTPUT	On the 32Q device the $\overline{PAE}$n/$\overline{PR}$n bus is 8 bits wide. During a Master Reset this bus is setup for either Almost Empty mode or Packet mode. This output bus provides $\overline{PAE}$/$\overline{PR}$n status of 8 queues (1 status word), within a selected device, having a maximum of 16 status words. During Queue read/write operations these outputs provide programmable empty flag status or packet ready status, in either direct or polled mode. The mode of flag operation is determined during master reset via the state of the FM input. This flag bus is capable of High-Impedance state, this is important during expansion of multi-queue devices. During direct operation the $\overline{PAE}$n/$\overline{PR}$n bus is updated to show the $\overline{PAE}$/$\overline{PR}$ status of a status word of queues within a selected device. Selection is made using RCLK, ESTR and RDADD. During Polled operation the $\overline{PAE}$n/$\overline{PR}$n bus is loaded with the $\overline{PAE}$/$\overline{PR}$n status of multi-queue flow-control status words sequentially based on the rising edge of RCLK. $\overline{PAE}$ or $\overline{PR}$ operation is determined by the state of PKT during master reset.
$\overline{PAF}$ (R8)	Programmable Almost-Full Flag	HSTL-LVTTL OUTPUT	This pin provides the Almost-Full flag status for the Queue that has been selected on the input port for write operations, (selected via WCLK, WRADD and WADEN). This pin is LOW when the selected Queue is almost-full. This flag output may be duplicated on one of the $\overline{PAF}$n bus lines. This flag is synchronized to WCLK.
$\overline{PAF}$n ($\overline{PAF}$7-P7 $\overline{PAF}$6-P6 $\overline{PAF}$5-R6 $\overline{PAF}$4-R7 $\overline{PAF}$3-P5 $\overline{PAF}$2-R5 $\overline{PAF}$1-T5 $\overline{PAF}$0-T4)	Programmable Almost-Full Flag Bus	HSTL-LVTTL OUTPUT	On the 32Q device the $\overline{PAF}$n bus is 8 bits wide. At any one time this output bus provides $\overline{PAF}$ status of 8 queues (1 status word), within a selected device, having a maximum of 16 status words. During Queue read/write operations these outputs provide programmable full flag status, in either direct or polled mode. The mode of flag operation is determined during master reset via the state of the FM input. This flag bus is capable of High-Impedance state, this is important during expansion of multi-queue devices. During direct operation the $\overline{PAF}$n bus is updated to show the $\overline{PAF}$ status of a status word of queues within a selected device. Selection is made using WCLK, FSTR, WRADD and WADEN. During Polled operation the $\overline{PAF}$n bus is loaded with the $\overline{PAF}$ status of multi-queue flow-control status words sequentially based on the rising edge of WCLK.
PKT[1] (J14)	Packet Mode	HSTL-LVTTL INPUT	The state of this pin during a Master Reset will determine whether the part is operating in Packet mode providing both a Packet Ready ($\overline{PR}$) output and a Programmable Almost Empty ($\overline{PAE}$) discrete output, or standard mode, providing a ($\overline{PAE}$) output only. If this pin is HIGH during Master Reset the part will operate in packet mode, if it is LOW then almost empty mode. If packet mode has been selected the read port flag bus becomes packet ready flag bus, $\overline{PR}$n and the discrete packet ready flag, $\overline{PR}$ is functional. If almost empty operation has been selected then the flag bus provides almost empty status, $\overline{PAE}$n and the discrete almost empty flag, $\overline{PAE}$ is functional, the $\overline{PR}$ flag is inactive and should not be connected. Packet Ready utilizes user marked locations to identify start and end of packets being written into the device.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
$\overline{PR}$ (R9)	Packet Ready Flag	HSTL-LVTTL OUTPUT	If packet mode has been selected this flag output provides Packet Ready status of the Queue selected for read operations. During a master reset the state of the PKT input determines whether Packet mode of operation will be used. If Packet mode is selected, then the condition of the $\overline{PR}$ flag and $\overline{EF}$/$\overline{OR}$ signal are asserted indicates a packet is ready for reading. The user must mark the start of a packet and the end of a packet when writing data into a queue. Using the Start Of Packet (SOP) and End Of Packet (EOP) markers, the multi-queue device sets $\overline{PR}$ LOW if one or more "complete" packets are available in the queue. A complete packet(s) must be written before the user is allowed to switch queues.
Q[35:0] Qout (See Pin No. table for details)	Data Output Bus	HSTL-LVTTL OUTPUT	These are the 36 data output pins. Data is read out of the device via these output pins on the rising edge of RCLK provided that $\overline{REN}$ is LOW, $\overline{OE}$ is LOW and the Queue is selected. Note, that in Packet Ready mode Q32-Q35 may be used as packet markers, please see packet ready functional discussion for more detail. Due to bus matching not all outputs may be used, any unused outputs should not be connected.
QSEL[1:0] (QSEL1-K1 QSEL0-J2	Queue Select	HSTL-LVTTL INPUT	The QSEL pins provides various queue programming options. Refer to Table 2, for details. 1. A QSEL value of 00, enables the user to program the number of queues using the Write Address bus. 2. A QSEL value of 01, enables the user to program the number of queues using the Read Address bus. 3. A QSEL value of 10, Selects a configuration of 4 queues. 4. A QSEL value of 11, selects a configuration of 8 queues
RADEN (R14)	Read Address Enable	HSTL-LVTTL INPUT	The RADEN input is used in conjunction with RCLK and the RDADD address bus to select a queue to be read from. A queue addressed via the RDADD bus is selected on the rising edge of RCLK provided that RADEN is HIGH. RADEN should be asserted (HIGH) only during a queue change cycle(s). RADEN should not be permanently tied HIGH. RADEN cannot be HIGH for the same RCLK cycle as ESTR. Note, that a read queue selection cannot be made, (RADEN must NOT go active) until programming of the part has been completed and $\overline{SENO}$ has gone LOW.
RCLK (T10)	Read Clock	HSTL-LVTTL INPUT	When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the selected queue via the output bus Qout. The queue to be read is selected via the RDADD address bus and a rising edge of RCLK while RADEN is HIGH. A rising edge of RCLK in conjunction with ESTR and RDADD will also select the $\overline{PAE}$n/$\overline{PR}$n flag status word to be placed on the $\overline{PAE}$n/$\overline{PR}$n bus during direct flag operation. During polled flag operation the $\overline{PAE}$n/$\overline{PR}$n bus is cycled with respect to RCLK and the ESYNC signal is synchronized to RCLK. The $\overline{PAE}$, $\overline{PR}$ and $\overline{OR}$ outputs are all synchronized to RCLK. During device expansion the EXO and EXI signals are based on RCLK. RCLK must be continuous and free-running.
$\overline{RCS}$ (R10)	Read Chip Select	HSTL-LVTTL INPUT	The $\overline{RCS}$ signal in concert with $\overline{REN}$ signal provides control to enable data on to the output read data bus. During a Master Reset cycle the $\overline{RCS}$ it is don't care signal.
RDADD [7:0] (RDADD7-P16 RDADD6-P15 RDADD5-P14 RDADD4-N16 RDADD3-N15 RDADD2-N14 RDADD1-M16 RDADD0-M15)	Read Address Bus	HSTL-LVTTL INPUT	For the 8Q device the RDADD bus is 8 bits. The RDADD bus is a dual purpose address bus. The first function of RDADD is to select a Queue to be read from. The least significant 5 bits of the bus, RDADD[4:0] are used to address 1 of 32 possible queues within a multi-queue device. The most significant 3 bits, RDADD[7:5] are used to select 1 of 8 possible multi-queue devices that may be connected in expansion mode. An in expansion configuration the 3 MSb's will address a device with the matching ID code. The address present on the RDADD bus will be selected on a rising edge of RCLK provided that RADEN is HIGH, (note, that data can be placed on to the Qout bus, read from the previously selected queue on this RCLK edge). Two RCLK rising edges after read queue select, data will be placed on to the Qout outputs from the newly selected queue, regardless of $\overline{REN}$ due to the first word fall through effect. The second function of the RDADD bus is to select the status word of queues to be loaded on to the $\overline{PAE}$n/$\overline{PR}$n bus during strobed flag mode. The least significant 4 bits, RDADD[3:0] are used to select the status word of a device to be placed on the $\overline{PAE}$n bus. The most significant 3 bits, RDADD[7:5] are again used to select 1 of 8 possible multi-queue devices that may be connected in expansion configuration. Address bits RDADD[4] is don't care during status word selection. The status word address present on the RDADD bus will be selected on the rising edge of RCLK provided that ESTR is HIGH, (note, that data can be placed on to the Qout bus, read from the previously selected Queue on this RCLK edge). Please refer to Table 5 for details on RDADD bus.
$\overline{REN}$ (T11)	Read Enable	HSTL-LVTTL INPUT	The $\overline{REN}$ input enables read operations from a selected Queue based on a rising edge of RCLK. In the FWFT mode, a queue to be read from can be selected via RCLK, RADEN and the RDADD address bus regardless of the state of $\overline{REN}$. A read enable is not required to cycle the $\overline{PAE}$n/$\overline{PR}$n bus (in polled mode) or to select the $\overline{PAE}$n status word, (in direct mode).

PIN DESCRIPTIONS (CONTINUED)

Symbol & (Pin No.)	Name	I/O TYPE	Description
SCLK (N3)	Serial Clock	HSTL-LVTTL INPUT	If serial programming of the multi-queue device has been selected during master reset, the SCLK input clocks the serial data through the multi-queue device. Data setup on the SI input is loaded into the device on the rising edge of SCLK provided that $\overline{SENI}$ is enabled, LOW. When expansion of devices is performed the SCLK of all devices should be connected to the same source.
$\overline{SENI}$ (M2)	Serial Input Enable	HSTL-LVTTL INPUT	During serial programming of a multi-queue device, data loaded onto the SI input will be clocked into the part (via a rising edge of SCLK), provided the $\overline{SENI}$ input of that device is LOW. If multiple devices are cascaded, the $\overline{SENI}$ input should be connected to the $\overline{SENO}$ output of the previous device. So when serial loading of a given device is complete, its $\overline{SENO}$ output goes LOW, allowing the next device in the chain to be programmed ($\overline{SENO}$ will follow $\overline{SENI}$ of a given device once that device is programmed). The $\overline{SENI}$ input of the master device (or single device), should be controlled by the user.
$\overline{SENO}$ (M1)	Serial Output Enable	HSTL-LVTTL OUTPUT	This output is used to indicate that serial programming or default programming of the multi-queue device has been completed. $\overline{SENO}$ follows $\overline{SENI}$ once programming of a device is complete. Therefore, $\overline{SENO}$ will go LOW after programming provided $\overline{SENI}$ is LOW, once $\overline{SENI}$ is taken HIGH again, $\overline{SENO}$ will also go HIGH. When the $\overline{SENO}$ output goes LOW, the device is ready to begin normal read/write operations. If multiple devices are cascaded and serial programming of the devices will be used, the $\overline{SENO}$ output should be connected to the $\overline{SENI}$ input of the next device in the chain. When serial programming of the first device is complete, $\overline{SENO}$ will go LOW, thereby taking the $\overline{SENI}$ input of the next device LOW and so on throughout the chain. When a given device in the chain is fully programmed the $\overline{SENO}$ output essentially follows the $\overline{SENI}$ input. The user should monitor the $\overline{SENO}$ output of the final device in the chain. When this output goes LOW, serial loading of all devices has been completed.
SI (L1)	Serial In	HSTL-LVTTL INPUT	During serial programming this pin is loaded with the serial data that will configure the multi-queue devices. Data present on SI will be loaded on a rising edge of SCLK provided that $\overline{SENI}$ is LOW. In expansion mode the serial data input is loaded into the first device in a chain. When that device is loaded and its $\overline{SENO}$ has gone LOW, the data present on SI will be directly output to the SO output. The SO pin of the first device connects to the SI pin of the second and so on. The multi-queue device setup registers are shift registers.
SO (M3)	Serial Out	HSTL-LVTTL OUTPUT	This output is used in expansion configuration and allows serial data to be passed through devices in the chain to complete programming of all devices. The SI of a device connects to SO of the previous device in the chain. The SO of the final device in a chain should not be connected.
TCK[2] (A8)	JTAG Clock	HSTL-LVTTL INPUT	Clock input for JTAG function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and outputs change on the falling edge of TCK. If the JTAG function is not used this signal needs to be tied to GND.
TDI[2] (B9)	JTAG Test Data Input	HSTL-LVTTL INPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded via the TDI on the rising edge of TCK to either the Instruction Register, ID Register and Bypass Register. An internal pull-up resistor forces TDI HIGH if left unconnected.
TDO[2] (A9)	JTAG Test Data Output	HSTL-LVTTL OUTPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded output via the TDO on the falling edge of TCK from either the Instruction Register, ID Register and Bypass Register. This output is high impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
TMS[2] (B8)	JTAG Mode Select	HSTL-LVTTL INPUT	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pull-up resistor forces TMS HIGH if left unconnected.
$\overline{TRST}$[2] (C7)	JTAG Reset	HSTL-LVTTL INPUT	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller. The JTAG TAP controller does not automatically reset upon power-up, thus it must be reset by either this signal or by setting TMS= HIGH for five TCK cycles. If the TAP controller is not properly reset then the outputs will always be in high-impedance. If the JTAG function is used but the user does not want to use $\overline{TRST}$, then $\overline{TRST}$ can be tied with $\overline{MRS}$ to ensure proper queue operation. If the JTAG function is not used then this signal needs to be tied to GND. An internal pull-up resistor forces $\overline{TRST}$ HIGH if left unconnected.
WADEN (P4)	Write Address Enable	HSTL-LVTTL INPUT	The WADEN input is used in conjunction with WCLK and the WRADD address bus to select a queue to be written in to. A queue addressed via the WRADD bus is selected on the rising edge of WCLK provided that WADEN is HIGH. WADEN should be asserted (HIGH) only during a queue change cycle(s). WADEN should not be permanently tied HIGH. WADEN cannot be HIGH for the same WCLK cycle as FSTR. Note,

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
WADEN (Continued)	Write Address Enable	HSTL-LVTTL INPUT	that a write queue selection cannot be made, (WADEN must NOT go active) until programming of the part has been completed and $\overline{SENO}$ has gone LOW.
WCLK (T7)	Write Clock	HSTL-LVTTL INPUT	When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the selected Queue via the input bus, Din. The Queue to be written to is selected via the WRADD address bus and a rising edge of WCLK while WADEN is HIGH. A rising edge of WCLK in conjunction with FSTR and WRADD will also select the flag status word to be placed on the $\overline{PAF}$n bus during direct flag operation. During polled flag operation the $\overline{PAF}$n bus is cycled with respect to WCLK and the FSYNC signal is synchronized to WCLK. The $\overline{PAF}$n, $\overline{PAF}$ and $\overline{FF}$ outputs are all synchronized to WCLK. During device expansion the FXO and FXI signals are based on WCLK. The WCLK must be continuous and free-running.
$\overline{WCS}$ (T8)	Write Chip Select	HSTL-LVTTL INPUT	The $\overline{WCS}$ pin can be regarded as a second $\overline{WEN}$ input, enabling/disabling write operations.
$\overline{WEN}$ (T6)	Write Enable	HSTL-LVTTL INPUT	The $\overline{WEN}$ input enables write operations to a selected Queue based on a rising edge of WCLK. A queue to be written to can be selected via WCLK, WADEN and the WRADD address bus regardless of the state of $\overline{WEN}$. Data present on Din can be written to a newly selected queue on the second WCLK cycle after queue selection provided that $\overline{WEN}$ is LOW. A write enable is not required to cycle the $\overline{PAF}$n bus (in polled mode) or to select the $\overline{PAF}$n status word , (in direct mode).
WRADD [7:0] (WRADD7-T1 WRADD6-R1 WRADD5-R2 WRADD4-P1 WRADD3-P2 WRADD2-P3 WRADD1-N1 WRADD0-N2)	Write Address Bus	HSTL-LVTTL INPUT	For the 32Q device the WRADD bus is 8 bits. The WRADD bus is a dual purpose address bus. The first function of WRADD is to select a Queue to be written to. The least significant 5 bits of the bus, WRADD[4:0] are used to address 1 of 32 possible queues within a multi-queue device. In expansion configuration the most significant 3 bits, WRADD[7:5] are used to select 1 of 8 possible multi-queue devices (dependant on the number of queues addressed) that may be connected in expansion configuration. These 3 MSb's will address a device with the matching ID code. The address present on the WRADD bus will be selected on a rising edge of WCLK provided that WADEN is HIGH, (note, that data present on the Din bus can be written into the previously selected queue on this WCLK edge and on the next rising WCLK also, providing that $\overline{WEN}$ is LOW). Two WCLK rising edges after write queue select, data can be written into the newly selected queue. The second function of the WRADD bus is to select the status word of queues to be loaded on to the $\overline{PAF}$n bus during strobed flag mode. The least significant 4 bits, WRADD[3:0] are used to select the status word of a device to be placed on the $\overline{PAF}$n bus. The most significant 3 bits, WRADD[7:5] are again used to select 1 of 8 possible multi-queue devices that may be connected in expansion configuration. Address bits WRADD[4] is don't care during status word selection. The status word address present on the WRADD bus will be selected on the rising edge of WCLK provided that FSTR is HIGH, (note, that data can be written into the previously selected queue on this WCLK edge). Please refer to Table 4 for details on the WRADD bus.
V_{DD} (See pg. 16)	+1.8V Supply	Power	These are V_{DD} power supply pins and must all be connected to a +1.8V supply rail.
V_{DDQ} (See pg. 16)	O/P Rail Voltage	Power	These pins must be tied to the desired output rail voltage. For LVTTL I/O these pins must be connected to +2.5V, for HSTL these pins must be connected to +1.5V and for eHSTL these pins must be connected to +1.8V.
GND (See pg. 16)	Ground Pin	Ground	These are Ground pins and must all be connected to the GND supply rail.
Vref (K3)	Reference Voltage	HSTL INPUT	This is a Voltage Reference input and must be connected to a voltage level determined from the table "Recommended DC Operating Conditions". The input provides the reference level for HSTL/eHSTL inputs. For LVTTL I/O mode this input should be tied to GND.

NOTES:
1. Inputs should not change after Master Reset.
2. These pins are for the JTAG port. Please refer to pages 82-86 and Figures 71-73.

PIN NUMBER TABLE

Symbol	Name	I/O TYPE	Pin Number
D[35:0] Din	Data Input Bus	HSTL-LVTTL INPUT	D35-J3, D(34-32)-H(3-1), D(31-29)-G(3-1), D(28-26)-F(3-1), D(25-23)-E(3-1), D(22-20)-D(3-1), D(19-17)-C(3-1), D(16,15)-B(2,1), D(14-12)-A(1-3), D11-B3, D10-A4, D9-B4, D8-C4, D7-A5, D6-B5, D5-C5, D4-A6, D3-B6, D2-C6, D1-A7, D0-B7
Q[35:0] Qout	Data Output Bus	HSTL-LVTTL OUTPUT	Q(35,34)-J(15,16), Q(33-31)-H(14-16), Q(30-28)-G(14-16), Q(27-25)-F(14-16), Q(24-22)-E(14-16), Q(21,20)-D(15,16), Q19-B16, Q(18,17)-C(16,15), Q16-D14, Q(15,14)-A(16,15), Q13-B15, Q12-A14, Q11-B14, Q10-C14, Q9-A13, Q8-B13, Q7-C13, Q6-A12, Q5-B12, Q4-C12, Q3-A11, Q2-B11, Q(1,0)-C(11,10)
V_{DD}	+1.8V Supply	Power	D(7-10), E(6,7,10,11), F(5,12), G(4,5,12,13), H(4,13), J(4,13), K(4,5,12,13), L(5,12), M(6,7,10,11), N(7-10)
V_{DDQ}	O/P Rail Voltage	Power	D(4-6,11-13), E(4,5,12,13), F(4,13), L(4,13), M(4,5,12,13), N(4-6,11-13)
GND	Ground Pin	Ground	E(8-9), F(6-11), G(6-11), H(5-12), J(1,5-12), K(2,6-11,14), L(6-11), M(8-9)

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +2.9[2]	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Compliant with JEDEC JESD8-5. V_{DD} terminal only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2,3]	Input Capacitance	V_{IN} = 0V	10[3]	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	15	pF

NOTES:

1. With output deselected, ($\overline{OE} \geq V_{IH}$).
2. Characterized values, not currently tested.
3. C_{IN} for Vref is 20pF.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.7	1.8	1.9	V
V_{DDQ}	Output Rail Voltage for I/Os	— LVTTL	2.375	2.5	2.625	V
		— eHSTL	1.7	1.8	1.9	V
		— HSTL	1.4	1.5	1.6	V
GND	Supply Voltage		0	0	0	V
V_{IH}[2]	Input High Voltage	— LVTTL	1.7	—	2.625	V
		— eHSTL	V_{REF}+0.2	—	—	V
		— HSTL	V_{REF}+0.2	—	—	V
V_{IL}	Input Low Voltage	— LVTTL	-0.3	—	0.7	V
		— eHSTL	—	—	V_{REF}-0.2	V
		— HSTL	—	—	V_{REF}-0.2	V
V_{REF}[1] (HSTL only)	Voltage Reference Input	— eHSTL	0.8	0.9	1.0	V
		— HSTL	0.68	0.75	0.9	V
T_A	Operating Temperature Commercial		0	—	70	°C
T_A	Operating Temperature Industrial		-40	—	85	°C

NOTE:

1. V_{REF} is only required for HSTL or eHSTL inputs. V_{REF} should be tied LOW for LVTTL operation.
2. V_{IH} AC Component = V_{REF} + 0.4V

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{DD} = 1.8V ± 0.10V, T_A = 0°C to +70°C;Industrial: V_{DD} = 1.8V ± 0.10V, T_A = -40°C to +85°C)

Symbol	Parameter		Min.	Max.	Unit
I_{LI}	Input Leakage Current		–10	10	µA
I_{LO}	Output Leakage Current		–10	10	µA
V_{OH}[3]	Output Logic "1" Voltage,	I_{OH} = –8 mA @ V_{DDQ} = 2.5V ± 0.125V (LVTTL)	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA @ V_{DDQ} = 1.8V ± 0.1V (eHSTL)	V_{DDQ}-0.4	—	V
		I_{OH} = –8 mA @ V_{DDQ} = 1.5V ± 0.1V (HSTL)	V_{DDQ}-0.4	—	V
V_{OL}	Output Logic "0" Voltage,	I_{OL} = 8 mA @ V_{DDQ} = 2.5V ± 0.125V (LVTTL)	—	0.4V	V
		I_{OL} = 8 mA @ V_{DDQ} = 1.8V ± 0.1V (eHSTL)	—	0.4V	V
		I_{OL} = 8 mA @ V_{DDQ} = 1.5V ± 0.1V (HSTL)	—	0.4V	V
I_{DD1}[1,2]	Active V_{DD} Current (V_{DD} = 1.8V)	I/O = LVTTL	—	80	mA
		I/O = HSTL	—	150	mA
		I/O = eHSTL	—	150	mA
I_{DD2}[1, 5]	Standby V_{DD} Current (V_{DD} = 1.8V)	I/O = LVTTL	—	25	mA
		I/O = HSTL	—	100	mA
		I/O = eHSTL	—	100	mA
I_{DDQ}[1,2]	Active V_{DDQ} Current (V_{DDQ} = 2.5V LVTTL)	I/O = LVTTL	—	10	mA
	(V_{DDQ} = 1.5V HSTL)	I/O = HSTL	—	10	mA
	(V_{DDQ} = 1.8V eHSTL)	I/O = eHSTL	—	10	mA

NOTES:

1. Both WCLK and RCLK toggling at 20MHz.
2. Data inputs toggling at 10MHz.
3. Total Power consumed: PT = [(V_{DD} x I_{DD}) + (V_{DDQ} x I_{DDQ})].
4. Outputs are not 3.3V tolerant.
5. The following inputs should be pulled to GND: $\overline{WRADD}$, $\overline{RDADD}$, $\overline{WADEN}$, $\overline{FSTR}$, $\overline{ESTR}$, $\overline{SCLK}$, $\overline{SI}$, $\overline{EXI}$, $\overline{FXI}$ and all Data Inputs.
   The following inputs should be pulled to V_{DD}: $\overline{WEN}$, $\overline{REN}$, $\overline{SENI}$, $\overline{MRS}$, TDI, TMS and $\overline{TRST}$.
   All other inputs are don't care and should be at a known state.

HSTL
1.5V AC TEST CONDITIONS

Input Pulse Levels	0.25 to 1.25V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.75
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.5V ± 0.1V.

EXTENDED HSTL
1.8V AC TEST CONDITIONS

Input Pulse Levels	0.4 to 1.4V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.9
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.8V ± 0.1V.

2.5V LVTTL
2.5V AC TEST CONDITIONS

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	1ns
Input Timing Reference Levels	$V_{DD}/2$
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 2.5V ± 0.125V.

AC TEST LOADS

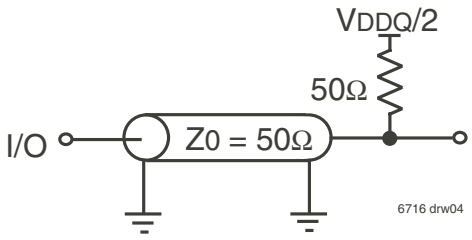


Figure 2a. AC Test Load

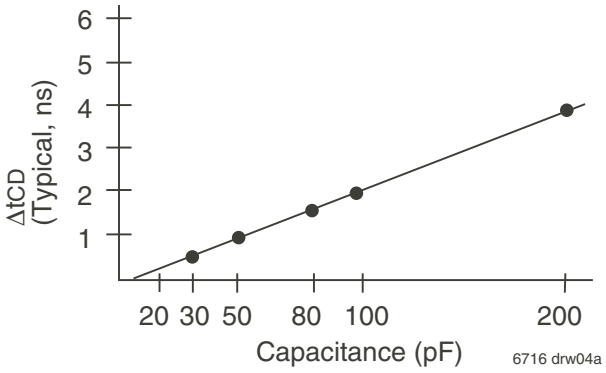
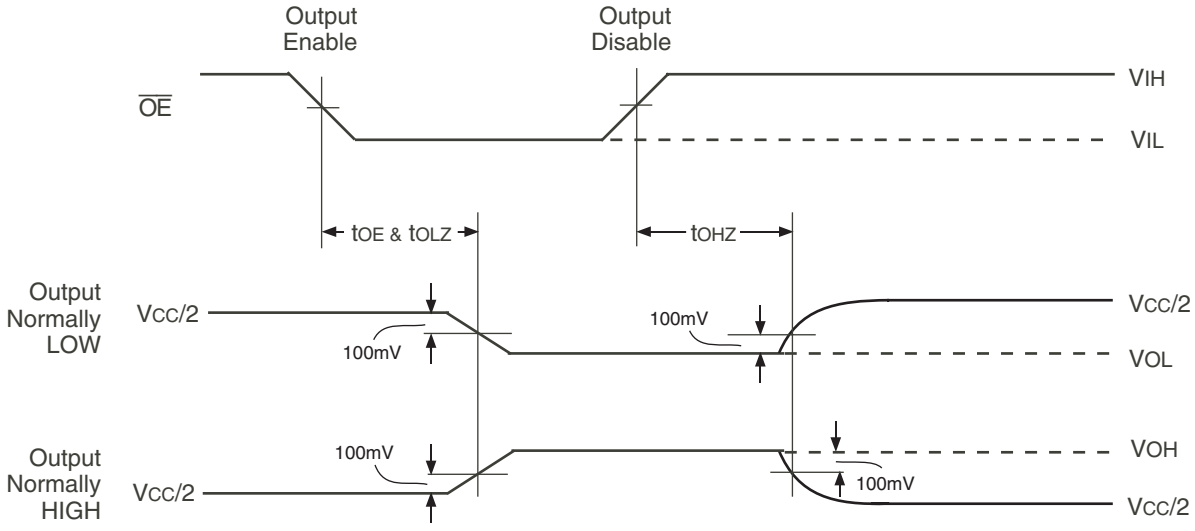


Figure 2b. Lumped Capacitive Load, Typical Derating

OUTPUT ENABLE & DISABLE TIMING



NOTE:
1. $\overline{REN}$ is HIGH.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{DD} = 1.8V ± 0.10V, T_A = 0°C to +70°C;Industrial: V_{DD} = 1.8V ± 0.10V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

Symbol	Parameter	Commercial IDT72P51339L5 IDT72P51349L5 IDT72P51359L5 IDT72P51369L5		Com'l & Ind'l[1] IDT72P51339L6 IDT72P51349L6 IDT72P51359L6 IDT72P51369L6		Unit
		Min.	Max.	Min.	Max.	
f_S	Clock Cycle Frequency (WCLK & RCLK)	—	200	—	166	MHz
t_A	Data Access Time	0.6	3.6	0.6	3.7	ns
t_{CLK}	Clock Cycle Time	5	—	6	—	ns
t_{CLKH}	Clock High Time	2.25	—	2.7	—	ns
t_{CLKL}	Clock Low Time	2.25	—	2.7	—	ns
t_{DS}	Data Setup Time	1.5	—	2.0	—	ns
t_{DH}	Data Hold Time	0.5	—	0.5	—	ns
t_{ENS}	Enable Setup Time	1.5	—	2.0	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.5	—	ns
t_{RS}	Reset Pulse Width	30	—	30	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	ns
t_{RSF}	Reset Output Status	—	10	—	10	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{OLZ} ($\overline{OE}$-Q_n)[2]	Output Enable to Output in Low-Impedance	0.6	3.6	0.6	3.7	ns
t_{OHZ}[2]	Output Enable to Output in High-Impedance	0.6	3.6	0.6	3.7	ns
t_{OE}	Output Enable to Data Output Ready	0.6	3.6	0.6	3.7	ns
f_C	Clock Cycle Frequency (SCLK)	—	10	—	10	MHz
t_{SCLK}	Serial Clock Cycle	100	—	100	—	ns
t_{SCKH}	Serial Clock High	45	—	45	—	ns
t_{SCKL}	Serial Clock Low	45	—	45	—	ns
t_{SDS}	Serial Data In Setup	20	—	20	—	ns
t_{SDH}	Serial Data In Hold	1.2	—	1.2	—	ns
t_{SENS}	Serial Enable Setup	20	—	20	—	ns
t_{SENH}	Serial Enable Hold	1.2	—	1.2	—	ns
t_{SDO}	SCLK to Serial Data Out	—	20	—	20	ns
t_{SENO}	SCLK to Serial Enable Out	—	20	—	20	ns
t_{SDOP}	Serial Data Out Propagation Delay	0.6	3.7	0.6	3.7	ns
t_{SENOP}	Serial Enable Propagation Delay	0.6	3.7	0.6	3.7	ns
t_{PCSF}	Programming Complete to Status Flag	—	7+1 SCLK	—	7+1 SCLK	clock cycles
t_{AS}	Address Setup	1.5	—	2.0	—	ns
t_{AH}	Address Hold	0.5	—	0.5	—	ns
t_{WFF}	Write Clock to Full Flag	—	3.6	—	3.7	ns
t_{REF}	Read Clock to Empty Flag	—	3.6	—	3.7	ns
t_{STS}	$\overline{PAE}$/$\overline{PAF}$ Strobe Setup	1.5	—	1.5	—	ns
t_{STH}	$\overline{PAE}$/$\overline{PAF}$ Strobe Hold	0.5	—	0.5	—	ns
t_{QS}	Queue Setup	1.5	—	2.0	—	ns
t_{QH}	Queue Hold	0.5	—	0.5	—	ns
t_{WAF}	WCLK to $\overline{PAF}$ flag	0.6	3.6	0.6	3.7	ns
t_{RAE}	RCLK to $\overline{PAE}$ flag	0.6	3.6	0.6	3.7	ns
t_{PAF}	Write Clock to Synchronous Almost-Full Flag Bus	0.6	3.6	0.6	3.7	ns
t_{PAE}	Read Clock to Synchronous Almost-Empty Flag Bus	0.6	3.6	0.6	3.7	ns
t_{PAELZ}[2]	RCLK to $\overline{PAE}$ Flag Bus to Low-Impedance	0.6	3.6	0.6	3.7	ns

NOTES:

1. Industrial temperature range product for the 6ns is available as a standard device. All other speed grades available by special order.
2. Values guaranteed by design, not currently tested.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

(Commercial: V_{DD} = 1.8V ± 0.10V, T_A = 0°C to +70°C;Industrial: V_{DD} = 1.8V ± 0.10V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

Symbol	Parameter	Commercial IDT72P51339L5 IDT72P51349L5 IDT72P51359L5 IDT72P51369L5		Com'l & Ind'l[1] IDT72P51339L6 IDT72P51349L6 IDT72P51359L6 IDT72P51369L6		Unit
		Min.	Max.	Min.	Max.	
t_{PAEHZ}[2]	RCLK to $\overline{PAE}$ Flag Bus to High-Impedance	0.6	3.6	0.6	3.7	ns
t_{PAFLZ}[2]	WCLK to $\overline{PAF}$ Flag Bus to Low-Impedance	0.6	3.6	0.6	3.7	ns
t_{PAFHZ}[2]	WCLK to $\overline{PAF}$ Flag Bus to High-Impedance	0.6	3.6	0.6	3.7	ns
t_{FFHZ}[2]	WCLK to Full Flag/Input Ready to High-Impedance	0.6	3.6	0.6	3.7	ns
t_{FFLZ}[2]	WCLK to Full Flag/Input Ready to Low-Impedance	0.6	3.6	0.6	3.7	ns
t_{EFLZ}[2]	RCLK to Empty Flag/Output Ready Flag to Low-Impedance	0.6	3.6	0.6	3.7	ns
t_{EFHZ}[2]	RCLK to Empty Flag/Output Ready Flag to High-Impedance	0.6	3.6	0.6	3.7	ns
t_{FSYNC}	WCLK to $\overline{PAF}$ Bus Sync to Output	0.6	3.6	0.6	3.7	ns
t_{FXO}	WCLK to $\overline{PAF}$ Bus Expansion to Output	0.6	3.6	0.6	3.7	ns
t_{ESYNC}	RCLK to $\overline{PAE}$ Bus Sync to Output	0.6	3.6	0.6	3.7	ns
t_{EXO}	RCLK to $\overline{PAE}$ Bus Expansion to Output	0.6	3.6	0.6	3.7	ns
t_{PR}	RCLK to Packet Ready Flag	0.6	3.6	0.6	3.7	ns
t_{SKEW1}	SKEW time between RCLK and WCLK for $\overline{FF}$/$\overline{IR}$ and $\overline{EF}$/$\overline{OR}$	5	—	6	—	ns
t_{SKEW2}	SKEW time between RCLK and WCLK for $\overline{PAF}$ and $\overline{PAE}$	5	—	6	—	ns
t_{SKEW3}	SKEW time between RCLK and WCLK for $\overline{PAF}$[0:7] and $\overline{PAE}$[0:7]	5	—	6	—	ns
t_{SKEW4}	SKEW time between RCLK and WCLK for $\overline{PR}$ and $\overline{EF}$/$\overline{OR}$	5	—	6	—	ns
t_{XIS}	Expansion Input Setup	1.5	—	2.0	—	ns
t_{XIH}	Expansion Input Hold	0.5	—	0.5	—	ns
t_{PPMS}	Parallel Programming Setup	15	—	15	—	ns
t_{PPMH}	Parallel Programming Hold	5	—	5	—	ns

NOTES:
1. Industrial temperature range product for the 6ns is available as a standard device. All other speed grades available by special order.
2. Values guaranteed by design, not currently tested.

FUNCTIONAL DESCRIPTION

MASTER RESET

A Master Reset is performed by toggling the $\overline{MRS}$ input from HIGH to LOW to HIGH. During a master reset all internal multi-queue device setup and control registers are initialized and require programming either serially by the user via the serial port, or via parallel programming or by using the default settings. Refer to Figure 4, *Device Programming Hierarchy* for the programming hierarchy structure. During a master reset the state of the following inputs determine the functionality of the part, these pins should be held HIGH or LOW.

PKT – Packet Mode
FM – Flag bus Mode
BM [3:0] – Bus Matching options
MAST – Master Device
ID0, 1, 2 – Device ID
DFM – Programming mode, serial or default
DF – Offset value for $\overline{PAE}$ and $\overline{PAF}$

Once a master reset has taken place, the device must be programmed either serially or via the default method before any read/write operations can begin.

See Figure 37, *Master Reset* for relevant timing.

PROGRAMMING MODE CAPTURED

On the rising of /MRS the programming mode signals (QSEL 0 &1, DEFAULT) are captured. Once the programming mode signals are captured (latched), refer to Table 1 for details. It will then require a number of clock cycles for the device to complete the configuration. Configuration completion is indicated when the $\overline{SENO}$ signal transitions from high to low. The configuration completion indication is consistent with the previous MQ device.

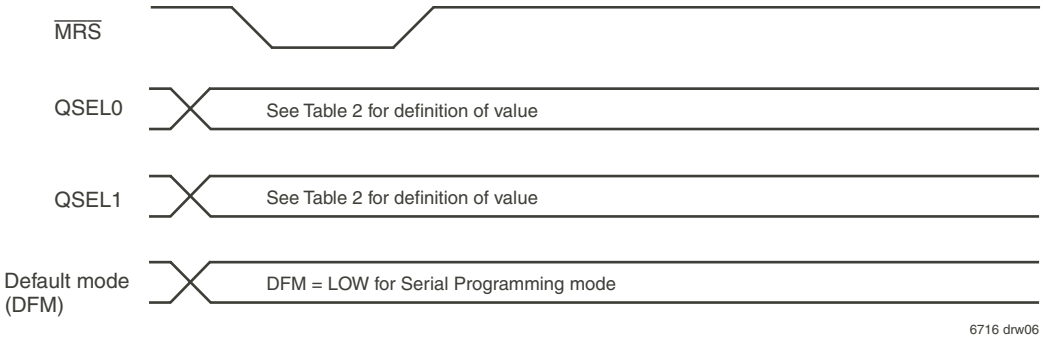


Figure 3. Reference Signals

TABLE 1 — DEVICE PROGRAMMING MODE COMPARISON

Programmable Parameter	Serial Programming	Parallel Programming	Default Programming
Number of Queues	Any number from 1 to 8	Any number from 1 to 8	4 or 8
Queue Depth	Each queue depth can be individualized	The total memory is evenly divided across the queues	The total memory is evenly divided across the queues
$\overline{PAE}$/$\overline{PAF}$ Offset Value	Programmable to any value	Fixed value	Fixed value
Bus Matching	Any combination of x9 or x18 or x36 can be selected using the BM[3:0] bits.	Any combination of x9 or x18 or x36 can be selected using the BM[3:0] bits.	Any combination of x9, x18, or x36 can be selected using the BM[3:0] bits
I/O voltage	LVTTL, eHSTL, HSTL	LVTTL, eHSTL, HSTL	LVTTL, eHSTL, HSTL

TABLE 2 — SETTING THE QUEUE PROGRAMMING MODE DURING MASTER RESET

$\overline{MRS}$	Default Mode (DFM)	QSEL 1	QSEL 0	Queue Programming Method
↑	0	0	0	RESERVED
↑	0	0	1	RESERVED
↑	0	1	0	RESERVED
↑	0	1	1	Serial programming mode
↑	1	0	0	Enables the user to program the number of Queues using the Write Address bus
↑	1	0	1	Enables the user to program the number of Queues using the Read Address bus
↑	1	1	0	Selects 4 Queue
↑	1	1	1	Selects 8 Queue

6716 drw07

SERIAL PROGRAMMING

The multi-queue flow-control device is a fully programmable device, providing the user with flexibility in how queues are configured in terms of the number of queues, depth of each queue and position of the $\overline{PAF}$/$\overline{PAE}$ flags within respective queues. All user programming is done via the serial port after a master reset has taken place. Internally the multi-queue device has setup registers which must be serially loaded, these registers contain values for every queue within the device, such as the depth and $\overline{PAE}$/$\overline{PAF}$ offset values. The IDT72P51339/72P51349/72P51359/72P51369 devices are capable of up to 8 queues and therefore contain 128 sets of registers for the setup of each queue.

During a Master Reset if the DFM (Default Mode) input is LOW, then the device will require serial programming by the user. It is recommended that the user utilize a 'C' program provided by IDT, this program will prompt the user for all information regarding the multi-queue setup. The program will then generate a serial bit stream which should be serially loaded into the device via the serial port. For the IDT72P51339/72P51349/72P51359/72P51369 devices the serial programming requires a total number of serially loaded bits per device, (SCLK cycles with $\overline{SENI}$ enabled), calculated by: 19+(Qx72) where Q is the number of queues the user wishes to setup within the device.

Once the master reset is complete and $\overline{MRS}$ is HIGH, the device can be serially loaded. Data present on the SI (serial in), input is loaded into the serial port on a rising edge of SCLK (serial clock), provided that $\overline{SENI}$ (serial in enable), is LOW. Once serial programming of the device has been successfully completed the device will indicate this via the $\overline{SENO}$ (serial output enable) going active, LOW. Upon detection of completion of programming, the user should cease all programming and take $\overline{SENI}$ inactive, HIGH. Note, $\overline{SENO}$ follows $\overline{SENI}$ once programming of a device is complete. Therefore, $\overline{SENO}$ will go LOW after programming provided $\overline{SENI}$ is LOW, once $\overline{SENI}$ is taken HIGH again, $\overline{SENO}$ will also go HIGH. The operation of the SO output is similar, when programming of a given device is complete, the SO output will follow the SI input.

If devices are being used in expansion configuration the serial ports of devices should be cascaded. The user can load all devices via the serial input port control pins, SI & $\overline{SENI}$, of the first device in the chain. Again, the user may utilize the 'C' program to generate the serial bit stream, the program prompting the user for the number of devices to be programmed. The $\overline{SENO}$ and SO (serial out) of the first device should be connected to the $\overline{SENI}$ and SI inputs of the second device respectively and so on, with the $\overline{SENO}$ & SO outputs connecting to the $\overline{SENI}$ & SI inputs of all devices through the chain. All devices in the chain should be connected to a common SCLK. The serial output port of the final device should be monitored by the user. When $\overline{SENO}$ of the final device goes LOW, this indicates that serial programming of all devices has been successfully completed. Upon detection of completion of programming, the user should cease all programming and take $\overline{SENI}$ of the first device in the chain inactive, HIGH.

As mentioned, the first device in the chain has its serial input port controlled by the user, this is the first device to have its internal registers serially loaded by the serial bit stream. When programming of this device is complete it will take its $\overline{SENO}$ output LOW and bypass the serial data loaded on the SI input to its SO output. The serial input of the second device in the chain is now loaded with the data from the SO of the first device, while the second device has its $\overline{SENI}$ input LOW. This process continues through the chain until all devices are programmed and the $\overline{SENO}$ of the final device (or master device, ID = '000') goes LOW.

Once all serial programming has been successfully completed, normal operations, (queue selections on the read and write ports) may begin. When connected in expansion configuration, the IDT72P51339/72P51349/72P51359/72P51369 devices require a total number of serially loaded bits per device to complete serial programming, (SCLK cycles with $\overline{SENI}$ enabled), calculated by: n[19+(Qx72)] where Q is the number of queues the user wishes to setup within the device, where n is the number of devices in the chain.

See Figure 42, *Serial Port Connection* and Figure 43, *Serial Programming* for connection and timing information.

DEFAULT PROGRAMMING

During a Master Reset if the DFM (Default Mode) input is HIGH the multi-queue device will be configured for default programming, (serial programming is not permitted). Default programming provides the user with a simpler, however limited means to setup the multi-queue flow-control device, rather than using the serial programming method. The default mode will configure a multi-queue device with the maximum number of queues setup, and the available memory allocated equally between the queues. The values of the $\overline{PAE}$/$\overline{PAF}$ offsets is determined by the state of the DF (default) pin during a master reset.

For the IDT72P51339/72P51349/72P51359/72P51369 devices the default mode will setup 8 queues, each queue being 512 x 36, 1024 x 36, 2048 x36, and 4096 x 36 deep respectively. For each device, the value of the $\overline{PAE}$/$\overline{PAF}$ offsets is determined at master reset by the state of the DF input. If DF is LOW then both the $\overline{PAE}$ & $\overline{PAF}$ offset will be 8, if HIGH then the value is 128.

When configuring the IDT72P51339/72P51349/72P51359/72P51369 devices in default mode the user simply has to apply WCLK cycles after a master reset, until $\overline{SENO}$ goes LOW, this signals that default programming is complete. These clock cycles are required for the device to load its internal setup registers. When a single multi-queue device is used, the completion of device programming is signaled by the $\overline{SENO}$ output of a device going from HIGH to LOW. Note, that $\overline{SENI}$ must be held LOW when a device is setup for default programming mode.

When multi-queue devices are connected in expansion configuration, the $\overline{SENI}$ of the first device in a chain can be held LOW. The $\overline{SENO}$ of a device should connect to the $\overline{SENI}$ of the next device in the chain. The $\overline{SENO}$ of the final device is used to indicate that default programming of all devices is complete. When the master (ID='000') $\overline{SENO}$ goes LOW normal operations may begin. Again, all devices will be programmed with their maximum number of queues and the memory divided equally between them. Please refer to Figure 38, *Default Programming*.

PARALLEL PROGRAMMING

During a Master Reset cycle (i.e. the $\overline{MRS}$ signal transitions from HIGH to LOW then LOW to HIGH) if the DFM (Default Mode) input signal is HIGH and the QSEL 1 input signal is LOW the Multi-Queue Flow Control device is configured for Parallel Programming. Parallel Programming enables the number of queues within the device to be set through either the Write Address (WRADD) bus or Read Address (RDADD) bus after the Master Reset cycle. Within Parallel Programming mode the Multi-Queue (MQ) device programmable parameters are; number of queues, queue depth, $\overline{PAE}$/$\overline{PAF}$ flag offset value, bus matching and the I/O voltage level. As previously indicated, the number of queues are configured using the write or read address bus, however bus matching is set during the Master Reset cycle. The value that is set during the Master Reset cycle is determined by the Bus Matching (BM) bits. For the IDT72P51339/72P51349/72P51359/72P51369 devices in Parallel Programming Mode the value of the $\overline{PAE}$/$\overline{PAF}$ offsets at master reset is determined by the state of the DF input. If DF is LOW then both the $\overline{PAE}$ & $\overline{PAF}$ offset will be 8, if HIGH then the value is 128.

When configuring the IDT72P51339/72P51349/72P51359/72P51369 devices in Parallel Programming Mode the user simply has to apply WCLK cycles after a master reset, until $\overline{SENO}$ goes LOW, this signals that Parallel Programming is complete. These clock cycles are required for the device to load its internal setup registers. When a single multi-queue device is used, the completion of device programming is signaled by the $\overline{SENO}$ output of a device going from HIGH to LOW. Note, that SENI must be held LOW when a device is setup for Parallel Programming mode.

When Multi-Queue devices are connected in an Expansion Configuration, the $\overline{SENI}$ signal of the first device in a chain must be held LOW. The $\overline{SENO}$ signal of a device should connect to the $\overline{SENI}$ of the next device in the chain. The $\overline{SENO}$ of the final device is used to indicate that the programming of all devices is complete. When the master device (ID='000') $\overline{SENO}$ signal goes LOW the internal programming is complete and queue write/read operation may begin. Please refer to Figure 39, *Parallel Programming* for signal timing details.

PROGRAMMING HIERARCHY

Configuring the device is a 2 stage sequence. The first stage is to set the expansion device type, the desired programming mode and the device operating mode during the master reset cycle (i.e. on the rising edge of Master Reset ($\overline{MRS}$)). The second stage is to set values such as $\overline{PAE}$/$\overline{PAF}$, number of queues, queue depth, etc. using the programming mode (serial, parallel, default) selected in stage 1. Refer to Figure 4, *Device Programming Hierarchy*.

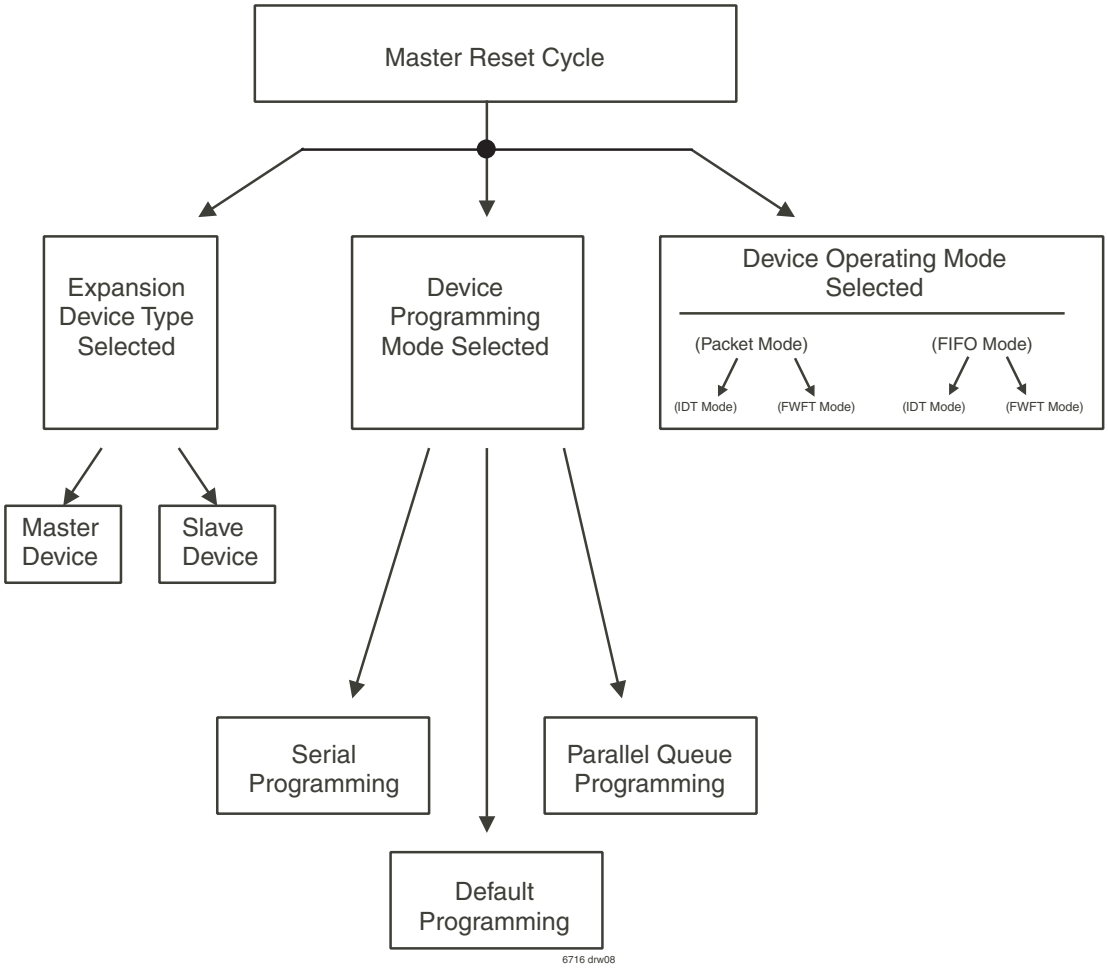


Figure 4. Device Programming Hierarchy

QUEUE DESCRIPTION

CONFIGURATION OF THE IDT MULTI-QUEUE FLOW-CONTROL DEVICE

The IDT72P51339/72P51349/72P51359/72P51369 multi-queue flow-control devices can be configured in distinct modes, namely Packet mode, FIFO mode, Standard mode, and FWFT mode. To configure the device operational mode set the configuration pins (PKT, $\overline{FWFT}$) as indicated in Table 3, Mode Configuration.

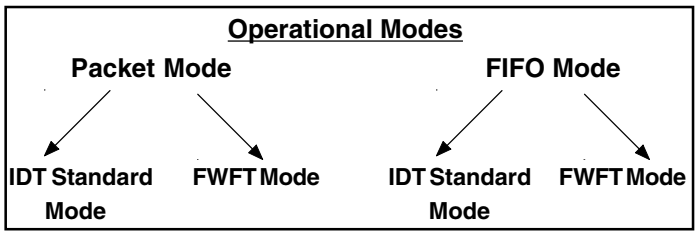


TABLE 3 — MODE CONFIGURATION

Configuration Signals		Modes
PKT	FWFT	
LOW	LOW	FIFO mode - IDT Standard Mode
LOW	HIGH	FIFO mode - FWFT
HIGH	LOW	Packet mode - IDT Standard Mode
HIGH	HIGH	Packet mode - FWFT

In IDT Standard mode the read port signal $\overline{EF}/\overline{OR}$ is configured for empty flag ($\overline{EF}$) signaling. $\overline{EF}$ is an active LOW signal. When $\overline{EF}$ is LOW it signifies the selected (present) queue is empty. On the write port, signal $\overline{FF}/\overline{IR}$ is configured for full flag ($\overline{FF}$) signaling. $\overline{FF}$ is an active LOW signal. When $\overline{FF}$ is LOW it signifies the selected (present) queue is full. Refer to Figure 5, *IDT Standard mode illustrated (Read Port)*.

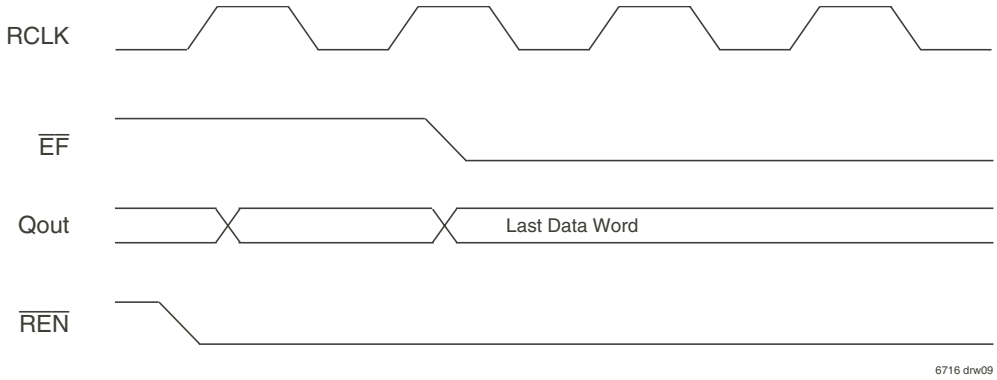


Figure 5. IDT Standard mode illustrated (Read Port)

In FWFT mode the read port signal $\overline{EF}/\overline{OR}$ is configured for output ready ($\overline{OR}$) signaling. $\overline{OR}$ is an active LOW signal. When $\overline{OR}$ is HIGH, it signifies there is no available word to read. On the write port, signal $\overline{FF}/\overline{IR}$ is configured for input ready ($\overline{IR}$) signaling. $\overline{IR}$ is an active LOW signal. When $\overline{IR}$ is LOW it signifies the write port is ready for writing into the selected queue. Refer to Figure 6, *FWFT mode illustrated (Read Port)*.

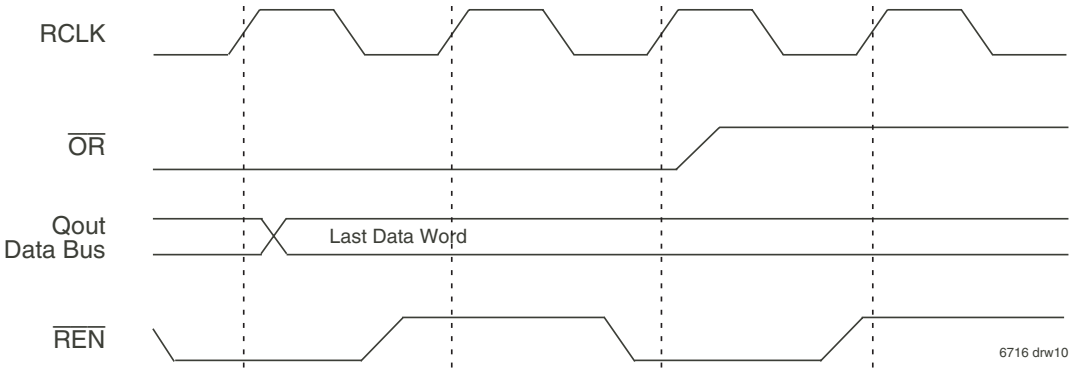


Figure 6. First Word Fall Through (FWFT) mode illustrated (Read Port)