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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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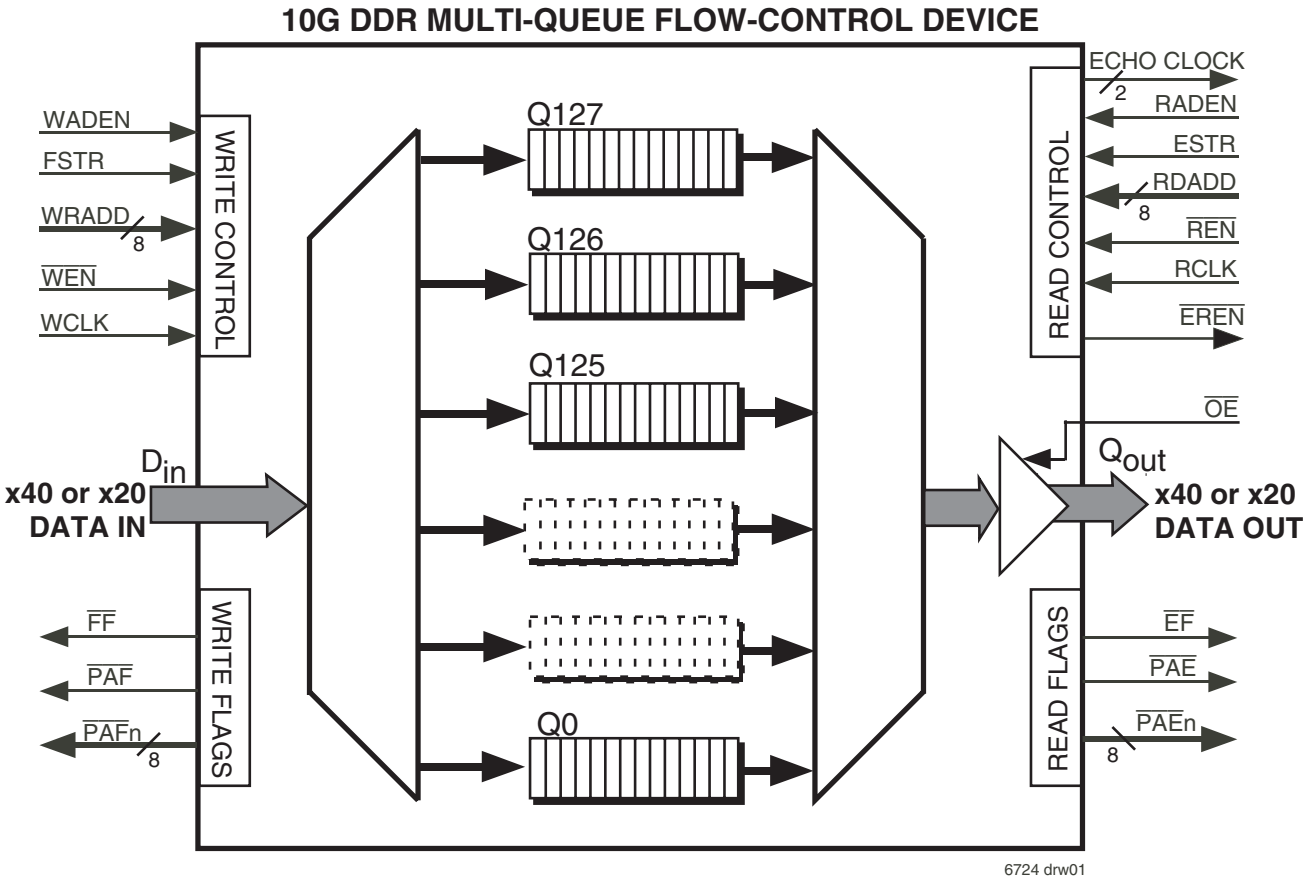
1.8V MULTI-QUEUE FLOW-CONTROL DEVICES
(128 QUEUES) 40 BIT WIDE CONFIGURATION

5,242,880 bits — *IDT72P51767*
10,485,760 bits — *IDT72P51777*

FEATURES

- Choose from among the following memory density options:
  IDT72P51767 — Total Available Memory = 5,242,880 bits
  IDT72P51777 — Total Available Memory = 10,485,760 bits
- Configurable from 1 to 128 Queues
- Multiple default configurations of symmetrical queues
- Default multi-queue device configurations
  – *IDT72P51767: 512 x 40 x 128Q*
  – *IDT72P51777: 1,024 x 40 x 128Q*
- Number of queues and queue sizes may be configured; at master reset, though serial programming, (via the queue address bus)
- 166 MHz High speed operation (6ns cycle time)
- 0.48ns access time
- Independent Read and Write access per queue
- Echo Read Clock available
- Internal PLL
- On-chip Output Impedance matching
- User Selectable Bus Matching Options:
  – *x40 in to x40 out* – *x20 in to x20 out*
  – *x40 in to x20 out* – *x20in to x40out*
- User selectable I/O: 1.5V HSTL or 1.8V eHSTL
- 100% Bus Utilization, Read and Write on every clock cycle
- Selectable Back off one (BOI) or IDT standard mode of operation
- Ability to operate on packet or word boundaries
- Mark and Re-Write operation
- Mark and Re-Read operation
- Individual, Active queue flags ($\overline{EF}$, $\overline{FF}$, $\overline{PAE}$, $\overline{PAF}$)
- 8 bit parallel flag status on both read and write ports
- Direct or polled operation of flag status bus
- Expansion of up to 256 queues
- JTAG Functionality (Boundary Scan)
- Available in a 376-pin BGA, 1mm pitch, 23mm x 23mm
- HIGH Performance submicron CMOS technology
- Industrial temperature range (-40°C to +85°C) is available
- Green parts available, seeing Ordering Information

FUNCTIONAL BLOCK DIAGRAM



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DESCRIPTION

The IDT72P51767/ IDT72P51777 multi-queue flow-control devices are single chip solutions containing up to 128 configurable queues. All queues within the device have a common data input bus, Din [39:0] (write port) and a common data output bus Qout [39:0], (read port). Data written into the write port is directed to a respective queue via an integrated de-multiplex function. Data read from the read port is accessed from a given queue transparently via an internal multiplex operation. Data writes and reads can be performed at high speeds up to 166MHz DDR allowing data rates up to 10Gigabits/s (OC-192). By utilizing high speed interfaces such as 1.5V HSTL, coupled with a x40 bit data bus and 10Mb of data storage, the 10G Multi-Queue can interface with the industry standard 10 Gigabits/sec Media Independent Interface (XGMII) to allow high speed data transmission over 10G Ethernet and SONET line cards. Data write and read operations are totally independent of each other. The Write Clock and Read Clock can operate at independent frequencies. A different queue may be selected on the write port and read port or both ports may select the same queue simultaneously. Multiple clocking schemes are offered for this device as well. The user can utilize either single ended or differential clocking for DDR read operations. DDR write operation utilize a single ended clock. SDR write and read operations utilize a single ended clock.

The devices provide Full flag and Empty flag status for the queue selected for write and read operations respectively. Also a Programmable Almost Full ($\overline{PAF}$) and Programmable Almost Empty ($\overline{PAE}$) flag for each queue is provided. Two 8 bit programmable flag busses ($\overline{PAF}$n, $\overline{PAE}$n) are available, providing status of queues that are not the present queue selected for write or read operations. When 8 or fewer queues are configured in the device, these flag busses provide an individual flag per queue, when more than 8 queues are used; the queue status is multiplexed through the 8 stus lines. The multiplexing can be configured either a Polled or Direct mode of bus.

Bus Matching is available on this device; either port can be x20 bits or x40 bits wide. When Bus Matching is used the device ensures the logical transfer of data throughput.. With a 40 data bits configuration parity checking and packet tagging is achievable if desired. Parity checking is available through the use of 4 user selectable bits as part of the 40 bit word. The user will be able to pass along parity bits through the Multi-Queue to use for error detection in a up/down stream device. The Multi-Queue device does not provide parity checking circuits.

In Back off One mode, the user can switch queues without having to read the last pipelined data word that is stored in the output register which in IDT standard mode is required to be read out during a queue switch . The last pipelined data word in BOI mode is retained in the output data register until it is actively read.

A Mark and Re-write and a Mark and Re-read function are available on the write and read ports respectively. These functions allows for a mark location to be independently issued on the read and/or write ports, in their respective queues. The option to reset a given queue to the mark location effectively dropping data written into the queue or allow data to be read again from the device.

The devices offer a default configuration upon reset, offering 128 symmetrical queues configured at start-up, which means the user can program the number of queues to divide the 10Mb/5Mb of memory depending on the device. The Multi-Queues can even be programmed to support one single queue to be used as a FIFO for high performance applications of sequential queuing. The programmable flag positions are also user programmable. If the user does not wish to program the multi-queue device, a default option is available that configures the device in a predetermined manner. A Master Reset latches in all configuration setup pins and must be performed before programming of the device can take place.

The multi-queue flow-control devices have the capability of operating its I/O in either 1.5V HSTL , or 1.8V eHSTL mode. The type of I/O is selected via the IOSEL input. The core supply voltage (VCC) to the multi-queue is always 1.8V, however the output levels can be set independently via a separate supply, VDDQ. The package used will be a 23mm x 23mm, BB-376 BGA package for better noise immunity and ground bounce prevention.

A JTAG test port is provided, here the multi-queue flow-control device has a fully functional Boundary Scan feature, compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture.

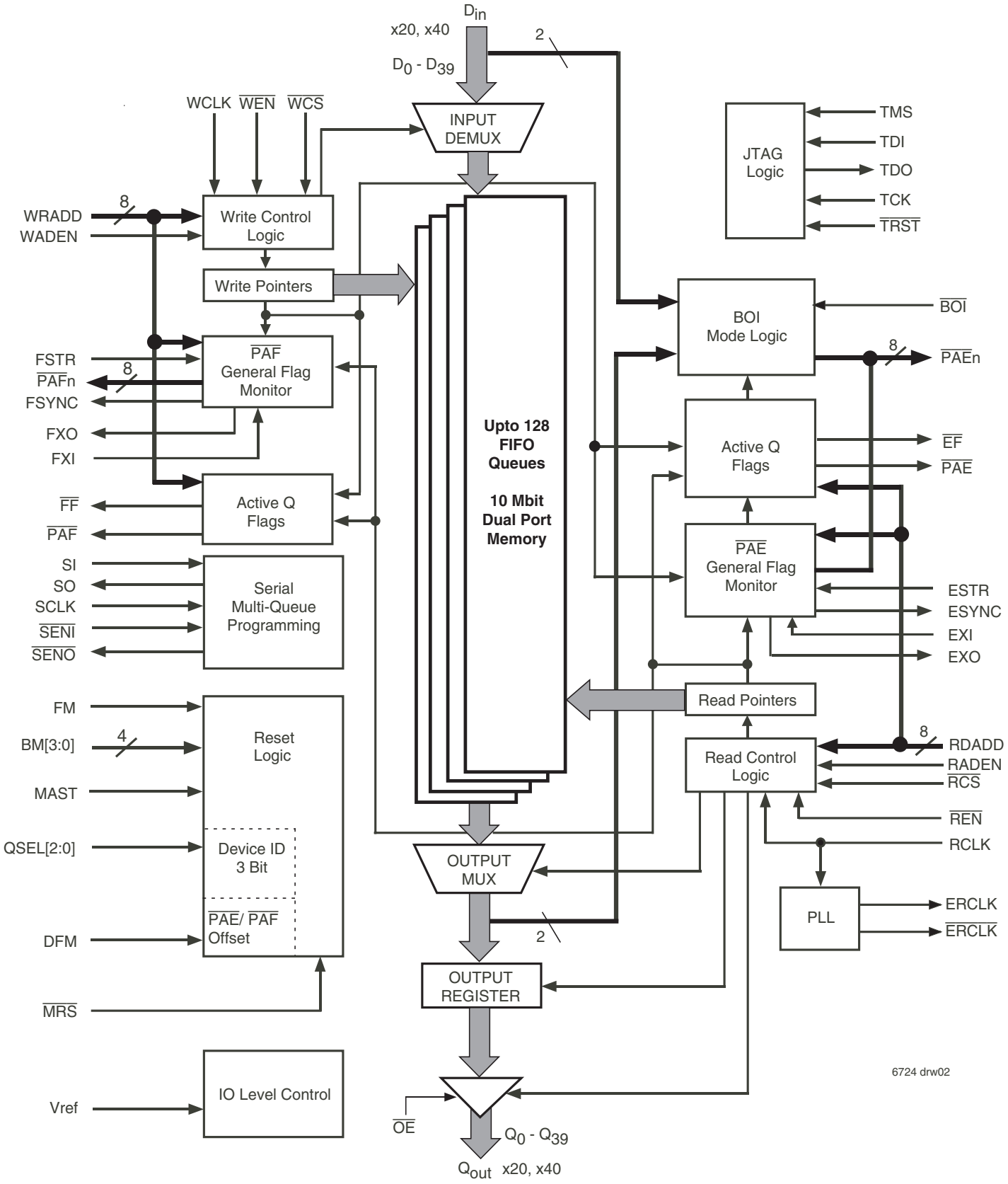
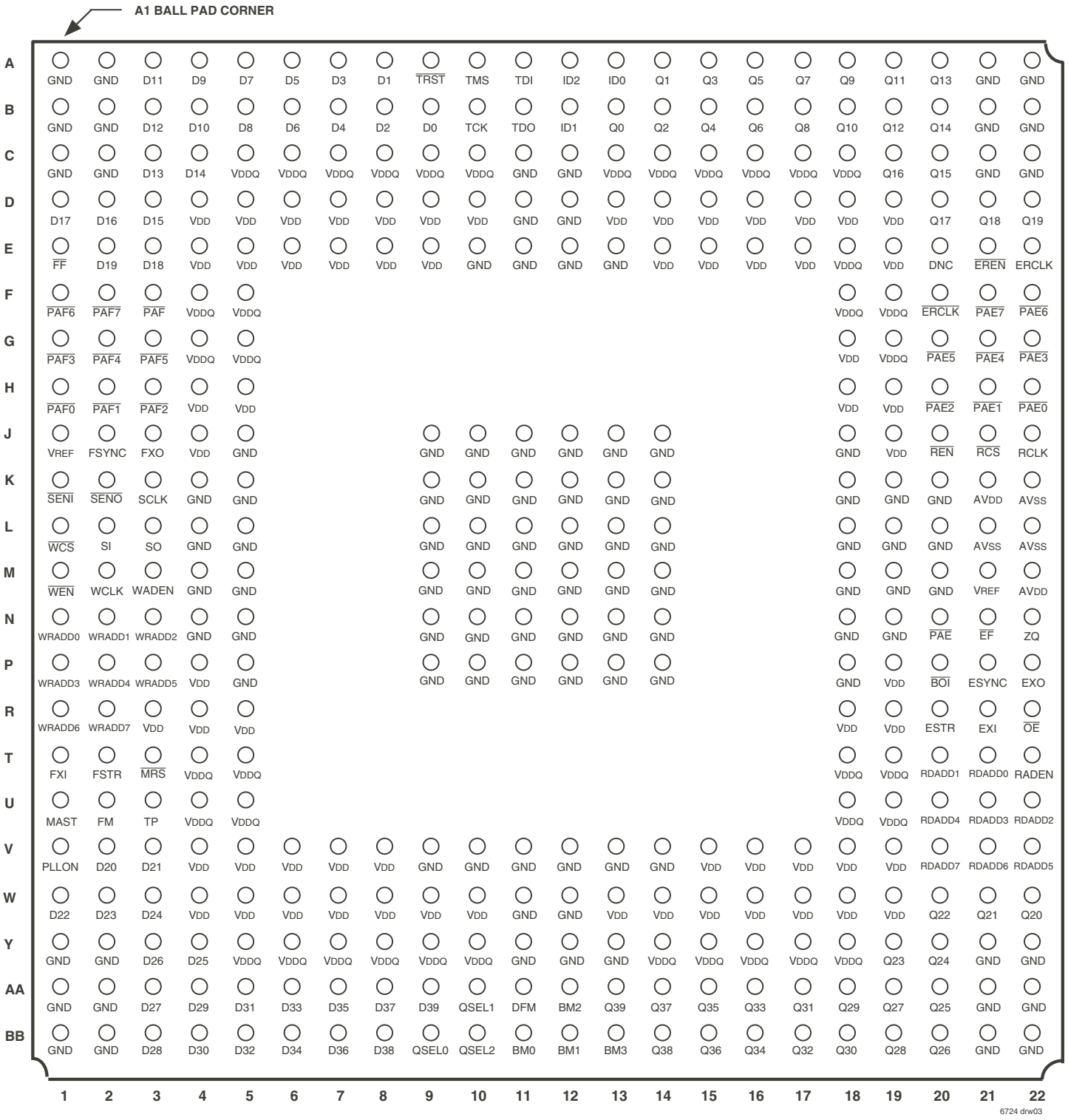


Figure 1. Multi-Queue Flow-Control Device Block Diagram

PIN CONFIGURATION



NOTE:
1. DNC - Do Not Connect.

PBGA (BB376-1, order code: BB)
TOP VIEW

DETAILED DESCRIPTION

MULTI-QUEUE STRUCTURE

The IDT multi-queue flow-control device has a single data input port and single data output port with up to 128 FIFO queues in parallel buffering between the two ports. The user can setup between 1 and 128 Queues within the device. These queues can be configured to utilize the total available memory, providing the user with full flexibility and ability to configure the queues to be various depths, independent of one another.

MEMORY ORGANIZATION/ ALLOCATION

The memory is organized into what is known as "blocks", each block being 256 x40 bits. When the user is configuring the number of queues and individual queue sizes the user must allocate the memory to respective queues, in units of blocks, that is, a single queue can be made up from 0 to m blocks, where m is the total number of blocks available within a device. Also the total size of any given queue must be in increments of 256 x40. For the IDT72P51767 and IDT72P51777 the Total Available Memory is 1024 and 512 blocks respectively (a block being 256 x40). Queues can be built from these blocks to make any size queue desired and any number of queues desired.

BUS WIDTHS

The input port is common to all queues within the device, as is the output port. The device provides the user with Bus Matching options such that the input port and output port can be either x20, x40 bits wide, the read and write port widths can be set independently of one another. Because a ports are common to all queues the width of the queues is not individually set. The input width of all queues are the same and the output width of all queues are the same.

WRITING TO & READING FROM THE MULTI-QUEUE

Data being written into the device via the input port is directed to a discrete queue via the write queue address input. Conversely, data being read from the device read port is read from a queue selected via the read queue address input. Data can be simultaneously written into and read from the same queue or different queues. Once a queue is selected for data writes or reads, the writing and reading operation is performed in the same manner as a conventional IDT synchronous FIFO, utilizing clocks and enables, there is a single clock and enable per port. When a specific queue is addressed on the write port, data placed on the data inputs is written to that queue sequentially based on the rising edge of a write clock provided setup and hold times are met. Conversely, data is read on to the output port after an access time from a rising edge on a read clock.

The operation of the write port is comparable to the function of a conventional FIFO operating in standard IDT mode. Write operations can be performed on the write port provided that the queue currently selected is not full, a full flag output provides status of the selected queue. When a queue is selected on the output port, the next word in that queue will be available for reading on the output register. All subsequent words from that queue require an enabled read cycle. Data cannot be read from a selected queue if that queue is empty, the read port provides an Empty flag indicating when data read out is valid. If the user switches to a queue that is empty, the last word from the previous queue will remain on the output bus. The device can operate in IDT Standard mode or $\overline{\text{BOI}}$ mode. In IDT Standard mode the read port provides a word to the output bus (Qout) for each clock cycle that $\overline{\text{REN}}$ is asserted. Refer to Figure 46, *SDR Read Queue Select, Read Operation (IDT Mode)*.

As mentioned, the write port has a full flag, providing full status of the selected queue. Along with the full flag a dedicated almost full flag is provided, this almost full flag is similar to the almost full flag of a conventional IDT FIFO. The device provides a user programmable almost full flag for all 128 queues and when a respective queue is selected on the write port, the almost full flag provides status for that queue. Conversely, the read port has an Empty flag, providing status of the data being read from the queue selected on the read port. As well as the Empty flag the device provides a dedicated almost empty flag. This almost empty flag is similar to the almost empty flag of a conventional IDT FIFO. The device provides a user programmable almost empty flag for each 128 queues and when a respective queue is selected on the read port, the almost empty flag provides status for that queue.

PROGRAMMABLE FLAG BUSSES

In addition to these dedicated flags, full & almost full on the write port and Output Ready & almost empty on the read port, there are two flag status busses. An almost full flag status bus is provided, this bus is 8 bits wide. Also, an almost empty flag status bus is provided, again this bus is 8 bits wide. The purpose of these flag busses is to provide the user with a means by which to monitor the data levels within queues that may not be selected on the write or read port. As mentioned, the device provides almost full and almost empty registers (programmable by the user) for each of the 128 queues in the device.

In the IDT72P51767/72P51777 multi-queue flow-control devices the user has the option of utilizing 1 to 128 queues, therefore the 8 bit flag status busses are multiplexed between the 128 queues, a flag bus can only provide status for 8 of the 128 queues at any moment, this is referred to as a "Status Word", such that when the bus is providing status of queues 1 through 8, this is status word 1, when it is queues 9 through 16, this is status word 2 and so on up to status word 16. If less than 128 queues are setup in the device, there are still 4 status words, such that in "Polled" mode of operation the flag bus will still cycle through 4 status words. If for example only 22 queues are setup, status words 1 and 2 will reflect status of queues 1 through 8 and 9 through 16 respectively. Status word 3 will reflect the status of queues 17 through 22 on the least significant 6 bits, the most significant 2 bits of the flag bus are don't care. The remaining status words are not used as there are no queues to report.

The flag busses are available in two user selectable modes of operation, "Polled" or "Direct". When operating in polled mode a flag bus provides status of each status word sequentially, that is, on each rising edge of a clock the flag bus is updated to show the status of each status word in order. The rising edge of the write clock will update the almost full bus and a rising edge on the read clock will update the almost empty bus. The mode of operation is always the same for both the almost full and almost empty flag busses. When operating in direct mode, the status word on the flag bus is selected by the user. So the user can actually address the status word to be placed on the flag status busses, these flag busses operate independently of one another. Addressing of the almost full flag bus is done via the write port and addressing of the almost empty flag bus is done via the read port.

EXPANSION

Expansion of multi-queue devices is possible. Expansion achieves either depth or queue expansion. Depth Expansion means expanding the depths of individual queues. Queue expansion means increasing the total number of queues available. Depth expansion is possible by virtue of the fact that more memory blocks within a multi-queue device can be allocated to a fewer number of queues to increase the depth of each queue. For example, depth expansion of 2 devices provides the possibility of 2 queues, each queue being setup within a single device utilizing all memory blocks available to produce a single queue. This is the deepest queue that can setup within a device.

For queue expansion a maximum number of 256 queues (2 x 128 queues) may be setup. If fewer queues are desired, then more memory blocks will be available to increase queue depths if desired. Refer to Figure 61, *Connecting two 10G Multi-Queue 128Q devices in Expansion Mode*, and Figure 62,

Connecting three or more 10G Multi-Queue 128Q in Expansion mode using WRADD bit 7 / RDADD bit 7 for device connection details.

10Gbps MULTI-QUEUE DIFFERENCES FROM THE 4M MULTI-QUEUE

The 10G Multi-Queue was developed to support very high performance applications that needed 10Gb/s of bandwidth, and the flexibility of buffering packets of information in large bursts such as Jumbo Ethernet packets that can be as large as 9KBs. Listed below are the differences between the 10G Multi-Queue and the previous 4M Multi-Queue with descriptions of the enhancements made to support performance functions in queuing.

PERFORMANCE ENHANCEMENTS

- 333.34 Mbps (per pin) High speed data rate in DDR mode
- x40 Din and x40 Qout (8 more pins for user selectable operation such as parity check or packet tagging)
- Electrical compatibility to 802.3ae XGMII specification for passive interconnection to Ethernet devices.
  - Single clocking in DDR and SDR, PLL on/off Mode. (PAD_PLLON pin) allowing data latency to be the same for SDR and DDR.
- Burst of 2 timing and interface logic
  - Output impedance matching for signal quality on the output pins.
  - More Data latency (same cycle on write, 1 cycle on read)
  - Three "echo" output pins: ERCLK, $\overline{\text{ERCLK}}$, and $\overline{\text{EREN}}$ used for Source Synchronous data on the output. Data can be center aligned on the Echo Clock or issued on the rising edge of the Echo Clock.
  - Access Time (Ta) reduced to 0.48ns with Echo Clock used for faster Synchronized data delivery down stream

USER FLEXIBILITY IMPROVEMENTS

- 10Mbits of storage and queuing density for support large packet frames such as Jumbo Ethernet
- During a Queue switch, BOI mode preserves the data word in the output register until it's read.
- "Real Time" Flags, for both DDR and SDR.
  - $\overline{\text{PAF}}$/$\overline{\text{PAE}}$ have 1 more cycle (WCLK/RCLK) latency (3 vs. 2)
  - Tskew of $\overline{\text{EF}}$/$\overline{\text{PAE}}$ with respect to WCLK has 1 WCLK cycle delay.
  - Tskew of $\overline{\text{FF}}$/$\overline{\text{PAF}}$ with respect to RCLK has 1 RCLK cycle delay.
- Programmable Default configuration of 128, 64, 32, 16, 8 or 4 symmetrical queues are available using DFM, QSEL[2:0] pins
- User selectable I/O: 1.5V HSTL, or 1.8V eHSTL for faster switching I/O
- Expansion of up to 256 queues and/or 80Mbit logical configuration using up to 8 multi-queue devices
- Default flag offset value is defined according to bus matching configuration
  - The $\overline{\text{PAE}}$ flag can be used as a packet indicator

TABLE 1 — SUMMARY OF THE DIFFERENCES BETWEEN THE 4M MQ AND 10G MQ

FEATURE	4M MQ (IDT72P51769)	10M MQ (IDT72P51777)
Data Transfer Modes	SDR	SDR, DDR
Bus Width	x36, x18, x9	x40, x20
XGMII Compatibility	no	yes
Access time (ta)	3.6 ns max	0.48ns max
Data Storage Capacity	4Mb	10Mb
Data Throughput	7.2Gbps	10Gbps
Operating Frequency	200mhz	166mhz
Configurable Queues	Up to 128	Up to 128
Package	256 pin PBGA	376 pin BGA
Output Impedance Technology	no	yes
I/O Voltages	1.5V,1.8V, 2.5V	1.5V,1.8V
Echo read Clock	no	yes
Modes of Operation	FWFT, IDT, Packet	IDT, BOI
Output data Clocking	Edge aligned	Centered aligned

PIN DESCRIPTIONS

Symbol & (Pin No.)	Name	I/O TYPE	Description
BM [3:0] (BM3-BB13 BM2-AA12 BM1-BB12 BM0-BB11)	Bus Matching	1.8V LVTTL INPUT	These pins define the bus width and data transfer rate (DDR/SDR) of the input write port and the output read port of the device. The bus widths/data rates are set during a Master Rest cycle. The BM[3:0] signals must meet the setup and hold time requirements of Master Reset and must not toggle/change state after a Master Reset cycle.
$\overline{BOI}$ (P20)	Back Off One Mode	HSTL INPUT	When in BOI, data is back-off one position in which Packet 1 and Packet 2 are out again during second Queue Switch. See section on 10Gbps Multi-queue Differences from the 4M multi-queue, previous page.
D[39:0] (See Pin No. table for details)	Data Input Bus	HSTL INPUT	These are the 32 data input pins. Data is written into the device via these input pins on the rising edge of WCLK provided that $\overline{WEN}$ is LOW. Any unused data input pins should be tied HIGH. D[39:36] user definable input bits D[33] user definableD[32] user definableD[31:0] data input bits
DFM (AA11)	Default Mode	1.8V LVTTL INPUT	The 10G multi-queue device requires programming after master reset. The user can do this serially via the serial port, or the user can use the default method. If DFM is LOW at Master Reset then serial mode will be selected, if DFM is HIGH then default mode is selected.
$\overline{EF}$ (N21)	Empty Flag	HSTL OUTPUT	The Empty Flag ($\overline{EF}$) provides valid status for the selected queue. The Empty Flag indicates the selected queue is empty, all words have been read. This flag is delayed to match the data output path delay.
ERCLK (E22)	Echo Read Clock	HSTL OUTPUT	The rising edge of this clock is centered aligned with Qout data.
$\overline{ERCLK}$ (F20)	Echo Read Clock	HSTL OUTPUT	Read Clock Echo is the inverse of ERCLK.
$\overline{EREN}$ (E21)	Echo Read Enable	HSTL OUTPUT	Echo Read Enable output, used in conjunction with ERCLK and $\overline{ERCLK}$.
ESTR (R20)	$\overline{PAE}$n Flag Bus	HSTL INPUT	If direct operation of the $\overline{PAE}$n bus has been selected, the ESTR input is used in conjunction with RCLK and the RDADD bus to select a quadrant of queues to be placed on to $\overline{PAE}$n output. A quadrant addressed via the RDADD bus is selected on the rising edge of RCLK provided that ESTR is HIGH. If Polled operation has been selected, ESTR should be tied inactive, LOW. Note, that a $\overline{PAE}$n flag bus selection cannot be made, (ESTR must NOT go active) until programming of the part has been completed and SENO has gone LOW.
ESYNC (P21)	$\overline{PAE}$n Bus Sync	HSTL OUTPUT	ESYNC is an output from the multi-queue device that provides a synchronizing pulse for the $\overline{PAE}$n bus during Polled operation of the $\overline{PAE}$n bus. During Polled operation each quadrant of queue status flags is loaded on to the $\overline{PAE}$n bus outputs sequentially based on RCLK. The first RCLK rising edge loads quadrant 1 on to $\overline{PAE}$n, the second RCLK rising edge loads quadrant 2 and so on. The fifth RCLK rising edge will again load quadrant 1. During the RCLK cycle that quadrant 1 of a selected device is placed on to the $\overline{PAE}$n bus, the ESYNC output will be HIGH. For all other quadrants of that device, the ESYNC output will be LOW.
EXI (R21)	$\overline{PAE}$n Bus Expansion In	HSTL INPUT	The EXI input is used when multi-queue devices are connected in expansion mode and Polled $\overline{PAE}$n bus operation has been selected. EXI of device 'N' connects directly to EXO of device 'N-1'. The EXI receives a token from the previous device in a chain. In single device mode the EXI input must be tied LOW if the $\overline{PAE}$n bus is operated in direct mode. If the $\overline{PAE}$n bus is operated in polled mode the EXI input must be connected to the EXO output of the same device. In expansion mode the EXI of the first device should be tied LOW, when direct mode is selected.
EXO (P22)	$\overline{PAE}$n Bus Expansion Out	HSTL OUTPUT	EXO is an output that is used when multi-queue devices are connected in expansion mode and Polled $\overline{PAE}$n bus operation has been selected. EXO of device 'N' connects directly to EXI of device 'N+1'. This pin pulses when device N has placed its final (4th) quadrant on to the $\overline{PAE}$n bus with respect to RCLK. This pulse (token) is then passed on to the next device in the chain 'N+1' and on the next RCLK rising edge the first quadrant of device N+1 will be loaded on to the $\overline{PAE}$n bus. This continues through the chain and EXO of the last device is then looped back to EXI of the first device. The ESYNC output of each device in the chain provides synchronization to the user of this looping event.
$\overline{FF}$ (E1)	Full Flag	HSTL OUTPUT	This pin provides the full flag output for the active Queue, that is, the queue selected on the input port for write operations, (selected via WCLK, WRADD bus and WADEN). On the WCLK cycle after a queue selection, this flag will show the status of the newly selected queue. Data can be written to this queue provided $\overline{FF}$ is HIGH. This flag has High-Impedance capability, this is important during expansion of

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
$\overline{FF}$ (Continued) (E1)	Full Flag	HSTL OUTPUT	devices, when the $\overline{FF}$ flag output of up to 8 devices may be connected together on a common line. The device with a queue selected takes control of the $\overline{FF}$ bus, all other devices place their $\overline{FF}$ output into High-Impedance. When a queue selection is made on the write port this output will switch from High-Impedance control on the next WCLK cycle. This flag is asserted synchronous to WCLK.
FM (U2)	Flag Mode	1.8V LVTTL INPUT	This pin is setup before a Master Reset and must not toggle during any device operation. The state of the FM pin during Master Reset will determine whether the $\overline{PAF}$n and $\overline{PAE}$n flag busses operate in either Polled or Direct mode. If FM is HIGH, Polled mode is selected, if FM LOW, Direct mode is selected.
FSTR (T2)	$\overline{PAF}$n Flag Bus Strobe	HSTL INPUT	If direct mode for the $\overline{PAF}$n bus has been selected, the FSTR input is used in conjunction with WCLK and the WRADD bus to select a quadrant of queues to be placed on to the $\overline{PAF}$n bus outputs. A quadrant addressed via the WRADD bus is selected on the rising edge of WCLK provided that FSTR is HIGH. If polled operations has been selected, FSTR should be tied inactive, LOW. Note, that a $\overline{PAF}$n flag bus selection cannot be made, (FSTR must NOT go active) until programming of the part has been completed and SENO has gone LOW.
FSYNC (J2)	$\overline{PAF}$n Bus Sync	HSTL OUTPUT	FSYNC is an output from the multi-queue device that provides a synchronizing pulse for the $\overline{PAF}$n bus during Polled operation of the $\overline{PAF}$n bus. During Polled operation each quadrant of queue status flags is loaded on to the $\overline{PAF}$n bus outputs sequentially based on WCLK. The first WCLK rising edge loads quadrant 1 on to $\overline{PAF}$n, the second WCLK rising edge loads quadrant 2 and so on. The fifth WCLK rising edge will again load quadrant 1 queue status flags. During the WCLK cycle that quadrant 1 of a selected device is placed on to the $\overline{PAF}$n bus, the FSYNC output will be HIGH. For all other quadrants of that device, the FSYNC output will be LOW.
FXI (T1)	$\overline{PAF}$n Bus Expansion In	HSTL INPUT	The FXI input is used when multi-queue devices are connected in expansion mode and Polled $\overline{PAF}$n bus operation has been selected . FXI of device 'N' connects directly to FXO of device 'N-1'. The FXI receives a token from the previous device in a chain. In single device mode the FXI input must be tied LOW if the $\overline{PAF}$n bus is operated in direct mode. If the $\overline{PAF}$n bus is operated in polled mode the FXI input must be connected to the FXO output of the same device. In expansion mode the FXI of the first device should be tied LOW, when direct mode is selected.
FXO (J3)	$\overline{PAF}$n Bus Expansion Out	HSTL OUTPUT	FXO is an output that is used when multi-queue devices are connected in expansion mode and Polled $\overline{PAF}$n bus operation has been selected . FXO of device 'N' connects directly to FXI of device 'N+1'. This pin pulses when device N has placed its final (4th) quadrant on to the $\overline{PAF}$n bus with respect to WCLK. This pulse (token) is then passed on to the next device in the chain 'N+1' and on the next WCLK rising edge the first quadrant of device N+1 will be loaded on to the $\overline{PAF}$n bus. This continues through the chain and FXO of the last device is then looped back to FXI of the first device. The FSYNC output of each device in the chain provides synchronization to the user of this looping event.
ID[2:0] (ID2-A12 ID1-B12 ID0-A13)	Device ID Pins	1.8V LVTTL INPUT	The ID[2:0] pins are used to uniquely address individual devices when multiple Multi-Queue devices are connected in expansion mode. Addressing devices in expansion mode requires matching WRADD/ RDADD address bits with the address that is assigned to each device by the ID[2:0] pins. During write/ read operations the WRADD/RDADD address are compared to the device ID [2:0] value. Note: expansion mode supports a maximum 256 queues, regardless of the number of devices used in expansion mode. The first device in a chain of multi-queue's (connected in expansion mode), may be setup as '000', the second as '001". In single device mode the ID[2:0] pins should be setup as '0xx' and the MSb (bit 7) of the WRADD and RDADD address busses should be zero. The ID[2:0] inputs setup a respective device ID during Master Reset. These ID pins must not toggle during any device operation. Note, the device selected as the 'Master' does not have to have the ID of '000'.
MAST (U1)	Master Device	1.8V LVTTL INPUT	The state of this input at Master Reset determines whether a given device (within a chain of devices), is the Master device or a Slave. If this pin is HIGH, the device is the master if it is LOW then it is a Slave. The master device is the first to take control of all outputs after a Master Reset, all slave devices go to High-Impedance, preventing bus contention. If a multi-queue device is being used in single device mode, this pin must be set HIGH.
$\overline{MRS}$ (T3)	Master Reset	HSTL INPUT	The Master Reset is used to configure the device. To configure the device configuration signals must be asserted that meet the setup time and hold time requirements of a Master Reset cycle. Transitioning $\overline{MRS}$ from HIGH to LOW then LOW to HIGH performs a complete Master Reset cycle. Note, additional device programming is required after master reset.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
$\overline{OE}$ (R22)	Output Enable	HSTL INPUT	The Output Enable signal is the three-state control of the multi-queue data output bus Q[39:0], Qout. If a device has been configured as a "Master" device, the Qout data outputs will be in a low impedance condition if the $\overline{OE}$ input is LOW. If $\overline{OE}$ is HIGH then the Qout data outputs will be in high impedance. If a device is configured a "Slave" device, then the Qout data outputs will always be in high impedance until that device has been selected on the Read Port, at which point $\overline{OE}$ provides three-state of that respective device.
$\overline{PAE}$ (N20)	Programmable Almost-Empty Flag	HSTL OUTPUT	This pin provides the Almost-Empty flag status for the Queue that has been selected on the output port for read operations, (selected via RCLK, RDADD and RADEN). This pin is LOW when the selected Queue is almost-empty. This flag output may be duplicated on one of the $\overline{PAE}$n bus lines. This flag is synchronized to RCLK.
$\overline{PAE}$n[7:0] ($\overline{PAE}$7-F21 $\overline{PAE}$6-F22 $\overline{PAE}$5-G20 $\overline{PAE}$4-G21 $\overline{PAE}$3-G22 $\overline{PAE}$2-H20 $\overline{PAE}$1-H21 $\overline{PAE}$0-H22)	Programmable Flag Bus	HSTL OUTPUT	The $\overline{PAE}$n bus is 8 bits wide. During a Master Reset this bus is setup for Almost Empty configuration. This output bus provides $\overline{PAE}$ status of 8 queues (1 quadrant), within a selected device. During Queue read/write operations these outputs provide programmable empty flag status or packet data available status, in either polled or direct mode. The mode of flag operation is determined during master reset via the state of the FM input. This flag bus is capable of High-Impedance state, this is important during expansion of multi-queue devices. During direct operation the $\overline{PAE}$n bus is updated to show the $\overline{PAE}$ status of a quadrant of queues within a selected device. Selection is made using RCLK, ESTR and RDADD. During Polled operation the $\overline{PAE}$n bus is loaded with the $\overline{PAE}$ status of multi-queue flow-control quadrants sequentially based on the rising edge of RCLK.
$\overline{PAF}$ (F3)	Programmable Almost–Full Flag	HSTL OUTPUT	This pin provides the Almost-Full flag status for the Queue that has been selected on the input port for write operations, (selected via WCLK, WRADD and WADEN). This pin is LOW when the selected Queue is almost-full. This flag output may be duplicated on one of the $\overline{PAF}$n bus lines. The $\overline{PAE}$ flag is asserted synchronous to WCLK.
$\overline{PAF}$n[7:0] ($\overline{PAF}$7-F2 $\overline{PAF}$6-F1 $\overline{PAF}$5-G3 $\overline{PAF}$4-G2 $\overline{PAF}$3-G1 $\overline{PAF}$2-H3 $\overline{PAF}$1-H2 $\overline{PAF}$0-H1)	Programmable Almost-Full Flag Bus	HSTL OUTPUT	The $\overline{PAF}$n bus is 8 bits wide. At any one time this output bus provides $\overline{PAF}$ status of 8 queues (1 quadrant), within a selected device. During Queue read/write operations these outputs provide programmable full flag status, in either direct or polled mode. The mode of flag operation is determined during master reset via the state of the FM input. This flag bus is capable of High-Impedance state, this is important during expansion of multi-queue devices. During direct operation the $\overline{PAF}$n bus is updated to show the $\overline{PAF}$ status of a quadrant of queues within a selected device. Selection is made using WCLK, FSTR, WRADD and WADEN. During Polled operation the $\overline{PAF}$n bus is loaded with the $\overline{PAF}$ status of multi-queue flow-control quadrants sequentially based on the rising edge of WCLK.
PLL ON (V1)	PLL ON	HSTL INPUT	This pin is used to enable the PLL. When PLL is activated, data will be clocked out by PLL generated clock.
Q[39:0](Qout) (See Pin No. table for details)	Data Output Bus	HSTL OUTPUT	These are the 40 data output pins. Data is read out of the device via these output pins on the rising edge of RCLK provided that $\overline{REN}$ is LOW, $\overline{OE}$ is LOW and the Queue is selected. Due to bus-matching not all outputs may be used, any unused outputs should not be connected.
QSEL[2:0] (QSEL2-BB10 QSEL1-AA10 QSEL0-BB9)	Queue Select	1.8V LVTTL INPUT	The QSEL pins provides various queue programming options. Refer to Table 10, Write Queue Switch Operation for details.
RADEN (T22)	Read Address Enable	HSTL INPUT	The RADEN input is used in conjunction with RCLK and the RDADD address bus to select a queue to be read from. A queue addressed via the RDADD bus is selected on the rising edge of RCLK provided that RADEN is HIGH. RADEN should be asserted (HIGH) only during a queue change cycle(s). RADEN should not be permanently tied HIGH. RADEN cannot be HIGH for the same RCLK cycle as ESTR. Note, that a read queue selection cannot be made, (RADEN must NOT go active) until programming of the part has been completed and SENO has gone LOW.
RCLK (J22)	Read Clock	HSTL INPUT	When enabled by $\overline{REN}$, the rising edge of RCLK reads data from the selected queue via the output bus Qout. The queue to be read is selected via the RDADD address bus and a rising edge of RCLK while RADEN is HIGH. A rising edge of RCLK in conjunction with ESTR and RDADD will also select the $\overline{PAE}$n flag quadrant to be placed on the $\overline{PAE}$n bus during direct flag operation. During polled flag operation the $\overline{PAE}$n bus is cycled with respect to RCLK and the ESYNC signal is synchronized to RCLK. The $\overline{PAE}$, and

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
RCLK (Cont'd) (J22)	Read Clock	HSTL INPUT	$\overline{EF}$ outputs are all synchronized to RCLK. During device expansion the EXO and EXI signals are based on RCLK. RCLK must be continuous and free-running.
$\overline{RCS}$ (J21)	Read Chip Select	HSTL INPUT	The $\overline{RCS}$ signal in concert with $\overline{REN}$ signal provides control to enable data on to the output read data bus. During a Master Reset cycle the $\overline{RCS}$ it is don't care signal.
RDADD[7:0] (RDADD7-V20 RDADD6-V21 RDADD5-V22 RDADD4-U20 RDADD3-U21 RDADD2-U22 RDADD1-T20 RDADD0-T21)	Read Address Bus	HSTL INPUT	For the 128Q device the RDADD bus is 8 bits. The RDADD bus is a dual purpose address bus. The first function of RDADD is to select a Queue to be read from. The least significant 5 bits of the bus, RDADD[4:0] are used to address 1 of 128 possible queues within a multi-queue device. The most significant 3 bits, RDADD[7:5] are used to select 1 of 8 possible multi-queue devices that may be connected in expansion mode. These 3 MSB's will address a device with the matching ID code. (See ID[2:0] description for more detail on matching ID code. The second function of the RDADD bus is to select the quadrant of queues to be loaded on to the $\overline{PAE}$n bus during strobed flag mode. The least significant 4 bits, RDADD[3:0] are used to select the quadrant of a device to be placed on the $\overline{PAE}$n bus. The most significant 3 bits, RDADD[7:5] are again used to select 1 of 8 possible multi-queue devices that may be connected in expansion mode. Address bit RDADD[4] is don't care during quadrant selection.
$\overline{REN}$ (J20)	Read Enable	HSTL INPUT	The $\overline{REN}$ input enables read operations from a selected Queue based on a rising edge of RCLK. A queue to be read from can be selected via RCLK, RADEN and the RDADD address bus regardless of the state of $\overline{REN}$. Data from a newly selected queue will be available on the Qout output bus on the second RCLK cycle after queue selection regardless of $\overline{REN}$. A read enable is not required to cycle the $\overline{PAE}$n bus (in polled mode) or to select the $\overline{PAE}$n quadrant , (in direct mode).
SCLK (K3)	Serial Clock	HSTL INPUT	If serial programming of the multi-queue device has been selected during master reset, the SCLK input clocks the serial data through the multi-queue device. Data setup on the SI input is loaded into the device on the rising edge of SCLK provided that SENI is enabled, LOW. When expansion of devices is performed the SCLK of all devices should be connected to the same source.
SENI (K1)	Serial Input Enable	HSTL INPUT	During serial programming of a multi-queue device, data loaded onto the SI input will be clocked into the part (via a rising edge of SCLK), provided the SENI input of that device is LOW. If multiple devices are cascaded, the SENI input should be connected to the SENO output of the previous device. So when serial loading of a given device is complete, its SENO output goes LOW, allowing the next device in the chain to be programmed (SENO will follow SENI of a given device once that device is programmed). The SENI input of the master device (or single device), should be controlled by the user.
SENO (K2)	Serial Output Enable	HSTL OUTPUT	This output is used to indicate that serial programming or default programming of the multi-queue device has been completed. SENO follows SENI once programming of a device is complete. Therefore, SENO will go LOW after programming provided SENI is LOW, once SENI is taken HIGH again, SENO will also go HIGH. When the SENO output goes LOW, the device is ready to begin normal read/write operations. If multiple devices are cascaded and serial programming of the devices will be used, the SENO output should be connected to the SENI input of the next device in the chain. When serial programming of the first device is complete, SENO will go LOW, thereby taking the SENI input of the next device LOW and so on throughout the chain. When a given device in the chain is fully programmed the SENO output essentially follows the SENI input. The user should monitor the SENO output of the final device in the chain. When this output goes LOW, serial loading of all devices has been completed.
SI (L2)	Serial In	HSTL INPUT	During serial programming this pin is loaded with the serial data that will configure the multi-queue devices. Data present on SI will be loaded on a rising edge of SCLK provided that SENI is LOW. In expansion mode the serial data input is loaded into the first device in a chain. When that device is loaded and its SENO has gone LOW, the data present on SI will be directly output to the SO output. The SO pin of the first device connects to the SI pin of the second and so on. The multi-queue device setup registers are shift registers.
SO (L3)	Serial Out	HSTL OUTPUT	This output is used in expansion mode and allows serial data to be passed through devices in the chain to complete programming of all devices. The SI of a device connects to SO of the previous device in the chain. The SO of the final device in a chain should not be connected.
TCK (B10)	JTAG Clock	HSTL INPUT	Clock input for JTAG function. One of four terminals required by IEEE Standard 1149.1-1990. Test operations of the device are synchronous to TCK. Data from TMS and TDI are sampled on the rising edge of TCK and outputs change on the falling edge of TCK. If the JTAG function is not used this signal needs to be tied to GND.

PIN DESCRIPTIONS (CONTINUED)

Symbol & (Pin No.)	Name	I/O TYPE	Description
TDI (A11)	JTAG Test Data	HSTL INPUT	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, Input test data serially loaded via the TDI on the rising edge of TCK to either the Instruction Register, ID Register and Bypass Register. An internal pull-up resistor forces TDI HIGH if left unconnected
TDO (B11)	JTAG Test Data Output	HSTL	One of four terminals required by IEEE Standard 1149.1-1990. During the JTAG boundary scan operation, test data serially loaded output via the TDO on the falling edge of TCK from either the Instruction Register, ID Register and Bypass Register. This output is high impedance except when shifting, while in SHIFT-DR and SHIFT-IR controller states.
TP (U3)	IDT Internal Test Pin	LVTTL	For IDT internal test purpose only, must be tied to GND for normal/correct operation.
TMS (A10)	JTAG Mode Select	HSTL INPUT	TMS is a serial input pin. One of four terminals required by IEEE Standard 1149.1-1990. TMS directs the device through its TAP controller states. An internal pull-up resistor forces TMS HIGH if left unconnected.
$\overline{TRST}$ (A9)	JTAG Reset	HSTL INPUT	$\overline{TRST}$ is an asynchronous reset pin for the JTAG controller. The JTAG TAP controller does not automatically reset upon power-up, thus it must be reset by either this signal or by setting TMS= HIGH for five TCK cycles. If the TAP controller is not properly reset then the outputs will always be in high-impedance. If the JTAG function is used but the user does not want to use $\overline{TRST}$, then $\overline{TRST}$ can be tied with $\overline{MRS}$ to ensure proper queue operation. If the JTAG function is not used then this signal needs to be tied to GND. An internal pull-up resistor forces $\overline{TRST}$ HIGH if left unconnected.
WADEN (M3)	Write Address Enable	HSTL INPUT	The WADEN input is used in conjunction with WCLK and the WRADD address bus to select a queue to be written in to. A queue addressed via the WRADD bus is selected on the rising edge of WCLK provided that WADEN is HIGH. WADEN should be asserted (HIGH) only during a queue change cycle(s). WADEN should not be permanently tied HIGH. WADEN cannot be HIGH for the same WCLK cycle as FSTR. Note, that a write queue selection cannot be made, (WADEN must NOT go active) until programming of the part has been completed and SENO has gone LOW.
WCLK (M2)	Write Clock	HSTL INPUT	When enabled by $\overline{WEN}$, the rising edge of WCLK writes data into the selected Queue via the input bus, Din. The Queue to be written to is selected via the WRADD address bus and a rising edge of WCLK while WADEN is HIGH. A rising edge of WCLK in conjunction with FSTR and WRADD will also select the flag quadrant to be placed on the $\overline{PAF}$n bus during direct flag operation. During polled flag operation the $\overline{PAF}$n bus is cycled with respect to WCLK and the FSYNC signal is synchronized to WCLK. The $\overline{PAF}$n, $\overline{PAF}$ and $\overline{FF}$ outputs are all synchronized to WCLK. During device expansion the FXO and FXI signals are based on WCLK. The WCLK must be continuous and free-running
$\overline{WCS}$ (L1)	Write Chip Select	HSTL INPUT	The $\overline{WCS}$ signal in concert with $\overline{WEN}$ signal provides control to enable data from the input write data bus to be written into the device. During a Master Reset cycle the $\overline{WCS}$ it is don't care signal.
$\overline{WEN}$ (M1)	Write Enable	HSTL INPUT	The $\overline{WEN}$ input enables write operations to a selected Queue based on a rising edge of WCLK. A queue to be written to can be selected via WCLK, WADEN and the WRADD address bus regardless of the state of $\overline{WEN}$. Data present on Din can be written to a newly selected queue on the second WCLK cycle after queue selection provided that $\overline{WEN}$ is LOW. A write enable is not required to cycle the $\overline{PAF}$n bus (in polled mode) or to select the $\overline{PAF}$n quadrant , (in direct mode).
WRADD[7:0] (WRADD7-R2 WRADD6-R1 WRADD5-P3 WRADD4-P2 WRADD3-P1 WRADD2-N3 WRADD1-N2 WRADD0-N1)	Write Address Bus	HSTL INPUT	The WRADD bus is 8 bits. The WRADD bus is a dual purpose address bus. The first function of WRADD is to select a Queue to be written to. The least significant 5 bits of the bus, WRADD[4:0] are used to address 1 of 128 possible queues within a multi-queue device. The most significant 3 bits, WRADD[7:5] are used to select 1 of 8 possible multi-queue devices that may be connected in expansion mode. These 3 MSB's will address a device with the matching ID code. (See ID[2:0] description for more detail on matching ID code. The second function of the WRADD bus is to select the quadrant of queues to be loaded on to the $\overline{PAF}$n bus during strobed flag mode. The least significant 4 bits, WRADD[3:0] are used to select the quadrant of a device to be placed on the $\overline{PAF}$n bus. The most significant 3 bits, WRADD[7:5] are again used to select 1 of 8 possible multi-queue devices that may be connected in expansion mode. Address bit WRADD[4] is don't care during quadrant selection.
ZQ (N22)	ZQ	HSTL INPUT	Output Impedance Matching Input. This input is used to tune the device outputs to the system data bus impedance. Q[39:0] output impedance is set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. This pin cannot be connected directly to GND or left unconnected.

PIN DESCRIPTIONS (CONTINUED)

Symbol & Pin No.	Name	I/O TYPE	Description
VDD (See below)	+1.8V Supply	Power	These are VCC power supply pins and must all be connected to a +1.8V supply
VDDQ (See below)	Output Voltage	Power	These pins must be tied to the desired output supply voltage (=1.5V for HSTL and =1.8V for eHSTL).
Vref (J1, M21)	Reference	INPUT	This is a Voltage Reference input and must be connected to a voltage level determined from the table Voltage "Recommended DC Operating Conditions". The input provides the reference level for HSTL/ eHSTL inputs.
GND (See below)	Ground	Ground	These are Ground pins and must all be connected to the Ground of the power supply.
AVDD (K21, M22)	PLL Power	Power	1.8V PLL Power Supply.
AVSS (L(21,22), K22)	PLL Ground	Ground	Ground for the PLL device. Should be connected to ground of the system.

NOTE:
1. Inputs should not change after Master Reset.

PIN NUMBER TABLE

Symbol	Name	I/O TYPE	Pin Number
D[39:0]	Data Input Bus	HSTL-LVTTL INPUT	D39-AA9, D38-BB8, D37-AA8, D36-BB7, D35-AA7, D34-BB6, D33-AA6, D32-BB5, D31-AA5, D30-BB4, D29-AA4, D28-BB3, D27-AA3, D(26,25)-Y(3,4), D(24-22)-W(3-1), D(21,20)-V(3,2), D(19,18)-E(2,3), D(17-15)-D(1-3), D(14,13)-C(4,3), D12-B3, D11-A3, D10-B4, D9-A4, D8-B5, D7-A5, D6-B6, D5-A6, D4-B7, D3-A7, D2-B8, D1-A8, D0-B9
Q[39:0]	Data Output Bus	HSTL-LVTTL	Q39-AA13, Q38-BB14, Q37-AA14, Q36-BB15, Q35-AA15, Q34-AA15, Q33-AA16, Q32-BB17, Q31-AA17, Q30-BB18, Q29-AA18, Q28-BB19, Q27-AA19, Q26-BB20, Q25-AA20, Q(24,23)-Y(20,19), Q(22-20)-W(20-22), Q(19-17)-D(22-20), Q(16,15)-C(19,20), Q14-B20, Q13-A20, Q12-B19, Q11-A19, Q10-B18, Q9-A18, Q8-B17, Q7-A17, Q6-B16, Q5-A16, Q4-B15, Q3-A15, Q2-B14, Q1-A14, Q0-B13
V_{DD}	+1.8V Supply	Power	D(4-10,13-19), E(4-9,14-17,19), G18, H(4,5,18,19), J(4,19), P(4,19), R(3-5,18,19), V(4-8,15-19), W(4-10,13-19)
V_{DDQ}	O/P Rail Voltage	Power	C(5-10,13-18) E18, F(4,5,18,19), G(4,5,19), T(4,5,18,19), U(4,5,18,19), Y(5-10,14-18)
GND	Ground Pin	Ground	A(1,2,21,22), B(1,2,21,22), C(1,2,11,12,21,22), D(11,12), E(10-13), J(5,9-14,18), K(4,5,9-14,18-20), L(4,5,9-14,18-20), M(4,5,9-14,18-20), N(4,5,9-14,18,19), P(5,9-14,18), V(9-14), W(11,12), Y(1,2,11-13,21,22), AA(1,2,21,22), BB(1,2,21,22)

ABSOLUTE MAXIMUM RATINGS

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with respect to GND	–0.5 to +2.9[2]	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Compliant with JEDEC JESD8-5. V_{DD} terminal only.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter[1]	Conditions	Max.	Unit
C_{IN}[2,3]	Input Capacitance	V_{IN} = 0V	10[3]	pF
C_{OUT}[1,2]	Output Capacitance	V_{OUT} = 0V	15	pF

NOTES:

1. With output deselected, ($\overline{OE} \geq V_{IH}$).
2. Characterized values, not currently tested.
3. C_{IN} for Vref is 20pF.

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.7	1.8	1.9	V
V_{DDQ}	Output Rail Voltage for I/Os	— eHSTL	1.7	1.8	1.9	V
		— HSTL	1.4	1.5	1.6	V
GND	Supply Voltage		0	0	0	V
V_{IH}[2]	Input High Voltage	— eHSTL	V_{REF}+0.2	—	—	V
		— HSTL	V_{REF}+0.2	—	—	V
V_{IL}	Input Low Voltage	— eHSTL	—	—	V_{REF}-0.2	V
		— HSTL	—	—	V_{REF}-0.2	V
V_{REF}[1] (HSTL only)	Voltage Reference Input	— eHSTL	0.8	0.9	1.0	V
		— HSTL	0.68	0.75	0.9	V
T_A	Operating Temperature Commercial		0	—	70	°C
T_A	Operating Temperature Industrial		-40	—	85	°C

NOTES:

1. V_{REF} is only required for HSTL or eHSTL inputs.
2. V_{IH} AC Component = V_{REF} + 0.4V

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{DD} = 1.8V ± 0.10V, T_A = 0°C to +70°C;Industrial: V_{DD} = 1.8V ± 0.10V, T_A = -40°C to +85°C)

Symbol	Parameter			Min.	Max.	Unit
I_{LI}	Input Leakage Current			–10	10	µA
I_{LO}	Output Leakage Current			–10	10	µA
V_{OH1}[7]	Output High Voltage (test conditions: RQ = 205Ω I_{OH} = -8mA)			V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V
V_{OL1}[8]	Output Low Voltage (test conditions: RQ = 205Ω I_{OL} = 8mA)			V_{DDQ}/2-0.12	V_{DDQ}/2+0.12	V
V_{OH2}[9]	Output High Voltage (test conditions: I_{OH} = -0.1mA)			V_{DDQ}-0.12	V_{DDQ}	V
V_{OL2}[10]	Output Low Voltage (test conditions: I_{OL} = 0.1mA)			V_{SS}	0.2	V
I_{DD1}[1,2]	Active V_{DD} Current (V_{DD} = 1.8V)		I/O = HSTL	—	200	mA
			I/O = eHSTL	—	200	mA
I_{DD2}[1, 5]	Standby V_{DD} Current (V_{DD} = 1.8V)		I/O = HSTL	—	120	mA
			I/O = eHSTL	—	120	mA
I_{DDQ}[1,2]	Active V_{DDQ} Current	(V_{DDQ} = 1.5V HSTL)	I/O = HSTL	—	20	mA
		(V_{DDQ} = 1.8V eHSTL)	I/O = eHSTL	—	20	mA

NOTES:

1. Both WCLK and RCLK toggling at 20MHz.
2. Data inputs toggling at 10MHz.
3. Total Power consumed: PT = [(V_{DD} x I_{DD}) + (V_{DDQ} x I_{DDQ})].
4. Outputs are not 2.5V or 3.3V tolerant.
5. The following inputs should be pulled to GND: $\overline{\text{WRADD}}$, $\overline{\text{RDADD}}$, $\overline{\text{WADEN}}$, FSTR, ESTR, SCLK, SI, EXI, FXI and all Data Inputs.
   The following inputs should be pulled to V_{DD}: $\overline{\text{WEN}}$, $\overline{\text{REN}}$, $\overline{\text{SENI}}$, $\overline{\text{MRS}}$, TDI, TMS and $\overline{\text{TRST}}$.
   All other inputs are don't care and should be at a known state.
6. The ZQ pin is used to control the device outputs (Q[39:0], $\overline{\text{EREN}}$, ERCLK, and $\overline{\text{ERCLK}}$).
7. Outputs are impedance-controlled. I_{OH}= -(V_{DDQ}/2)/(RQ/5) and is guaranteed by device characterization for 175Ω< RQ < 350Ω. This parameter is tested at RQ = 250Ω which gives a nominal 50Ω output impedance.
8. Outputs are impedance-controlled. I_{OL} = (V_{DDQ}/2)/(RQ/5) and is guaranteed by device characterization for 175Ω< RQ < 350Ω This parameter is tested at RQ = 250Ω which gives a nominal 50Ω output impedance.
9. This measurement is taken to ensure that the output has the capability of pulling to the V_{DDQ} rail, and is not intended to be used as an impedance measurement point.
10. This measurement is taken to ensure that the output has the capability of pulling to V_{SS}, and is not intended to be used as an impedance measurement point.

HSTL
1.5V AC TEST CONDITIONS

Input Pulse Levels	0.25 to 1.25V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.75
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.5V ± 0.1V.

EXTENDED HSTL
1.8V AC TEST CONDITIONS

Input Pulse Levels	0.4 to 1.4V
Input Rise/Fall Times	0.4ns
Input Timing Reference Levels	0.9
Output Reference Levels	$V_{DDQ}/2$

NOTE:
1. V_{DDQ} = 1.8V ± 0.1V.

AC TEST LOADS

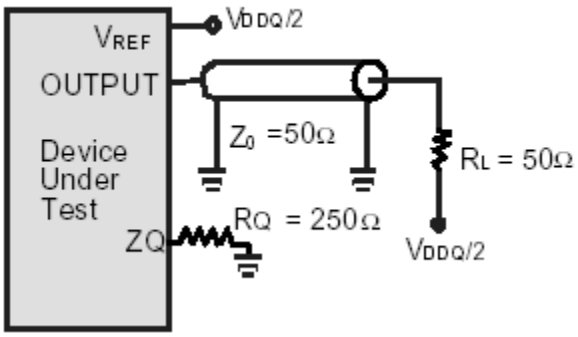


Figure 2a. AC Test Load

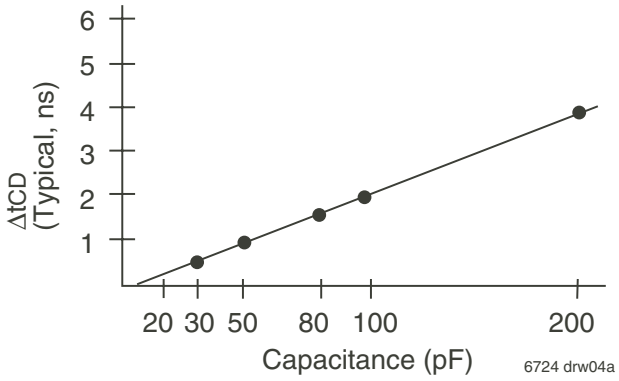
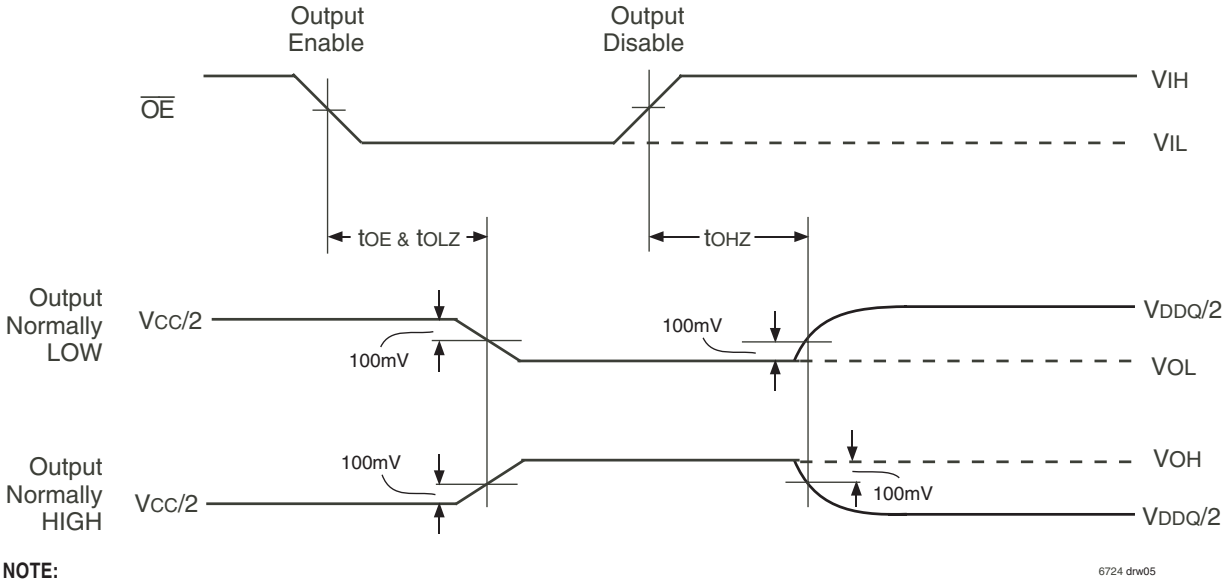


Figure 2b. Lumped Capacitive Load, Typical Derating

OUTPUT ENABLE & DISABLE TIMING



NOTE:
1. $\overline{REN}$ is HIGH.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{DD} = 1.8V ± 0.10V, T_A = 0°C to +70°C;Industrial: V_{DD} = 1.8V ± 0.10V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

		Commercial		Com'l and Ind'l		
		IDT72P51767L6 IDT72P51777L6		IDT72P51767L7-5 IDT72P51777L7-5		
Symbol	Parameter	Min.	Max.	Min.	Max.	Unit
f_C	Clock Cycle Frequency	—	166	—	133	MHz
t_A (PLL ON)	Data Access Time	-1.0	1.0	-1.2	1.2	ns
t_A (PLL OFF)	Data Access Time	0.6	3.6	0.8	3.8	ns
t_{CLK}	Clock Cycle Time	6.0	—	7.5	—	ns
t_{CLKH}	Clock High Time	2.8	—	3.0	—	ns
t_{CLKL}	Clock Low Time	2.8	—	3.0	—	ns
t_{DS}	Data Setup Time	0.48	—	0.7	—	ns
t_{DH}	Data Hold Time	0.48	—	0.7	—	ns
t_{ENS}	Enable Setup Time	2.0	—	2.2	—	ns
t_{ENH}	Enable Hold Time	0.5	—	0.7	—	ns
t_{RS}	Reset Pulse Width[3]	30	—	30	—	ns
t_{RSS}	Reset Setup Time	15	—	15	—	ns
t_{RSR}	Reset Recovery Time	10	—	10	—	ns
t_{OHZ}	Output Enable to Output in High Z	0.6	3.6	0.8	3.8	ns
t_{OE}	Output Enable to $\overline{OE}$	0.6	3.6	0.8	3.8	ns
f_S	Clock Cycle (SCLK)	—	10	—	10	MHz
t_{SCLK}	Serial Clock Cycle	100	—	100	—	ns
t_{SCKH}	Serial Clock High	45	—	45	—	ns
t_{SCKL}	Serial Clock Low	45	—	45	—	ns
t_{SDS}	Serial Data in Setup	20	—	20	—	ns
t_{SDH}	Serial Data in Hold	0.8	—	0.8	—	ns
t_{SENS}	Serial Enable Setup	20	—	20	—	ns
t_{SENH}	Serial Enable Hold	0.8	—	0.8	—	ns
t_{SDO}	SCLK to Serial Data Out	—	20	—	20	ns
t_{SENO}	SCLK to Enable Out	—	20	—	20	ns
t_{SDOP}	Serial Data Out Delay	0.8	3.6	0.8	3.6	ns
t_{SENOP}	Serial Enable Delay	0.8	3.6	0.8	3.6	ns
t_{PCWQ}	Programming to Write Queue Selection	—	7	—	7	cycles
t_{PCRQ}	Programming to Read Queue Selection	—	7	—	7	cycles
t_{AS}	Address Setup	2.0	—	2.2	—	ns
t_{AH}	Address Hold	0.5	—	0.7	—	ns
t_{WFF}	Write Clock to Full Flag ($\overline{FF}$)	-—	3.6	—	3.8	ns
t_{REF}	Read Clock to Empty Flag ($\overline{EF}$)	-—	3.6	—	3.8	ns
t_{STS}	Strobe Setup	2.0	—	2.2	—	ns
t_{STH}	Strobe Hold	0.5	—	0.7	—	ns
t_{QS}	Queue Setup	2.0	—	2.2	—	ns
t_{QH}	Queue Hold	0.5	—	0.7	—	ns
t_{WAF}	WCLK to $\overline{PAF}$ flag	0.6	3.6	0.8	3.8	ns
t_{RAE}	RCLK to $\overline{PAE}$ flag	0.6	3.6	0.8	3.8	ns
t_{PAF}	WCLK to Sync $\overline{PAF}$ bus	0.6	3.6	0.8	3.8	ns
t_{PAE}	RCLK to Sync $\overline{PAE}$ bus	0.6	3.6	0.8	3.8	ns
t_{PAELZ}	RCLK to Low-Z	0.6	3.6	0.8	3.8	ns
t_{PAEHZ}	RCLK to High-Z	0.6	3.6	0.8	3.8	ns
t_{PAFLZ}	WCLK to $\overline{PAF}$ Bus Low-Z	0.6	3.6	0.8	3.8	ns

NOTES:

1. Industrial temperature range product for the 7-5ns is available as a standard device. All other speed grades available by special order.
2. Values guaranteed by design, not currently tested.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

(Commercial: V_{DD} = 1.8V ± 0.10V, T_A = 0°C to +70°C;Industrial: V_{DD} = 1.8V ± 0.10V, T_A = -40°C to +85°C; JEDEC JESD8-A compliant)

Symbol	Parameter	Commercial IDT72P51767L6 IDT72P51777L6		Com'l and Ind'l IDT72P51767L7-5 IDT72P51777L7-5		Unit
		Min.	Max.	Min.	Max.	
t_{PAFHZ}	WCLK to $\overline{PAF}$ Bus High-Z	0.6	3.6	0.8	3.8	ns
t_{FFHZ}	WCLK to $\overline{FF}$ High-Z	0.6	3.6	0.8	3.8	ns
t_{FFLZ}	WCLK to $\overline{FF}$ Low-Z	0.6	3.6	0.8	3.8	ns
t_{EFHZ}	RCLK to $\overline{EF}$ High-Z	0.6	3.6	0.8	3.8	ns
t_{EFLZ}	RCLK to $\overline{EF}$ Low-Z	0.6	3.6	0.8	3.8	ns
t_{FSYNC}	WCLK to $\overline{PAF}$ Bus Sync	0.6	3.6	0.8	3.8	ns
t_{FXO}	WCLK to $\overline{PAF}$ Bus Exp	0.6	3.6	0.8	3.8	ns
t_{ESYNC}	RCLK to $\overline{PAF}$ Bus Sync	0.6	3.6	0.8	3.8	ns
t_{EXO}	RCLK to $\overline{PAF}$ Bus Exp	0.6	3.6	0.8	3.8	ns
t_{ERCLK} (DDR)	RCLK to ERCLK (DDR)	—	2.5	—	3.2	ns
t_{ERCLK} (SDR)	RCLK to ERCLK (SDR)	—	4	—	5	ns
t_{SKEW1}	Skew time for $\overline{EF}$ and $\overline{FF}$	6.0	—	7.0	—	ns
t_{SKEW2}	Skew time for $\overline{PAF}$ and $\overline{PAE}$	6.0	—	7.0	—	ns
t_{SKEW3}	Skew time for $\overline{PAF}$/$\overline{PAE}$[0:7]	6.0	—	7.0	—	ns
t_{XIS}	Expansion Input Setup	2.0	—	2.2	—	ns
t_{XIH}	Expansion Input Hold	0.5	—	0.7	—	ns
t_{LOCK}	PLL Lock Time	—	15	—	15	µs

NOTES:
1. Industrial temperature range product for the 7-5ns is available as a standard device. All other speed grades available by special order.
2. Values guaranteed by design, not currently tested.

XGMII REFERENCE SPECIFICATION

The XGMII uses 1.5V High Speed Transceiver Logic (HSTL) signal levels.

The electrical characteristics of the XGMII are specified such that the XGMII can be applied within a variety of 10 Gb/s equipment types. The electrical specifications are selected for an integrated circuit to integrated circuit application. The electrical characteristics specified in this clause apply to all XGMII signals.

When implemented as a chip-to-chip interface, the XGMII uses High Speed Transceiver Logic (HSTL), specified for a 1.5 volt output buffer supply voltage. XGMII chip-to-chip signals shall comply with EIA/JEDEC Standard EIA/JESD8-6 using Class I, output buffers. Output impedance shall be greater than 38Ω to assure acceptable overshoot and undershoot performance in an un-terminated interconnection.

TABLE 2 — DC AND AC SPECIFICATIONS (INFORMATIVE)

Symbol	Parameter	Minimum	Nominal	Maximum	Units
V_{DDQ}	Output Voltage Supply	1.4	1.5	1.6	V
V_{REF}	Input Reference Voltage	0.68	0.75	0.90	V
V_{IH_DC}	DC Input Logic High	V_{REF}+0.10	-	V_{DDQ}+0.3	V
V_{IL_DC}	DC Input Logic Low	-0.30	-	V_{REF}-0.1	V
V_{IH_AC}	AC Input Logic High	V_{REF}+0.20	-	-	V
V_{IL_AC}	AC Input Logic Low	-	-	V_{REF}-0.20	V

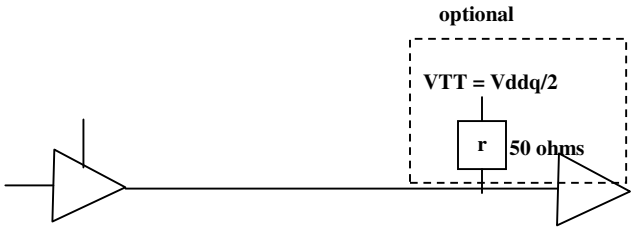


Figure 3. HSTL Termination for XGMII

TABLE 3 — IDT TO XGMII INTERFACE MAPPING SCHEMA

Signal Type	IDT Interface Signal Nomenclature	XGMII Signal Nomenclature
Input Port		
- Input Port Data	D[31:0]	TXD [31:0]
	D[32:39]	User definable
- Input Port Enable	$\overline{WEN}$	N/A
- Input Port Control	N/A	TXC[3:0]
- Input Port Status	$\overline{FF}$, $\overline{PAF}$	N/A
- Input Port Clock	WCLK	TX_CLK
Output Port		
- Output Port Data	Q[31:0]	RXD [31:0]
	Q[32:39]	User definable
- Output Port Enable	$\overline{REN}$	N/A
- Output Port Control	N/A	RXC [3:0}
- Output Port Status	$\overline{EF}$, $\overline{PAE}$	N/A
- Output Port Clock	RCLK	RX_CLK

FUNCTIONAL DESCRIPTION

MASTER RESET

A Master Reset is performed by toggling the $\overline{MRS}$ input from HIGH to LOW to HIGH. During a master reset all internal multi-queue device setup and control registers are initialized and require programming either serially by the user via the serial port, or via parallel programming or by using the default settings. Refer to Figure 6, *Device Programming Hierarchy* for the programming hierarchy structure. During a master reset the state of the following inputs determine the functionality of the part, these pins should be held HIGH or LOW.

FM – Flag bus Mode
BM [3:0] – Bus Matching options
MAST – Master Device
ID0, 1, 2 – Device ID
QSEL[2:0] Queue Select Mode
DFM – Programming mode, serial or default

Once a master reset has taken place, the device must be programmed either serially or via the default method before any read/write operations can begin.

See Figure 37, *Master Reset* for relevant timing.

PROGRAMMING MODE CAPTURED

On the rising of $\overline{MRS}$ the programming mode signals (QSEL [2:0], DFM) are captured. Once the programming mode signals are captured (latched), refer to Table 5, Setting the Queue Programming Mode during Master Reset for details. It will then require a number of clock cycles for the device to complete the configuration. Configuration completion is indicated when the $\overline{SENO}$ signal transitions from high to low. The configuration completion indication is consistent with the previous MQ device.

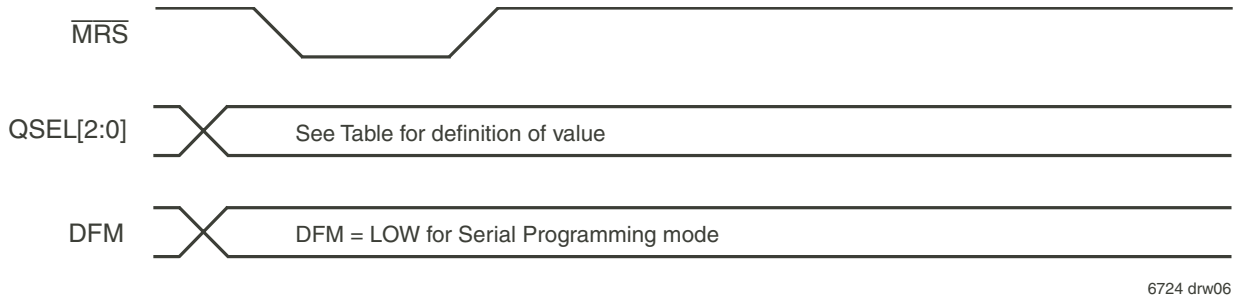


Figure 4. Reference Signals

TABLE 4 — DEVICE PROGRAMMING MODE COMPARISON

Programming Options	Serial Programming Mode	Default/Parallel Programming Mode
Queue Selection	Any number from 1 to 128	Any number from 1 to 128
Queue Depth	Each queue depth can be individualized	Default Value (total available memory divided by number of queues)
$\overline{PAE}$/$\overline{PAF}$	Programmable to any value	Default value
Bus-Matching	Any available option can be selected using BM[3:0] pins	Any available option can be selected using BM[3:0] pins
I/O voltage	Any available option can be selected	Any available option can be selected

TABLE 5 — SETTING THE QUEUE PROGRAMMING MODE DURING MASTER RESET

/MRS	Default Mode (DFM)	QSEL 2	QSEL 1	QSEL 0	Queue Programming Method
↑	0	0	0	0	Serial programming mode
↑	0	0	0	1	RESERVED
↑	0	0	1	0	RESERVED
↑	0	0	1	1	RESERVED
↑	0	1	0	0	RESERVED
↑	0	1	0	1	RESERVED
↑	0	1	1	0	RESERVED
↑	0	1	1	1	RESERVED
↑	1	0	0	0	Selects 128 Queues
↑	1	0	0	1	Selects 64 Queues
↑	1	0	1	0	Selects 32 Queues
↑	1	0	1	1	Selects 16 Queues
↑	1	1	0	0	Selects 8 Queues
↑	1	1	0	1	Selects 4 Queues
↑	1	1	1	0	Parallel programming enables the user to program the number of queues using the Write Address bus
↑	1	1	1	1	Parallel programming enables the user to program the number of queues using the Read Address bus

6724 drw07

SERIAL PROGRAMMING

The multi-queue flow-control device is a fully programmable device, providing the user with flexibility in how queues are configured in terms of the number of queues, depth of each queue and position of the $\overline{PAF}$/$\overline{PAE}$ flags within respective queues. All user programming is done via the serial port after a master reset has taken place. Internally the multi-queue device has setup registers which must be serially loaded, these registers contain values for every queue within the device, such as the depth and $\overline{PAE}$/$\overline{PAF}$ offset values. The IDT72P51767/72P51777 devices are capable of up to 128 queues and therefore contain 128 sets of registers for the setup of each queue.

During a Master Reset if the DFM (Default Mode) input is LOW, then the device will require serial programming by the user. It is recommended that the user utilize a 'C' program provided by IDT, this program will prompt the user for all information regarding the multi-queue setup. The program will then generate a serial bit stream which should be serially loaded into the device via the serial port. For the IDT72P51767/72P51777 devices the serial programming requires a total number of serially loaded bits per device, (SCLK cycles with $\overline{SENI}$ enabled), calculated by: 27+(Qx104) where Q is the number of queues the user wishes to setup within the device.

Once the master reset is complete and $\overline{MRS}$ is HIGH, the device can be serially loaded. Data present on the SI (serial in), input is loaded into the serial port on a rising edge of SCLK (serial clock), provided that $\overline{SENI}$ (serial in enable), is LOW. Once serial programming of the device has been successfully completed the device will indicate this via the $\overline{SENO}$ (serial output enable) going active, LOW. Upon detection of completion of programming, the user should cease all programming and take $\overline{SENI}$ inactive, HIGH. Note, $\overline{SENO}$ follows $\overline{SENI}$ once programming of a device is complete. Therefore, $\overline{SENO}$ will go LOW after programming provided $\overline{SENI}$ is LOW, once $\overline{SENI}$ is taken HIGH again, $\overline{SENO}$ will also go HIGH. The operation of the SO output is similar, when programming of a given device is complete, the SO output will follow the SI input.

If devices are being used in expansion configuration the serial ports of devices should be cascaded. The user can load all devices via the serial input port control pins, SI & $\overline{SENI}$, of the first device in the chain. Again, the user may utilize the 'C' program to generate the serial bit stream, the program prompting the user for the number of devices to be programmed. The $\overline{SENO}$ and SO (serial out) of the first device should be connected to the $\overline{SENI}$ and SI inputs of the second device respectively and so on, with the $\overline{SENO}$ & SO outputs connecting to the $\overline{SENI}$ & SI inputs of all devices through the chain. All devices in the chain should be connected to a common SCLK. The serial output port of the final device should be monitored by the user. When $\overline{SENO}$ of the final device goes LOW, this indicates that serial programming of all devices has been successfully completed. Upon detection of completion of programming, the user should cease all programming and take $\overline{SENI}$ of the first device in the chain inactive, HIGH.

As mentioned, the first device in the chain has its serial input port controlled by the user, this is the first device to have its internal registers serially loaded by the serial bit stream. When programming of this device is complete it will take its $\overline{SENO}$ output LOW and bypass the serial data loaded on the SI input to its SO output. The serial input of the second device in the chain is now loaded with the data from the SO of the first device, while the second device has its $\overline{SENI}$ input LOW. This process continues through the chain until all devices are programmed and the $\overline{SENO}$ of the final device (or master device, ID = '000') goes LOW.

Once all serial programming has been successfully completed, normal operations, (queue selections on the read and write ports) may begin. When connected in expansion configuration, the IDT72P51767/72P51777 devices require a total number of serially loaded bits per device to complete serial programming, (SCLK cycles with $\overline{SENI}$ enabled), calculated by: n[27+(Qx104)] where Q is the number of queues the user wishes to setup within the device, where n is the number of devices in the chain.

See Figure 40, *Serial Port Connection* and Figure 41, *Serial Programming* for connection and timing information.

The IDT72P51777/72P51767 device can be programmed using the serial input signals (SENI, SI, SCLK). Serial programming is accomplished by shifting in 26 bit words. It requires 1 Header Word to start the programming sequence and an additional 4 Programming Words for each queue that is configured within the device.

EACH OF THE 26 BIT WORDS ARE DESCRIBED BELOW:

Header Word: This is 1st 26-bit word and has the following bit assignments.

- Bits [25:7] is the Start of Header identifier.
- Bits [6:0] are the number of queues to be programmed.

The Start of Header identifier MUST be all ones (1's). The all 1's pattern in the Header word signifies the start of the programming cycle. The Header Word is only needed once for each device. For example, for 128 queues bits [6:0] = "1111111" for 32 queues bits [6:0] = "0011111".

Bits	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	Q64	Q32	Q16	Q8	Q4	Q2	Q1

$\overline{FF}$: This is the 2nd 26-bit word and represents the Full Flag programmed value. The Full Flag value is equal to the Queue depth-2. Each queue requires an individual $\overline{FF}$ value.

Bits	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary Value	0	0	0	0	0	0	524288	262144	131072	65536	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

$\overline{\text{PAE}}$: This is the 3rd 26-bit word and represents the Programmable Almost Empty ($\overline{\text{PAE}}$) value. Each queue requires an individual $\overline{\text{PAE}}$ value. The $\overline{\text{PAE}}$ value that is programmed into the device is the number of words. For example, for a $\overline{\text{PAE}}$ value = 52 words, bits [19:0] = "00000000000000110100".

Bits	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary Value	0	0	0	0	0	0	524288	262144	131072	65536	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

$\overline{\text{PAF}}$: This is the 4th 26-bit word and represents the Programmable Almost Full ($\overline{\text{PAF}}$) value. Each queue requires an individual $\overline{\text{PAF}}$ value. The $\overline{\text{PAF}}$ value that is programmed into the device is the "Queue Depth Value" – "The $\overline{\text{PAF}}$ Offset value". For example, with a Queue Depth of 16K (16384) and a desired $\overline{\text{PAF}}$ value = 39 words, bits [19:0] = "00000011111111011001".

Bits	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Binary Value	0	0	0	0	0	0	524288	262144	131072	65536	32768	16384	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1

Queue End/Start Address

This is the 5th 26-bit word and represents both the start and end address of each queue.

End Address: The queue end address is bits [25:13] of the 26-bit. An end addresses is specified as; Queue Depth – 1k . Ending address are specified in increments of 1K words. For example, for a Queue Depth of 16K, the first queue would have a starting address of 0, bits [12:0] = "0000000000000" and an end address of 15K, bits [25:13] = "0000000001111",

Start Address: The queue starting address is bits [12:0] of the 26-bit word. Start addresses are specified in increments of words. The first queue should always start at address 0. The starting address of the next queue should be programmed at an address that is words greater the ending address of the previous queue.

Bits	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	4096	2048	1024	512	256	128	64	32	16	8	4	2	1