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FEATURES:

- Bus switches provide zero delay paths
- Low switch on-resistance
- TTL-compatible input and output levels
- ESD > 2000V per MIL-STD-883, Method 3015; > 200V using machine model (C = 200pF, R = 0)
- Hot insertion capability
- Very low power dissipation
- Available in TSSOP package

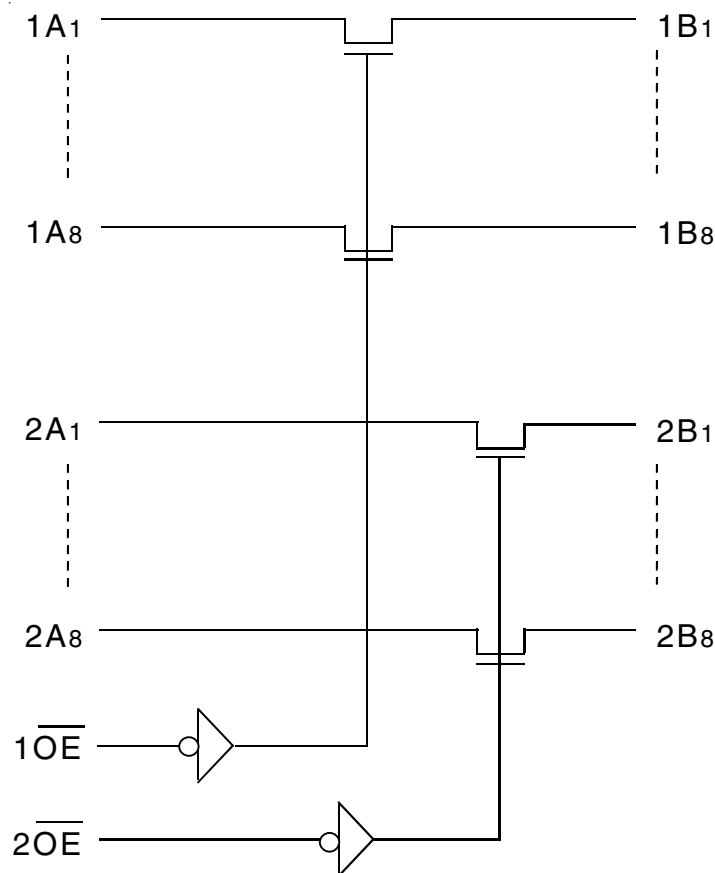
DESCRIPTION:

The FST163245 belongs to IDT's family of Bus switches. Bus switch devices perform the function of connecting or isolating two ports without providing any inherent current sink or source capability. Thus they generate little or no noise of their own while providing a low resistance path for an external driver. These devices connect input and output ports through an n-channel FET. When the gate-to-source junction of this FET is adequately forward-biased the device conducts and the resistance between input and output ports is small. Without adequate bias on the gate-to-source junction of the FET, the FET is turned off, therefore with no Vcc applied, the device has hot insertion capability.

The low on-resistance and simplicity of the connection between input and output ports reduces the delay in this path to close to zero.

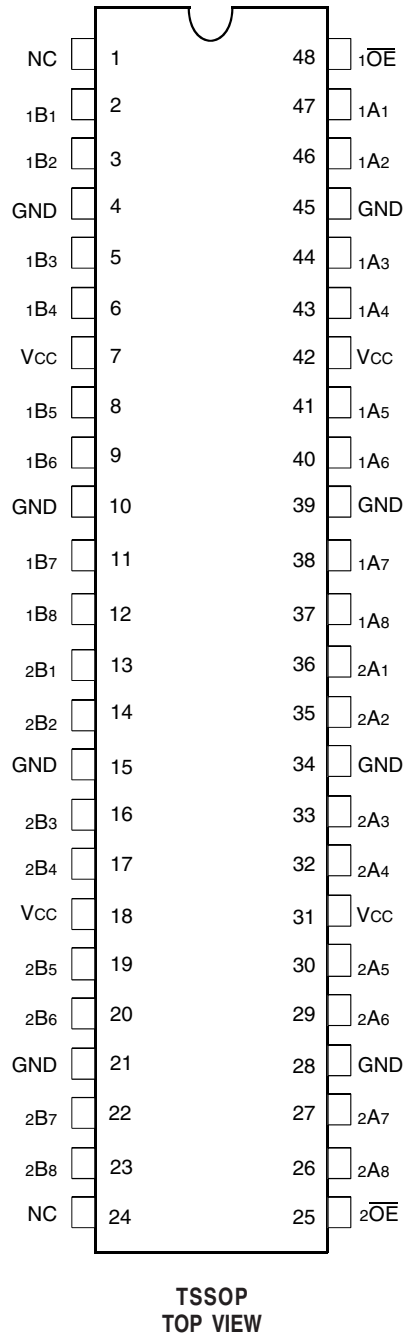
The FST163245 is pin compatible with and functionally similar to FCT16245.

FUNCTIONAL BLOCK DIAGRAM



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PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Description | Max | Unit |
|----------------------|--------------------------------------|-------------|------|
| VTERM ⁽²⁾ | Terminal Voltage with Respect to GND | -0.5 to +7 | V |
| TSTG | Storage Temperature | -65 to +150 | °C |
| IOUT | Maximum Continuous Channel Current | 128 | mA |

NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V_{CC}, Control, and Switch terminals.

CAPACITANCE⁽¹⁾

| Symbol | Parameter | Conditions ⁽²⁾ | Typ. | Unit |
|------------------|---------------------------------|---------------------------|------|------|
| C _{IN} | Control Input Capacitance | | 6 | pF |
| C _{I/O} | Switch Input/Output Capacitance | Switch Off | 12 | pF |

NOTES:

- Capacitance is characterized but not tested.
- T_A = 25°C, f = 1MHz, V_{IN} = 0V, V_{OUT} = 0V.

PIN DESCRIPTION

| Pin Names | I/O | Description |
|--------------|-----|--------------------------------|
| 1A1-8, 2A1-8 | I/O | Bus A |
| 1B1-8, 2B1-8 | I/O | Bus B |
| 1OE, 2OE | I | Bus Switch Enable (Active LOW) |

FUNCTION TABLE⁽¹⁾

| Inputs | Outputs |
|--------|---------------------|
| xOE | |
| L | Connect A to B |
| H | Disconnect A from B |

NOTE:

- H = HIGH Voltage Level
L = LOW Voltage Level

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol | Parameter | Test Conditions ⁽¹⁾ | Min. | Typ. ⁽²⁾ | Max. | Unit |
|-----------|--------------------------------|---|--------------------|---------------------|---------|---------------|
| V_{IH} | Control Input HIGH Voltage | Guaranteed Logic HIGH for Control Inputs | 2 | — | — | V |
| V_{IL} | Control Input LOW Voltage | Guaranteed Logic LOW for Control Inputs | — | — | 0.8 | V |
| I_{IH} | Control Input HIGH Current | $V_{CC} = \text{Max.}$ $V_i = V_{CC}$ | — | — | ± 1 | μA |
| I_{IL} | Control Input LOW Current | | $V_i = \text{GND}$ | — | — | |
| I_{OZH} | Current During | $V_{CC} = \text{Max.}, V_O = 0$ to 5V | — | — | ± 1 | μA |
| I_{OZL} | Bus Switch Disconnect | | — | — | ± 1 | |
| V_{IK} | Clamp Diode Voltage | $V_{CC} = \text{Min.}, I_{IN} = -18\text{mA}$ | — | -0.7 | -1.2 | V |
| I_{OFF} | Switch Power Off Leakage | $V_{CC} = 0\text{V}, V_{IN}$ or $V_O \leq 5.5\text{V}$ | — | — | ± 1 | μA |
| I_{CC} | Quiescent Power Supply Current | $V_{CC} = \text{Max.}, V_{IN} = \text{GND}$ or V_{CC} | — | 0.1 | 3 | μA |

BUS SWITCH IMPEDANCE OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Industrial: $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = 5.0\text{V} \pm 10\%$

| Symbol | Parameter | Test Conditions | Min. | Typ. ⁽¹⁾ | Max. | Unit |
|----------|--------------------------------------|--|------|---------------------|------|-------------|
| R_{ON} | Switch On Resistance ⁽²⁾ | $V_{CC} = \text{Min.}, V_{IN} = 0\text{V}, I_{ON} = 30\text{mA}$ | — | 5 | 7 | Ω |
| | | $V_{CC} = \text{Min.}, V_{IN} = 2.4\text{V}, I_{ON} = 15\text{mA}$ | — | 10 | 15 | |
| I_{OS} | Short Circuit Current ⁽³⁾ | $A(B) = 0\text{V}, B(A) = V_{CC}$ | 100 | — | — | mA |

NOTES:

1. Typical values are at $V_{CC} = 5.0\text{V}$, $+25^{\circ}\text{C}$ ambient.
2. The voltage drop between the indicated ports divided by the current through the switch.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.

POWER SUPPLY CHARACTERISTICS

| Symbol | Parameter | Test Conditions ⁽¹⁾ | | Min. | Typ. ⁽²⁾ | Max. | Unit |
|------------------|---|--|-------------------------|------|---------------------|------|-----------------------|
| ΔI_{CC} | Quiescent Power Supply Current TTL Inputs HIGH | VCC = Max. VIN = 3.4V ⁽³⁾ | | — | 0.5 | 1.5 | mA |
| I _{CCD} | Dynamic Power Supply Current ^(4,5) | VCC = Max., Outputs Open One Enable Pin Toggling 50% Duty Cycle | VIN = VCC VIN = GND | — | 240 | 320 | μA/ MHz/ Enable |
| I _C | Total Power Supply Current ⁽⁶⁾ | VCC = Max., Outputs Open Two Enable Pins Toggling fi = 10MHz 50% Duty Cycle | VIN = VCC VIN = GND | — | 4.8 | 6.4 | mA |
| | | | VIN = VCC VIN = 3.4V | — | 5.3 | 7.9 | |

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type. TA = -40°C to +85°C
- Typical values are at VCC = 5.0V, +25°C ambient.
- Per TTL driven input (VIN = 3.4V). All other inputs at VCC or GND. Switch inputs do not contribute to ΔI_{CC} .
- This parameter represents the current required to switch the internal capacitance of the control inputs at the specified frequency.
Switch inputs generate no significant power supply currents as they transition. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- $C_{PD} = I_{CCD}/V_{CC}$
CPD = Power Dissipation Capacitance
- $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
I_C = I_{CC} + $\Delta I_{CC} \cdot D_H \cdot N_T$ + I_{CCD} (fiN)
I_{CC} = Quiescent Current
 ΔI_{CC} = Power Supply Current for a TTL High Input (VIN = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
fi = Control Input Frequency
N = Number of Control Inputs Toggling at fi

SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

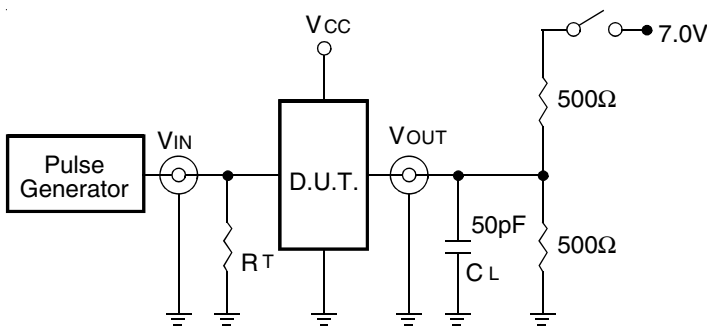
Industrial: TA = -40°C to +85°C, VCC = 5.0V ± 10%

| Symbol | Description | Min. ⁽¹⁾ | Typ. | Max. | Unit |
|------------------|--|---------------------|------|------|------|
| t _{PLH} | Data Propagation Delay | — | — | 0.25 | ns |
| t _{PHL} | A to B, B to A ⁽²⁾ | — | — | — | — |
| t _{PZH} | Switch CONNECT Delay | 1.5 | — | 6.5 | ns |
| t _{PZL} | \overline{xOE} to A or B | — | — | — | — |
| t _{PHZ} | Switch DISCONNECT Delay | 1.5 | — | 5.5 | ns |
| t _{PLZ} | \overline{xOE} to A or B | — | — | — | — |
| Q _{CI} | Charge Injection During Switch DISCONNECT \overline{xOE} to A or B ⁽³⁾ | — | 1.5 | — | pC |

NOTES:

- See test circuits and waveforms.
- The bus switch contributes no Propagation Delay other than the RC Delay of the load interacting with the RC of the switch.
- |Q_{CI}| is the charge injection for a single switch DISCONNECT and applies to either single switches or multiplexers. Charge injection is reduced because the injection from the DISCONNECT of the first path is compensated by the CONNECT of the second path.

TEST CIRCUITS AND WAVEFORMS



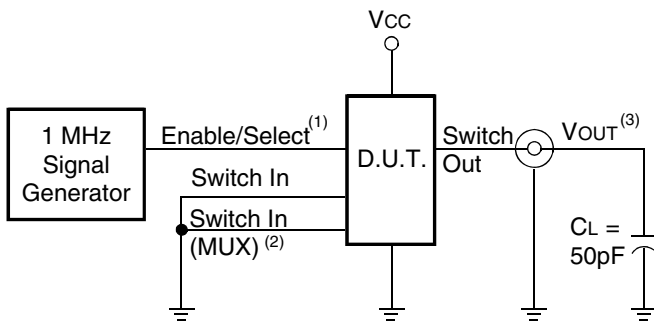
Test Circuits for All Outputs

SWITCH POSITION

| Test | Switch |
|---|--------|
| Open Drain Disable Low Enable Low | Closed |
| All Other Tests | Open |

DEFINITIONS:

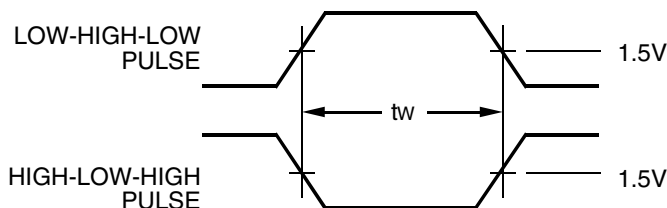
CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to ZOUT of the Pulse Generator.



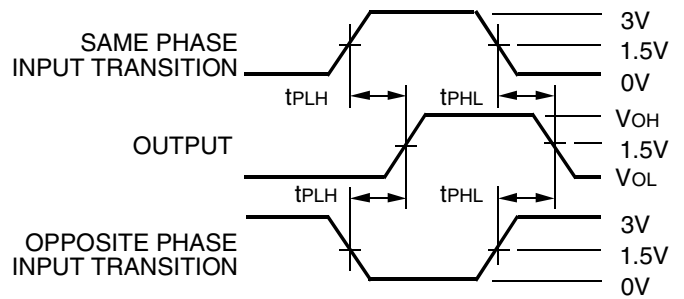
Charge Injection

NOTES:

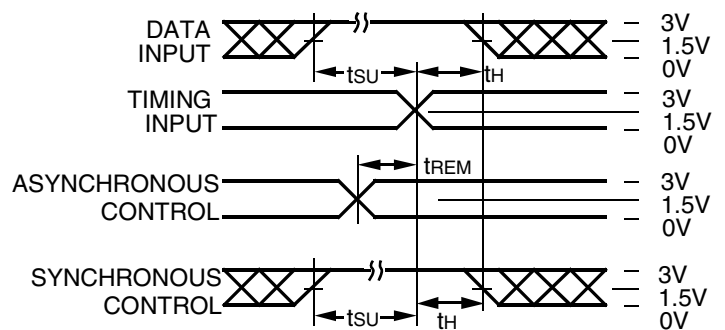
- Select is used with multiplexers for measuring IQDcil during multiplexer select. During all other tests Enable is used.
- Used with multiplexers to measure IQDcil only.
- Charge Injection = $\Delta V_{OUT} C_L$, with Enable toggling for IQDcil or Select toggling for IQDcil. ΔV_{OUT} is the change in V_{OUT} and is measured with a 10MΩ probe.



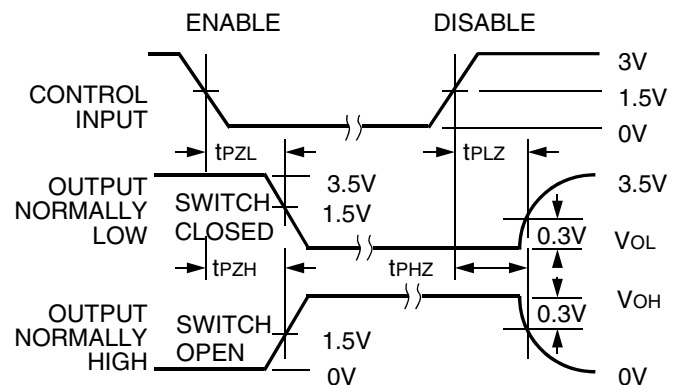
Pulse Width



Propagation Delay



Set-up, Hold, and Release Times

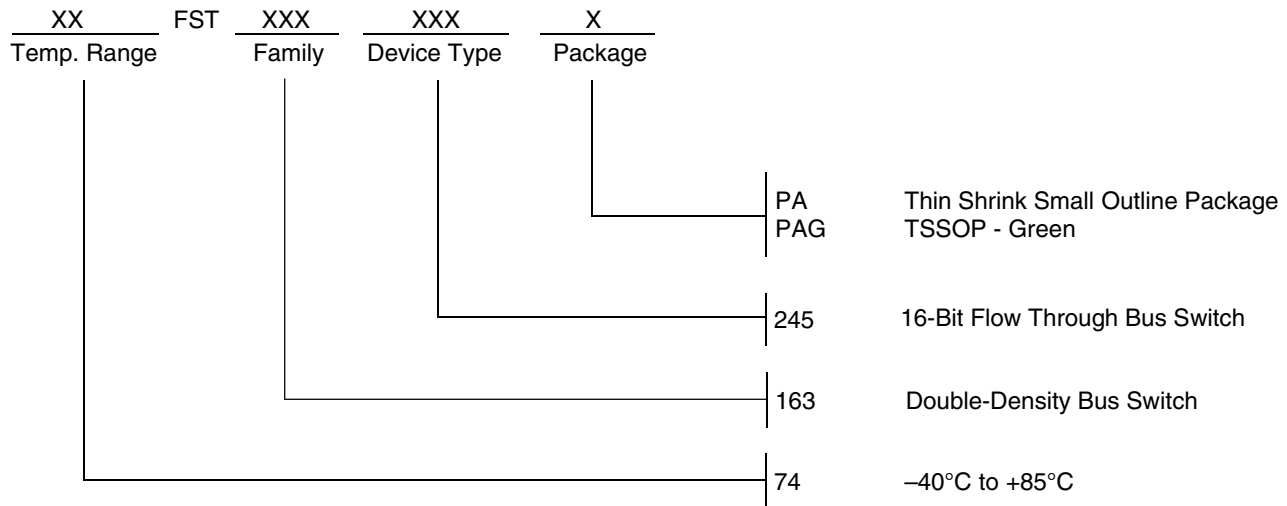


Enable and Disable Times

NOTES:

- Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.
- Pulse Generator for All Pulses: Rate $\leq 1.0\text{MHz}$; $t_r \leq 2.5\text{ns}$; $t_f \leq 2.5\text{ns}$.

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