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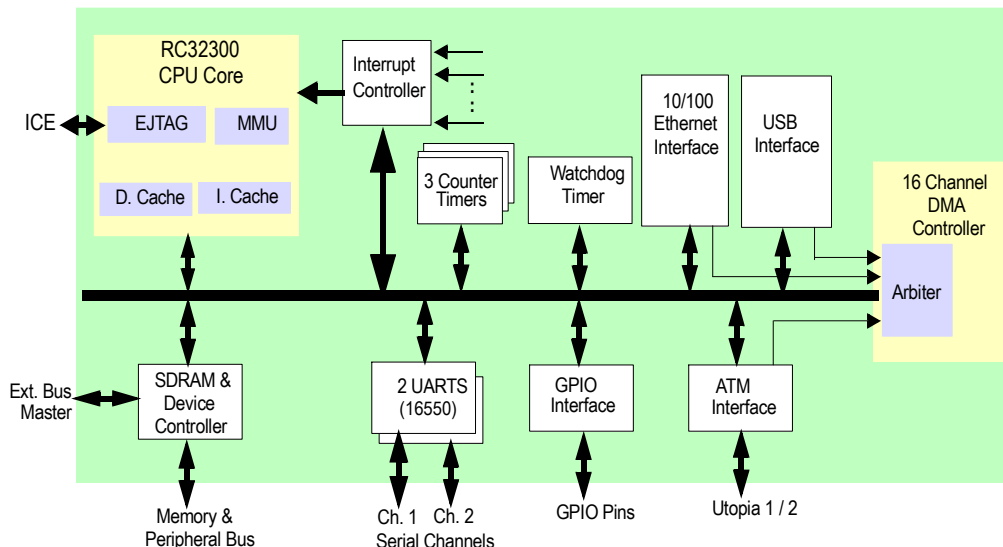


**Features List**

- ◆ **RC32300 32-bit Microprocessor**
  - Enhanced MIPS-II ISA
  - Enhanced MIPS-IV cache prefetch instruction
  - DSP Instructions
  - MMU with 16-entry TLB
  - 8kB Instruction cache, 2-way set associative
  - 2kB Data cache, 2-way set associative
  - Per line cache locking
  - Write-through and write-back cache management
  - Debug interface through the EJTAG port
  - Big or little endian support
- ◆ **Interrupt Controller**
  - Allows status of each interrupt to be read and masked
- ◆ **UARTs**
  - Two 16550 Compatible UARTs
  - Baud rate support up to 1.5 Mb/s
- ◆ **Counter/Timers**
  - Three general purpose 32-bit counter/timers
- ◆ **General Purpose I/O Pins (GPIO)**
  - 32 individually programmable pins: each pin programmable as input, output, or alternate function, input can be an interrupt or NMI source, input can also be active high or active low
  - 4 additional, auxiliary GPIO pins can be configured as input or output

- ◆ **SDRAM Controller**
  - 2 memory banks, non-interleaved, 512 MB total
  - 32-bit wide data path
  - Supports 4-bit, 8-bit, and 16-bit wide SDRAM chips
  - SODIMM support
  - Stays on page between transfers
  - Automatic refresh generation
- ◆ **Peripheral Device Controller**
  - 26-bit address bus
  - 32-bit data bus with variable width support of 8-, 16-, or 32-bits
  - 8-bit boot ROM support
  - 6 banks available, up to 64MB per bank
  - Supports Flash ROM, PROM, SRAM, dual-port memory, and peripheral devices
  - Supports external wait-state generation, Intel or Motorola style
  - Write protect capability
  - Direct control of optional external data transceivers
- ◆ **System Integrity**
  - Programmable system watchdog timer resets system on time-out
  - Programmable bus transaction times memory and peripheral transactions and generates a warm reset on time-out
- ◆ **DMA**
  - 14 DMA channels
  - Services on-chip and external peripherals
  - Supports memory-to-memory, memory-to-I/O, and I/O-to-I/O transfers
  - Supports flexible descriptor based operation and chaining via linked lists of records (scatter / gather capability)
  - Supports unaligned transfers

**Block Diagram**



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- Supports burst transfers
- ◆ **USB**
  - Revision 1.1 compliant
  - USB slave device controller
  - Supports a 6<sup>th</sup> USB endpoint
  - Full speed operation at 12 Mb/s
  - Supports control, interrupt, bulk and isochronous endpoints
  - Supports USB remote wakeup
  - Integrated USB transceiver
- ◆ **EJTAG**
  - Run-time Mode provides a standard JTAG interface
  - Real-Time Mode provides additional pins for real-time trace information
- ◆ **Ethernet**
  - Full duplex support for 10 and 100 Mb/s Ethernet
  - IEEE 802.3u compatible Media Independent Interface (MII) with serial management interface
  - IEEE 802.3u auto-negotiation for automatic speed selection
  - Flexible address filtering modes
  - 64-entry hash table based multicast address filtering

- ◆ **ATM SAR**
  - Can be configured as one UTOPIA level 1 interface or 1 UTOPIA level 2 interface with 2 address lines (3 PHYs max)
  - Supports 25Mb/s and faster ATM
  - Supports UTOPIA data path interface operation at speeds up to 33 MHz
  - Supports standard 53-byte ATM cells
  - Performs HEC generation and checking
  - Cell processing discards short cells and clips long cells
  - 16 cells worth of buffering
  - UTOPIA modes: 8 cell input buffer and 8 cell output buffer
  - Hardware support for CRC-32 generation and checking for AAL5
  - Hardware support for CRC-10 generation and checking
  - Virtual caching receive mechanism supports reception of any length packet without CPU intervention on up to eight simultaneously active receive channels
  - Frame Mode transmit mechanism supports transmission of any length packet without CPU intervention
- ◆ **System Features**
  - JTAG interface (IEEE Std. 1149.1 compatible)
  - 208 pin PQFP package
  - 2.5V core supply and 3.3V I/O supply
  - Up to 133 MHz pipeline frequency and up to 66 MHz bus frequency

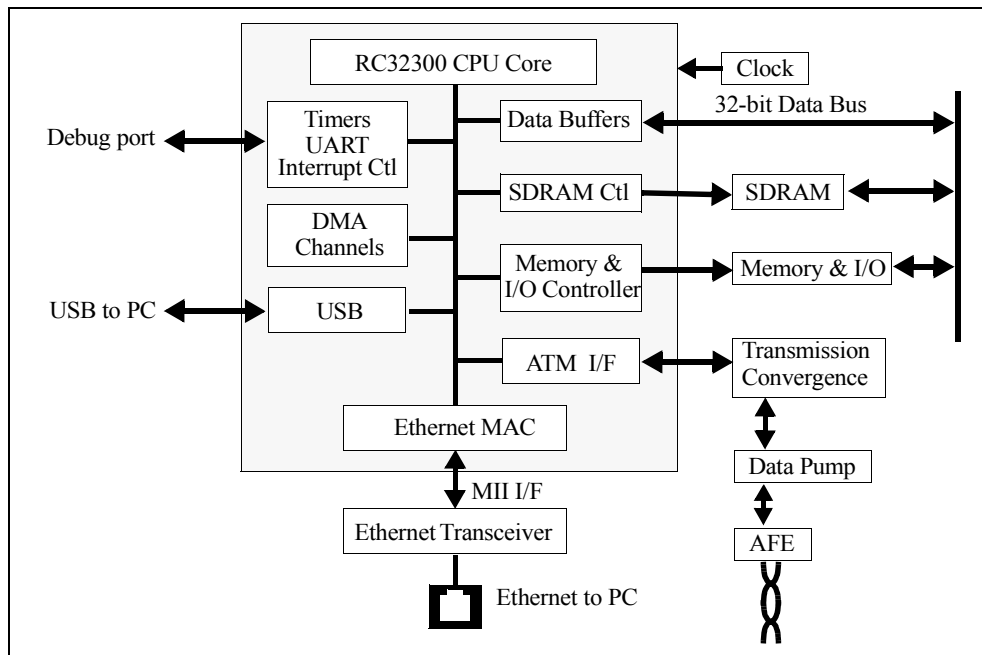


Figure 2 Example of xDSL Residential Gateway Using RC32351

## Device Overview

The RC32351 is a "System on a Chip" which contains a high performance 32-bit microprocessor. The microprocessor core is used extensively at the heart of the device to implement the most needed functionalities in software with minimal hardware support. The high performance microprocessor handles diverse general computing tasks and specific application tasks that would have required dedicated hardware. Specific application tasks implemented in software can include routing functions, fire wall functions, modem emulation, ATM SAR emulation, and others.

The RC32351 meets the requirements of various embedded communications and digital consumer applications. It is a single chip solution that incorporates most of the generic system functionalities and application specific interfaces that enable rapid time to market, very low cost systems, simplified designs, and reduced board real estate.

### CPU Execution Core

The RC32351 is built around the RC32300 32-bit high performance microprocessor core. The RC32300 implements the enhanced MIPS-II ISA and helps meet the real-time goals and maximize throughput of communications and consumer systems by providing capabilities such as a prefetch instruction, multiple DSP instructions, and cache locking. The DSP instructions enable the RC32300 to implement 33.6 and 56kbps modem functionality in software, removing the need for external dedicated hardware. Cache locking guarantees real-time performance by holding critical DSP code and parameters in the cache for immediate availability. The microprocessor also implements an on-chip MMU with a TLB, making the it fully compliant with the requirements of real time operating systems.

### Memory and IO Controller

The RC32351 incorporates a flexible memory and peripheral device controller providing support for SDRAM, Flash ROM, SRAM, dual-port memory, and other I/O devices. It can interface directly to 8-bit boot ROM for a very low cost system implementation. It enables access to high bandwidth external memory (200 MB/sec peak) at very low system costs. It also offers various trade-offs in cost / performance for the main memory architecture. The timers implemented on the RC32351 satisfy the requirements of most RTOS.

### DMA Controller

The DMA controller off-loads the CPU core from moving data among the on-chip interfaces, external peripherals, and memory. The DMA controller supports scatter / gather DMA with no alignment restrictions, appropriate for communications and graphics systems.

### Ethernet Interface

The RC32351 contains an on-chip Ethernet MAC capable of 10 and 100 Mbps line interface with an MII interface. It supports up to 4 MAC addresses. In a SOHO router, the high performance RC32300 CPU core routes the data between the Ethernet and the ATM interface. In other applications, such as high speed modems, the Ethernet interface can be used to connect to the PC.

### USB Device Interface

The RC32351 includes the industry standard USB device interface to enable consumer appliances to directly connect to the PC.

### ATM SAR

The RC32351 includes a configurable ATM SAR that supports a UTOPIA level 1 or a UTOPIA level 2 interface. The ATM SAR is implemented as a hybrid between software and hardware. A hardware block provides the necessary low level blocks (like CRC generation and checking and cell buffering) while the software is used for higher level SARing functions. In xDSL modem applications, the UTOPIA port interfaces directly to an xDSL chip set. In SOHO routers or in a line card for a Layer 3 switch, it provides access to an ATM network.

### Enhanced JTAG Interface for ICE

For low-cost In-Circuit Emulation (ICE), the RC32300 CPU core includes an Enhanced JTAG (EJTAG) interface. This interface consists of two operation modes: Run-Time Mode and Real-Time Mode.

The Run-Time Mode provides a standard JTAG interface for on-chip debugging, and the Real-Time Mode provides additional status pins—PCST[2:0]—which are used in conjunction with the JTAG pins for real-time trace information at the processor internal clock or any division of the pipeline clock.

## Thermal Considerations

The RC32351 consumes less than 1.5 W peak power and is guaranteed in an ambient temperature range of 0° to +70° C (commercial).

## Revision History

**January 7, 2002:** Initial publication.

**May 20, 2002:** Added values (in place of TBD) to Table 18, Power Consumption.

**September 19, 2002:** Added COLDRSTN Trise1 parameter to Table 5, Reset and System AC Timing Characteristics.

**December 6, 2002:** In Features section, changed UART speed from 115 Kb/s to 1.5 Mb/s.

**December 17, 2002:** Added  $V_{OH}$  parameter to Table 16, DC Electrical Characteristics.

**May 25, 2004:** In Table 7, signals MIIRXCLK and MIITXCLK, the Min and Max values for 10 Mbps Thigh1/Tlow1 were changed to 140 and 260 respectively and the Min and Max values for 100 Mbps Thigh1/Tlow1 were changed to 14.0 and 26.0 respectively.

## Pin Description Table

The following table lists the functions of the pins provided on the RC32351. Some of the functions listed may be multiplexed onto the same pin.

To define the active polarity of a signal, a suffix will be used. Signals ending with an “N” should be interpreted as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses and select lines) will be interpreted as being active, or asserted when at a logic one (high) level.

**Note:** The input pads of the RC32351 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as BRN) which, if left floating, could adversely affect the RC32351's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Name	Type	I/O Type	Description
<b>System</b>			
CLKP	I	Input	<b>System Clock input.</b> This is the system master clock input. The RISCORE 32300 pipeline frequency is a multiple (x2, x3, or x4) of this clock frequency. All other logic runs at this frequency or less.
COLDRSTN	I	STI <sup>1</sup>	<b>Cold Reset.</b> The assertion of this signal low initiates a cold reset. This causes the RC32351 state to be initialized, boot configuration to be loaded, and the internal processor PLL to lock onto the system clock (CLKP).
RSTN	I/O	Low Drive with STI	<b>Reset.</b> This bidirectional signal is either driven low or tri-stated, an external pull-up is required to supply the high state. The RC32351 drives RSTN low during a reset (to inform the external system that a reset is taking place) and then tri-states it. The external system can drive RSTN low to initiate a warm reset, and then should tri-state it.
SYSCCLKP	O	High Drive	<b>System clock output.</b> This is a buffered and delayed version of the system clock input (CLKP). All SDRAM transactions are synchronous to this clock. This pin should be externally connected to the SDRAMs and to the RC32351 SDCLKINP pin (SDRAM clock input).
<b>Memory and Peripheral Bus</b>			
MADDR[25:0]	O	[21:0] High Drive [25:22] Low Drive with STI	<b>Memory Address Bus.</b> 26-bit address bus for memory and peripheral accesses. MADDR[20:17] are used for the SODIMM data mask enables if SODIMM mode is selected. MADDR[22] Primary function: General Purpose I/O, GPIO[27]. MADDR[23] Primary function: General Purpose I/O, GPIO[28]. MADDR[24] Primary function: General Purpose I/O, GPIO[29]. MADDR[25] Primary function: General Purpose I/O, GPIO[30].
MDATA[31:0]	I/O	High Drive	<b>Memory Data Bus.</b> 32-bit data bus for memory and peripheral accesses.
BDIRN	O	High Drive	<b>External Buffer Direction.</b> External transceiver direction control for the memory and peripheral data bus, MDATA[31:0]. It is asserted low during any read transaction, and remains high during write transactions.
BOEN[1:0]	O	High Drive	<b>External Buffer Output Enable.</b> These signals provide two output enable controls for external data bus transceivers on the memory and peripheral data bus, MDATA. BOEN[0] is asserted low during external device read transactions. BOEN[1] is asserted low during SDRAM read transactions.
BRN	I	STI	<b>External Bus Request.</b> This signal is asserted low by an external master device to request ownership of the memory and peripheral bus.
BGN	O	Low Drive	<b>External Bus Grant.</b> This signal is asserted low by RC32351 to indicate that RC32351 has relinquished ownership of the local memory and peripheral bus to an external master.
WAITACKN	I	STI	<b>Wait or Transfer Acknowledge.</b> When configured as wait, this signal is asserted low during a memory and peripheral device bus transaction to extend the bus cycle. When configured as transfer acknowledge, this signal is asserted low during a memory and peripheral device bus transaction to signal the completion of the transaction.
CSN[5:0]	O	[3:0] High Drive [5:4] Low Drive	<b>Device Chip Select.</b> These signals are used to select an external device on the memory and peripheral bus during device transactions. Each bit is asserted low during an access to the selected external device. CSN[4] Primary function: General purpose I/O, GPIO[16]. CSN[5] Primary function: General purpose I/O, GPIO[17].

Table 1 Pin Descriptions (Part 1 of 7)

Name	Type	I/O Type	Description
RWN	O	High Drive	<b>Read or Write.</b> This signal indicates if the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device, a low level indicates a write to an external device.
OEN	O	High Drive	<b>Output Enable.</b> This signal is asserted low when data should be driven by an external device during device read transactions on the memory and peripheral bus.
BWEN[3:0]	O	High Drive	<b>SDRAM Byte Enable Mask or Memory and I/O Byte Write Enables.</b> These signals are used as data input/output masks during SDRAM transactions and as byte write enable signals during device controller transactions on the memory and peripheral bus. They are active low. BWEN[0] corresponds to byte lane MDATA[7:0]. BWEN[1] corresponds to byte lane MDATA[15:8]. BWEN[2] corresponds to byte lane MDATA[23:16]. BWEN[3] corresponds to byte lane MDATA[31:24].
SDCSN[1:0]	O	High Drive	<b>SDRAM Chip Select.</b> These signals are used to select the SDRAM device on the memory and peripheral bus. Each bit is asserted low during an access to the selected SDRAM.
RASN	O	High Drive	<b>SDRAM Row Address Strobe.</b> The row address strobe asserted low during memory and peripheral bus SDRAM transactions.
CASN	O	High Drive	<b>SDRAM Column Address Strobe.</b> The column address strobe asserted low during memory and peripheral bus SDRAM transactions.
SDWEN	O	High Drive	<b>SDRAM Write Enable.</b> Asserted low during memory and peripheral bus SDRAM write transactions.
CKENP	O	Low Drive	<b>SDRAM Clock Enable.</b> Asserted high during active SDRAM clock cycles. Primary function: General Purpose I/O, GPIO[21].
SDCLKINP	I	STI	<b>SDRAM Clock Input.</b> This clock input is a delayed version of SYSCLKP. SDRAM read data is sampled into the RC32351 on the rising edge of this clock.

**ATM Interface**

ATMINP[11:0]	I	STI	<b>ATM PHY Inputs.</b> These pins are the inputs for the ATM interface.
ATMIOP[1:0]	I/O	Low Drive with STI	<b>ATM PHY Bidirectional Signals.</b> These pins are the bidirectional pins for the ATM interface.
ATMOUTP[9:0]	O	Low Drive	<b>ATM PHY Outputs.</b> These pins are the outputs for the ATM interface.
TXADDR[1:0]	O	Low Drive	<b>ATM Transmit Address [1:0].</b> 2-bit address bus used for transmission in Utopia-2 mode. TXADDR[0] Primary function: General purpose I/O, GPIO[22]. TXADDR[1] Primary function: General purpose I/O, GPIO[23].
RXADDR[1:0]	O	Low Drive	<b>ATM Receive Address [1:0].</b> 2-bit address bus for receiving in Utopia-2 mode. RXADDR[0] Primary function: General purpose I/O, GPIO[24]. RXADDR[1] Primary function: General purpose I/O, GPIO[25].

**General Purpose Input/Output**

GPIO[0]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial output, U0SOUTP.
GPIO[1]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 serial input, U0SINP.
GPIO[2]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 ring indicator, U0RIN. 2nd Alternate function: JTAG boundary scan tap controller reset, JTAG_TRST_N.
GPIO[3]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data carrier detect, U0DCRN.
GPIO[4]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 0 data terminal ready, U0DTRN. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.

Table 1 Pin Descriptions (Part 2 of 7)

Name	Type	I/O Type	Description
GPIOP[5]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 data set ready, U0DSRN.
GPIOP[6]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 request to send, U0RTSN.
GPIOP[7]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: UART channel 0 clear to send, U0CTSN.
GPIOP[8]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial output, U1SOUTP. 2nd Alternate function: Active DMA channel code, DMAP[3].
GPIOP[9]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 serial input, U1SINP. 2nd Alternate function: Active DMA channel code, DMAP[2].
GPIOP[10]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[0].
GPIOP[11]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 data set ready, U1DSRN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[1].
GPIOP[12]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 request to send, U1RTSN. 2nd Alternate function: ICE PC trace status, EJTAG_PCST[2].
GPIOP[13]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: UART channel 1 clear to send, U1CTSN. 2nd Alternate function: ICE PC trace clock, EJTAG_DCLK.
GPIOP[14]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin.
GPIOP[15]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin.
GPIOP[16]	I/O	High Drive	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[4].
GPIOP[17]	I/O	High Drive	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus chip select, CSN[5].
GPIOP[18]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: External DMA device request, DMAREQN.
GPIOP[19]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: External DMA device done, DMADONEN.
GPIOP[20]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: USB start of frame, USBSOF.
GPIOP[21]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: SDRAM clock enable CKENP.
GPIOP[22]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: ATM transmit PHY address, TXADDR[0].
GPIOP[23]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: ATM transmit PHY address, TXADDR[1]. 2nd Alternate function: Active DMA channel code, DMAP[0].

Table 1 Pin Descriptions (Part 3 of 7)



Name	Type	I/O Type	Description
GPIOP[24]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: ATM receive PHY address, RXADDR[0].
GPIOP[25]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1st Alternate function: ATM receive PHY address, RXADDR[1]. 2nd Alternate function: Active DMA channel code, DMAP[1].
GPIOP[26]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin.
GPIOP[27]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[22].
GPIOP[28]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[23].
GPIOP[29]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[24].
GPIOP[30]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. Alternate function: Memory and peripheral bus address, MADDR[25].
GPIOP[31]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as a general purpose I/O pin. 1ST Alternate function: DMA finished, DMAFIN. 2nd Alternate function: EJTAG/ICE reset, EJTAG_TRST_N.
GPIOP[32]	I/O	High Drive	<b>General Purpose I/O.</b> This pin can be configured as an auxiliary general purpose I/O pin.
GPIOP[33]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as an auxiliary general purpose I/O pin.
GPIOP[34]	I/O	High Drive	<b>General Purpose I/O.</b> This pin can be configured as an auxiliary general purpose I/O pin.
GPIOP[35]	I/O	Low Drive with STI	<b>General Purpose I/O.</b> This pin can be configured as an auxiliary general purpose I/O pin.

**DMA**

DMAFIN	O	Low	<b>External DMA finished.</b> This signal is asserted low by the RC32351 when the number of bytes specified in the DMA descriptor have been transferred to or from an external device. Primary function: General Purpose I/O, GPIOP[31]. At reset, this pin defaults to primary function GPIOP[31]. 2nd Alternate function: EJTAG_TRST_N.
DMAREQN	I	STI	<b>External DMA Device Request.</b> The external DMA device asserts this pin low to request DMA service. Primary function: General purpose I/O, GPIOP[18]. At reset, this pin defaults to primary function GPIOP[18].
DMADONEN	I	STI	<b>External DMA Device Done.</b> The external DMA device asserts this signal low to inform the RC32351 that it is done with the current DMA transaction. Primary function: General purpose I/O, GPIOP[19]. At reset, this pin defaults to primary function GPIOP[19].

**USB**

USBCLKP	I	STI	<b>USB Clock.</b> 48 MHz clock input used as time base for the USB interface.
USBDN	I/O	USB	<b>USB D- Data Line.</b> This is the negative differential USB data signal.
USBDP	I/O	USB	<b>USB D+ Data Line.</b> This is the positive differential USB data signal.
USBSOF	O	Low Drive	<b>USB start of frame.</b> Primary function: General Purpose I/O, GPIOP[20]. At reset, this pin defaults to primary function GPIOP[20].

**Ethernet**

MIICOLP	I	STI	<b>MII Collision Detected.</b> This signal is asserted by the ethernet PHY when a collision is detected.
MIICRSP	I	STI	<b>MII Carrier Sense.</b> This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MIIMDCP	O	Low Drive	<b>MII Management Data Clock.</b> This signal is used as a timing reference for transmission of data on the management interface.

Table 1 Pin Descriptions (Part 4 of 7)

Name	Type	I/O Type	Description
MIIMDIOP	I/O	Low Drive with STI	<b>MII Management Data.</b> This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
MIIRXCLKP	I	STI	<b>MII Receive Clock.</b> This clock is a continuous clock that provides a timing reference for the reception of data.
MIIRXDP[3:0]	I	STI	<b>MII Receive Data.</b> This nibble wide data bus contains the data received by the ethernet PHY.
MIIRXDVP	I	STI	<b>MII Receive Data Valid.</b> The assertion of this signal indicates that valid receive data is in the MII receive data bus.
MIIRXERP	I	STI	<b>MII Receive Error.</b> The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus.
MIITXCLKP	I	STI	<b>MII Transmit Clock.</b> This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXDP[3:0]	O	Low Drive	<b>MII Transmit Data.</b> This nibble wide data bus contains the data to be transmitted.
MIITXENP	O	Low Drive	<b>MII Transmit Enable.</b> The assertion of this signal indicates that data is present on the MII for transmission.
MIITXERP	O	Low Drive	<b>MII Transmit Coding Error.</b> When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.

**EJTAG**

JTAG_TCK	I	STI	<b>JTAG Clock.</b> This is an input test clock, used to shift data into or out of the boundary scan logic. This signal requires an external resistor, listed in Table 14.
JTAG_TDI	I	STI	<b>JTAG Data Input.</b> This is the serial data shifted into the boundary scan logic. This signal requires an external resistor, listed in Table 14. This is also used to input EJTAG_DINTN during EJTAG/ICE mode. EJTAG_DINTN is an interrupt to switch the PC trace mode off.
JTAG_TDO	O	Low Drive	<b>JTAG Data Output.</b> This is the serial data shifted out from the boundary scan logic. When no data is being shifted out, this signal is tri-stated. This signal requires an external resistor, listed in Table 14. This is also used to output the EJTAG_TPC during EJTAG/ICE mode. EJTAG_TPC is the non-sequential program counter output.
JTAG_TMS	I	STI	<b>JTAG Mode Select.</b> This input signal is decoded by the tap controller to control test operation. This signal requires an external resistor, listed in Table 14.
EJTAG_PCST[0]	O	Low Drive	<b>PC trace status.</b> This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[10]. 1st Alternate function: UART channel 1 data terminal ready, U1DTRN.
EJTAG_PCST[1]	O	Low Drive	<b>PC trace status.</b> This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[11]. At reset, this pin defaults to primary function GPIOP[11]. 1st Alternate function: UART channel 1 data set ready, U1DSRN.
EJTAG_PCST[2]	O	Low Drive	<b>PC trace status.</b> This bus gives the PC trace status information during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[12]. 1st Alternate function: UART channel 1 request to send, U1RTSN.
EJTAG_DCLK	O	Low Drive	<b>PC trace clock.</b> This is used to capture address and data during EJTAG/ICE mode. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary function: General Purpose I/O, GPIOP[13]. 1st Alternate function: UART channel 1 clear to send, U1CTSN.

Table 1 Pin Descriptions (Part 5 of 7)

Name	Type	I/O Type	Description
EJTAG_TRST_N	I	STI	<b>EJTAG Test Reset.</b> EJTAG_TRST_N is an active-low signal for asynchronous reset of only the EJTAG/ICE controller. EJTAG_TRST_N requires an external pull-up on the board. EJTAG/ICE enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. This signal requires an external resistor, listed in Table 14. Primary: General Purpose I/O, GPIOP[31] 1st Alternate function: DMA finished output, DMAFIN.
JTAG_TRST_N	I	STI	<b>JTAG Test Reset.</b> JTAG_TRST_N is an active-low signal for asynchronous reset of only the JTAG boundary scan controller. JTAG_TRST_N requires an external pull-down on the board that will hold the JTAG boundary scan controller in reset when not in use if selected. JTAG reset enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[2]. 1st Alternate function: UART channel 0 ring indicator, U0RIN.

**Debug**

INSTP	O	Low Drive	<b>Instruction or Data Indicator.</b> This signal is driven high during CPU instruction fetches and low during CPU data transactions on the memory and peripheral bus.
CPUP	O	Low Drive	<b>CPU or DMA Transaction Indicator.</b> This signal is driven high during CPU transactions and low during DMA transactions on the memory and peripheral bus if CPU/DMA Transaction Indicator Enable is enabled. CPU/DMA Status mode enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[4]. 1st Alternate function: UART channel 0 data terminal ready U0DTRN.
DMAP[0]	O	Low Drive	<b>Active DMA channel code.</b> DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[23]. 1st Alternate function: TXADDR[1].
DMAP[1]	O	Low Drive	<b>Active DMA channel code.</b> DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[25]. 1st Alternate function: RXADDR[1].
DMAP[2]	O	Low Drive	<b>Active DMA channel code.</b> DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[9]. 1st Alternate function: U1SINP.
DMAP[3]	O	Low Drive	<b>Active DMA channel code.</b> DMA debug enable is selected during reset using the boot configuration and overrides the selection of the Primary and Alternate functions. Primary function: General Purpose I/O, GPIOP[8]. 1st Alternate function: U1SOUTP.

**UART**

U0SOUTP	I	STI	<b>UART channel 0 serial transmit.</b> Primary function: General Purpose I/O, GPIOP[0]. At reset, this pin defaults to primary function GPIOP[0].
U0SINP	I	STI	<b>UART channel 0 serial receive.</b> Primary function: General Purpose I/O, GPIOP[1]. At reset, this pin defaults to primary function GPIOP[1].
U0RIN	I	STI	<b>UART channel 0 ring indicator.</b> Primary function: General Purpose I/O, GPIOP[2]. At reset, this pin defaults to primary function GPIOP[2] if JTAG reset enable is not selected during reset using the boot configuration. 2nd Alternate function: JTAG boundary scan reset, JTAG_TRST_N.
U0DCRN	I	STI	<b>UART channel 0 data carrier detect.</b> Primary function: General Purpose I/O, GPIOP[3]. At reset, this pin defaults to primary function GPIOP[3].

Table 1 Pin Descriptions (Part 6 of 7)

Name	Type	I/O Type	Description
U0DTRN	O	Low Drive	<b>UART channel 0 data terminal ready.</b> Primary function: General Purpose I/O, GPIO[4]. At reset, this pin defaults to primary function GPIO[4] if CPU/DMA Status Mode enable is not selected during reset using the boot configuration. 2nd Alternate function: CPU or DMA transaction indicator, CPUP.
U0DSRN	I	STI	<b>UART channel 0 data set ready.</b> Primary function: General Purpose I/O, GPIO[5]. At reset, this pin defaults to primary function GPIO[5].
U0RTSN	O	Low Drive	<b>UART channel 0 request to send.</b> Primary function: General Purpose I/O, GPIO[6]. At reset, this pin defaults to primary function GPIO[6].
U0CTSN	I	STI	<b>UART channel 0 clear to send.</b> Primary function: General Purpose I/O, GPIO[7]. At reset, this pin defaults to primary function GPIO[7].
U0SOUTP	O	Low Drive	<b>UART channel 1 serial transmit.</b> Primary function: General Purpose I/O, GPIO[8]. At reset, this pin defaults to primary function GPIO[8] if DMA Debug enable is not selected during reset using the boot configuration. 2nd Alternate function: DMA channel, DMAP[3].
U1SINP	I	STI	<b>UART channel 1 serial receive.</b> Primary function: General Purpose I/O, GPIO[9]. At reset, this pin defaults to primary function GPIO[9] if DMA Debug enable is not selected during reset using the boot configuration. 2nd Alternate function: DMA channel, DMAP[2].
U1DTRN	O	Low Drive	<b>UART channel 1 data terminal ready.</b> Primary function: General Purpose I/O, GPIO[10]. At reset, this pin defaults to primary function GPIO[10] if ICE Interface enable is not selected during reset using the boot configuration. Alternate function: PC trace status bit 0, EJTAG_PCST[0].
U1DSRN	I	STI	<b>UART channel 1 data set ready.</b> Primary function: General Purpose I/O, GPIO[11]. At reset, this pin defaults to primary function GPIO[11] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace status bit 1, EJTAG_PCST[1].
U1RTSN	O	Low Drive	<b>UART channel 1 request to send.</b> Primary function: General Purpose I/O, GPIO[12]. At reset, this pin defaults to primary function GPIO[12] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace status bit 2, EJTAG_PCST[2].
U1CTSN	I	STI	<b>UART channel 1 clear to send.</b> Primary function: General Purpose I/O, GPIO[13]. At reset, this pin defaults to primary function GPIO[13] if ICE Interface enable is not selected during reset using the boot configuration. 2nd Alternate function: PC trace clock, EJTAG_DCLK.

Table 1 Pin Descriptions (Part 7 of 7)

<sup>1</sup>. Schmitt Trigger Input.

## Boot Configuration Vector

The boot configuration vector is read into the RC32351 during cold reset. The vector defines parameters in the RC32351 that are essential to operation when cold reset is complete.

The encoding of boot configuration vector is described in Table 2, and the vector input is illustrated in Figure 6.

Signal	Name/Description
MDATA[2:0]	<b>Clock Multiplier.</b> This field specifies the value by which the system clock (CLKP) is multiplied internally to generate the CPU pipeline clock. 0x0 - multiply by 2 0x1 - multiply by 3 0x2 - multiply by 4 0x3 - reserved 0x4 - reserved 0x5 - reserved 0x6 - reserved 0x7 - reserved
MDATA[3]	<b>Endian.</b> This bit specifies the endianness of RC32351. 0x0 - little endian 0x1 - big endian
MDATA[4]	<b>Reserved.</b> Must be set to 0.
MDATA[5]	<b>Debug Boot Mode.</b> When this bit is set, the RC32351 begins executing from address 0xFF20_0200 rather than 0xBFC0_0000 following a reset. 0x0 - regular mode (processor begins executing at 0xBFC0_0000) 0x1 - debug boot mode (processor begins executing at 0xFF20_0200)
MDATA[7:6]	<b>Boot Device Width.</b> This field specifies the width of the boot device. 0x0 - 8-bit boot device width 0x1 - 16-bit boot device width 0x2 - 32-bit boot device width 0x3 - reserved
MDATA[8]	<b>EJTAG/ICE Interface Enable.</b> When this bit is set, Alternate 2 pin functions EJTAG_PCST[2:0], EJTAG_DCLK, and EJTAG_TRST_N are selected. 0x0 - GPIO[31, 13:10] pins behaves as GPIO 0x1 - GPIO[31] pin behaves as EJTAG_TRST_N, GPIO[12:10] pins behave as EJTAG_PCST[2:0], and GPIO[13] pin behaves as EJTAG_DCLK
MDATA[9]	<b>Fast Reset.</b> When this bit is set, RC32351 drives RSTN for 64 clock cycles, used during test only. Clear this bit for normal operation. 0x0 - Normal reset: RC32351 drives RSTN for minimum of 4096 clock cycles 0x1 - Fast Reset: RC32351 drives RSTN for 64 clock cycles (test only)
MDATA[10]	<b>DMA Debug Enable.</b> When this bit is set, Alternate 2 pin function, DMAP is selected. DMAP provides the DMA channel number during memory and peripheral bus DMA transactions. 0x0 - GPIO[8, 9, 25, 23] pins behave as GPIO 0x1 - GPIO[8, 9, 25, 23] pins behave as DMAP[3:0]
MDATA[11]	<b>Hold SYSCLKP Constant.</b> For systems that do not require a SYSCLKP output and can instead use CLKP, setting this bit to a one causes the SYSCLKP output to be held at a constant level. This may be used to reduce EMI. 0x0 - Allow SYSCLKP to toggle 0x1 - Hold SYSCLKP constant
MDATA[12]	<b>JTAG Boundary Scan Reset Enable.</b> When this bit is set, Alternate 2 pin function, JTAG_TRST_N is selected. 0x0 - GPIO[2] pin behaves as GPIO 0x1 - GPIO[2] pin behaves as JTAG_TRST_N
MDATA[13]	<b>CPU / DMA Transaction Indicator Enable.</b> When this bit is set, Alternate 2 pin function, CPUP is selected. 0x0 - GPIO[4] pin behaves as GPIO 0x1 - GPIO[4] pin behaves as CPUP
MDATA[15:14]	<b>Reserved.</b> These pins must be driven low during boot configuration.

Table 2 Boot Configuration Vector Encoding

# Logic Diagram

The following Logic Diagram shows the primary pin functions of the RC32351.

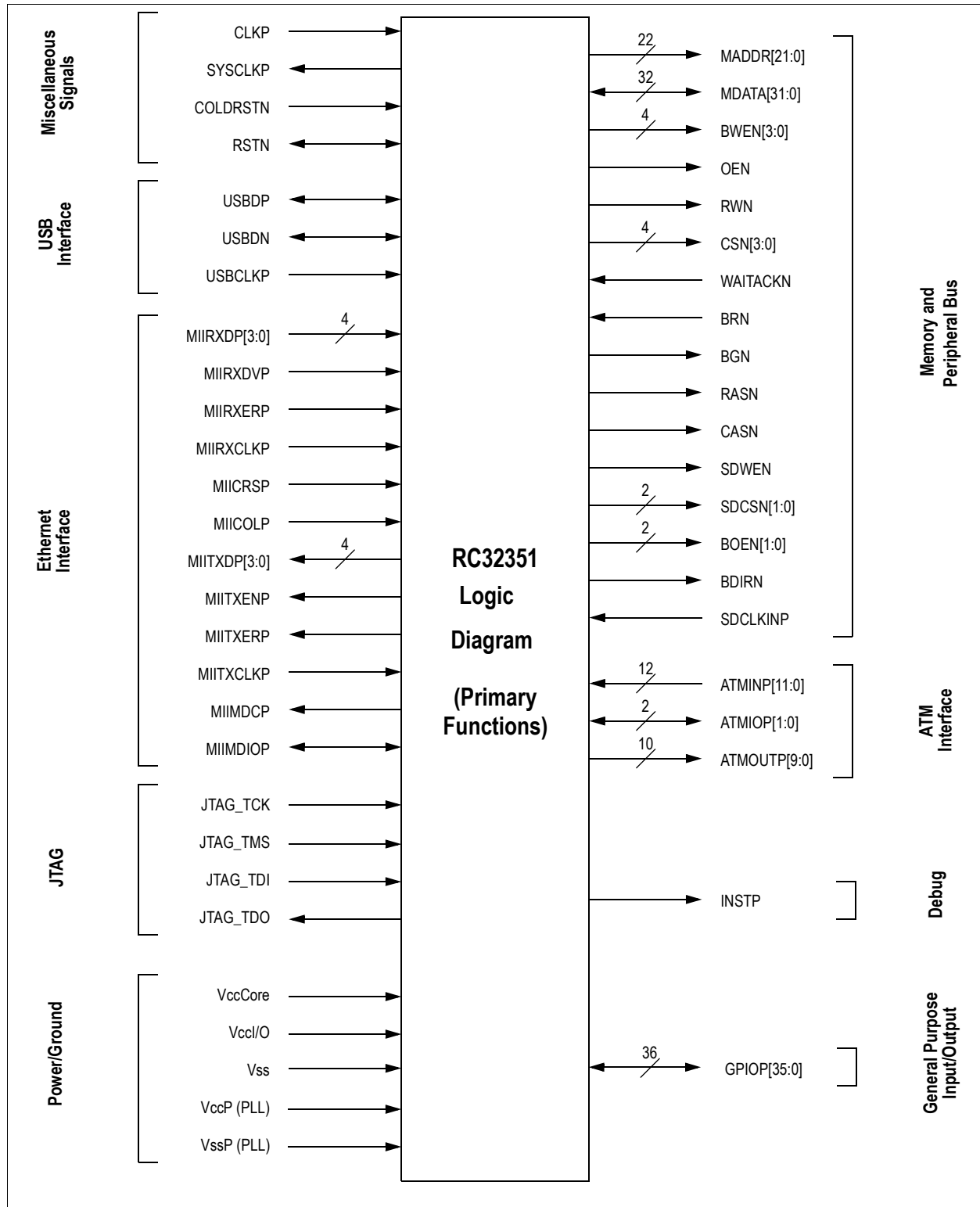


Figure 3 Logic Diagram

## Clock Parameters

( $T_a = 0^\circ\text{C}$  to  $+70^\circ\text{C}$  Commercial,  $V_{cc\ I/O} = +3.3\text{V}\pm 5\%$ ,  $V_{cc\ Core}$  and  $V_{cc\ P} = +2.5\text{V}\pm 5\%$ )

Parameter	Symbol	Reference Edge	RC32351 100MHz		RC32351 133MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max		
Internal CPU pipeline clock <sup>1</sup>	Frequency	none	100	100	100	133	MHz	Figure 4
CLKP <sup>2,3,4</sup>	Frequency	none	25	50	25	67	MHz	
	Tperiod1		20	40	15	40	ns	
	Thigh1		10	—	6	—	ns	
	Tlow1		10	—	6	—	ns	
	Trise1		—	3	—	3	ns	
	Tfall1		—	3	—	3	ns	
	Tjitter		—	$\pm 250$	—	$\pm 250$	ps	

<sup>1</sup> The CPU pipeline clock speed is selected during cold reset by the boot configuration vector (see Table 2).  
<sup>2</sup> Ethernet clock (MIIRXCLKP and MIITXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.  
<sup>3</sup> USB clock (USBCLKP) frequency must be less than CLKP frequency.  
<sup>4</sup> ATM Utopia clock (RXCLKP and TXCLKP) frequency must be equal to or less than 1/2 CLKP frequency.

Table 3 Clock Parameters

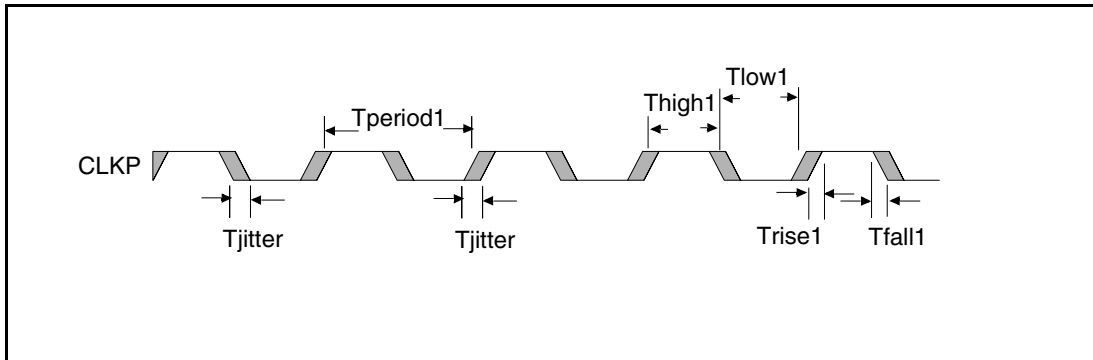


Figure 4 Clock Parameters Waveform

## AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

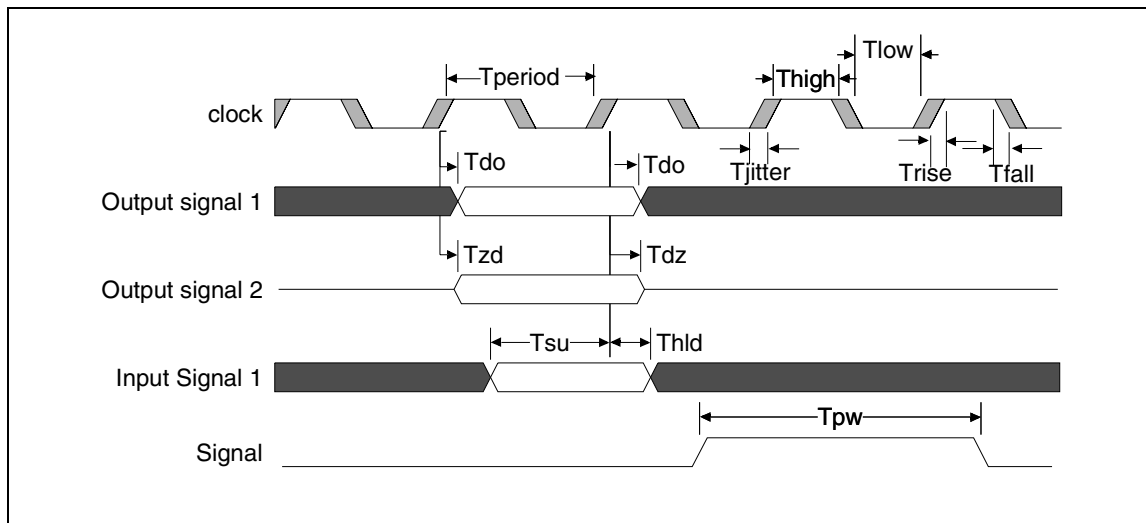


Figure 5 AC Timing Definitions Waveform

Symbol	Definition
Tperiod	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active.

Table 4 AC Timing Definitions



## AC Timing Characteristics

(Ta = 0°C to +70°C Commercial, V<sub>cc</sub> I/O = +3.3V±5%, V<sub>cc</sub> Core = +2.5V±5%, V<sub>cc</sub>P = +2.5V±5%)

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
<b>Reset and System</b>									
COLDRSTN	Tpw1	none	110	—	110	—	ms		Figure 6 Figure 7
	Trise1	none	—	5.0	—	5.0	ns		
RSTN <sup>1</sup>	Tdo2	CLKP rising	4.0	10.7	4.0	10.7	ns		
MDATA[15:0] Boot Configuration Vector	Thld3	COLDRSTN rising	3	—	3	—	ns		
INSTP	Tdo	CLKP rising	5	8	5.0	8.0	ns		
CPUP	Tdo	CLKP rising	3.5	7	3.5	7.0	ns		
DMAP	Tdo	CLKP rising	3.5	6.6	3.5	6.6	ns		
DMAREQN <sup>2</sup>	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMADONEN <sup>2</sup>	Tpw	none	(CLKP+7)	—	(CLKP+7)	—	ns		
DMAFIN	Tdo	CLKP rising	3.5	5.9	3.5	5.9	ns		
BRN	Tsu	CLKP rising	1.6	—	1.6	—	ns		
	Thld		0	—	0	—	ns		
BGN	Tdo	CLKP rising	3.3	5.8	3.3	5.8	ns		
<sup>1</sup> RSTN is a bidirectional signal. It is treated as an asynchronous input. <sup>2</sup> DMAREQN and DMADONEN minimum pulse width equals the CLKP period plus 7ns.									

Table 5 Reset and System AC Timing Characteristics

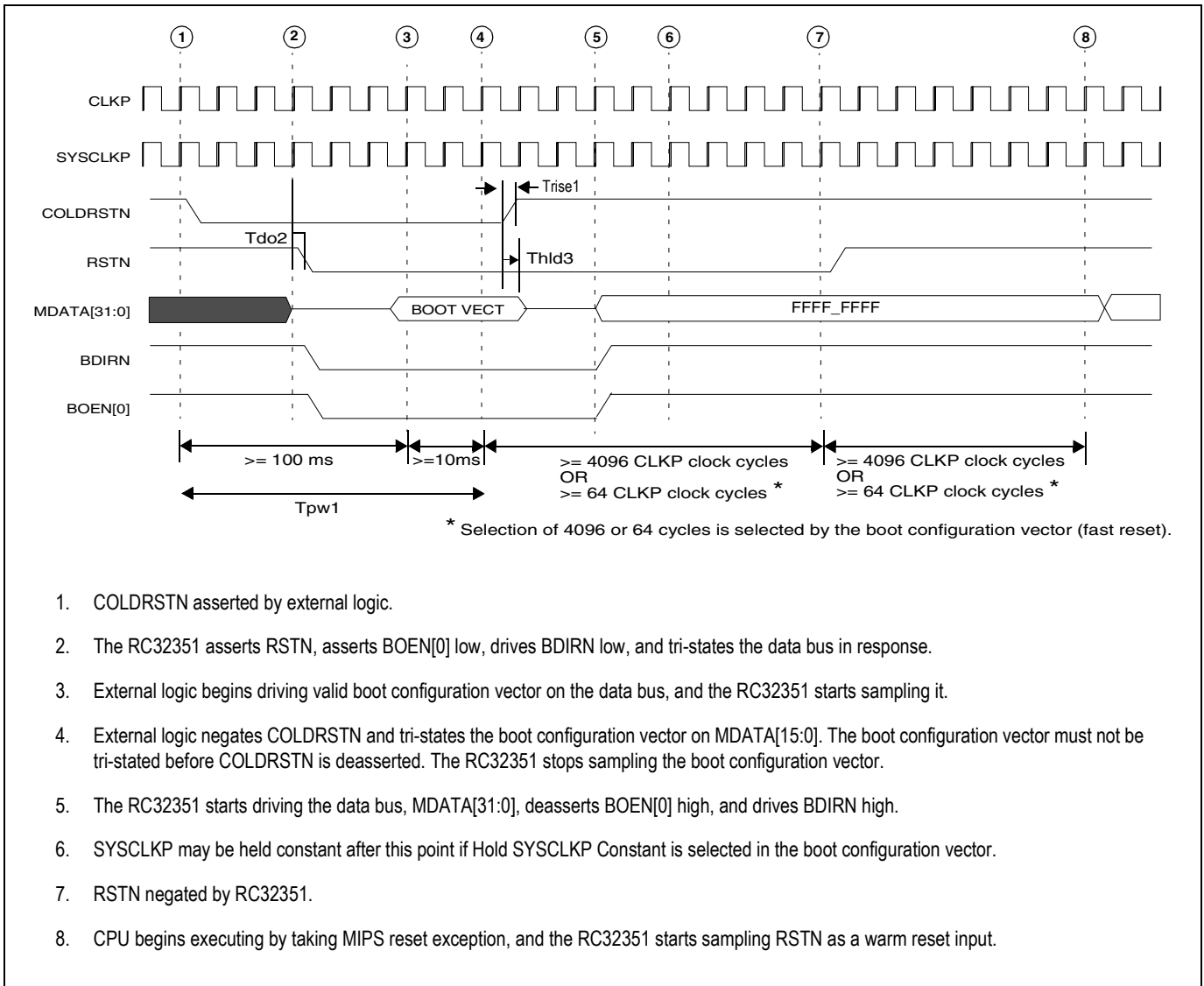


Figure 6 Cold Reset AC Timing Waveform

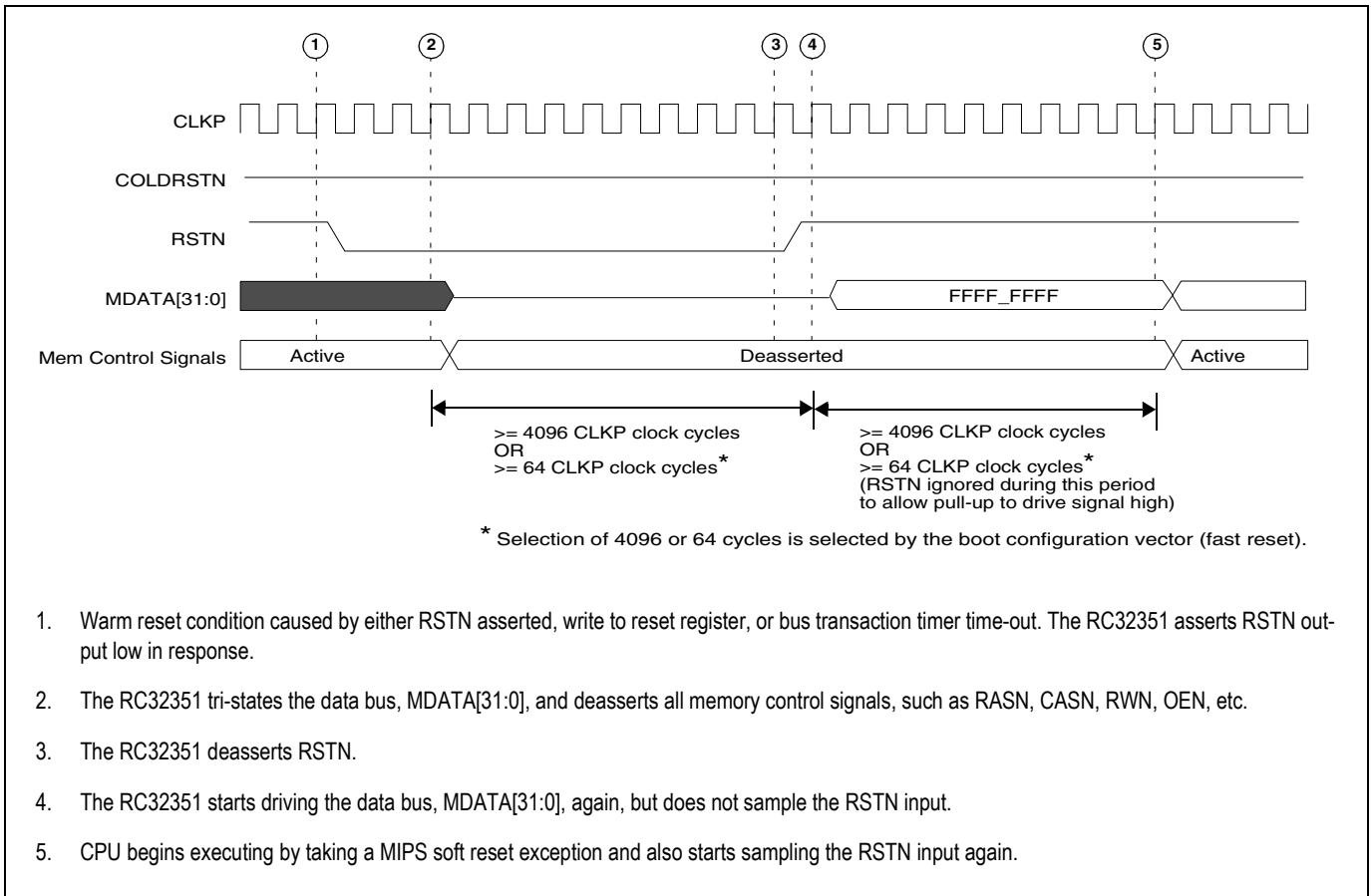


Figure 7 Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
<b>Memory and Peripheral Bus - SDRAM Access</b>									
MDATA[31:0]	Tsu1	SDCLKINP rising	2.5	—	2.5	—	ns		Figure 8 Figure 9 Figure 10
	Thd1		1.2	—	1.2	—	ns		
	Tdo1	SYSCLKP rising	1.2	5.8	1.2	5.8	ns		
	Tdz1		—	5.0	—	5.0	ns		
	Tzd1		1.0	—	1.0	—	ns		
MADDR[20:2], BWEN[3:0]	Tdo2	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
CASN, RASN, SDCSN[1:0], SDWEN	Tdo3	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
CKENP	Tdo4	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
BDIRN	Tdo5	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
BOEN[1:0]	Tdo6	SYSCLKP rising	1.2	5.3	1.2	5.3	ns		
SYSCLKP rising	Tdo7	CLKP rising	0.5	5.0	0.5	5.0	ns		
SDCLKINP	Tperiod8	none	20	50	15	50	ns		
	Thigh8, Tlow8		10	—	6.0	—	ns		
	Trise8, Tfall8		—	3.0	—	3.0	ns		
	Tdelay8	SYSCLKP rising	0	4.8	0	4.8	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
<b>Memory and Peripheral Bus - Device Access</b>									
MDATA[31:0]	Tsu1	CLKP rising	2.5	—	2.5	—	ns		Figure 11 Figure 12
	Thld1		1.5	—	1.5	—	ns		
	Tdo1		2.0	6.5	2.0	6.5	ns		
	Tdz1		—	9.0	—	9.0	ns		
	Tzd1		2.0	—	2.0	—	ns		
WAITACKN, BRN	Tsu	CLKP rising	2.5	—	2.5	—	ns		
	Thld		1.5	—	1.5	—	ns		
MADDR[21:0]	Tdo2	CLKP rising	2.0	6.0	2.0	6.0	ns		
	Tdz2		—	9.0	—	9.0	ns		
	Tzd2		2.0	—	2.0	—	ns		
MADDR[25:22]	Tdo3	CLKP rising	2.5	6.5	2.5	6.5	ns		
	Tdz3		—	9.0	—	9.0	ns		
	Tzd3		2.0	—	2.0	—	ns		
BDIRN, BOEN[0]	Tdo4	CLKP rising	2.0	6.0	2.0	6.0	ns		
	Tdz4		—	9.0	—	9.0	ns		
	Tzd4		2.0	—	2.0	—	ns		
BGN, BWEN[3:0], OEN, RWN	Tdo5	CLKP rising	2.0	6.0	2.0	6.0	ns		
	Tdz5		—	9.0	—	9.0	ns		
	Tzd5		2.0	—	2.0	—	ns		
CSN[3:0]	Tdo6	CLKP rising	1.7	5.0	1.7	5.0	ns		
	Tdz6		—	9.0	—	9.0	ns		
	Tzd6		2.0	—	2.0	—	ns		
CSN[5:4]	Tdo7	CLKP rising	2.5	6.0	2.5	6.0	ns		
	Tdz7		—	9.0	—	9.0	ns		
	Tzd7		2.0	—	2.0	—	ns		

Table 6 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

**Note:** The RC32351 provides bus turnaround cycles to prevent bus contention when going from a read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32351 are both driving. See Chapter 10, "Device Controller," Chapter 11, "Synchronous DRAM Controller," and Chapter 12, "Bus Arbitration" in the RC32351 User Reference Manual.

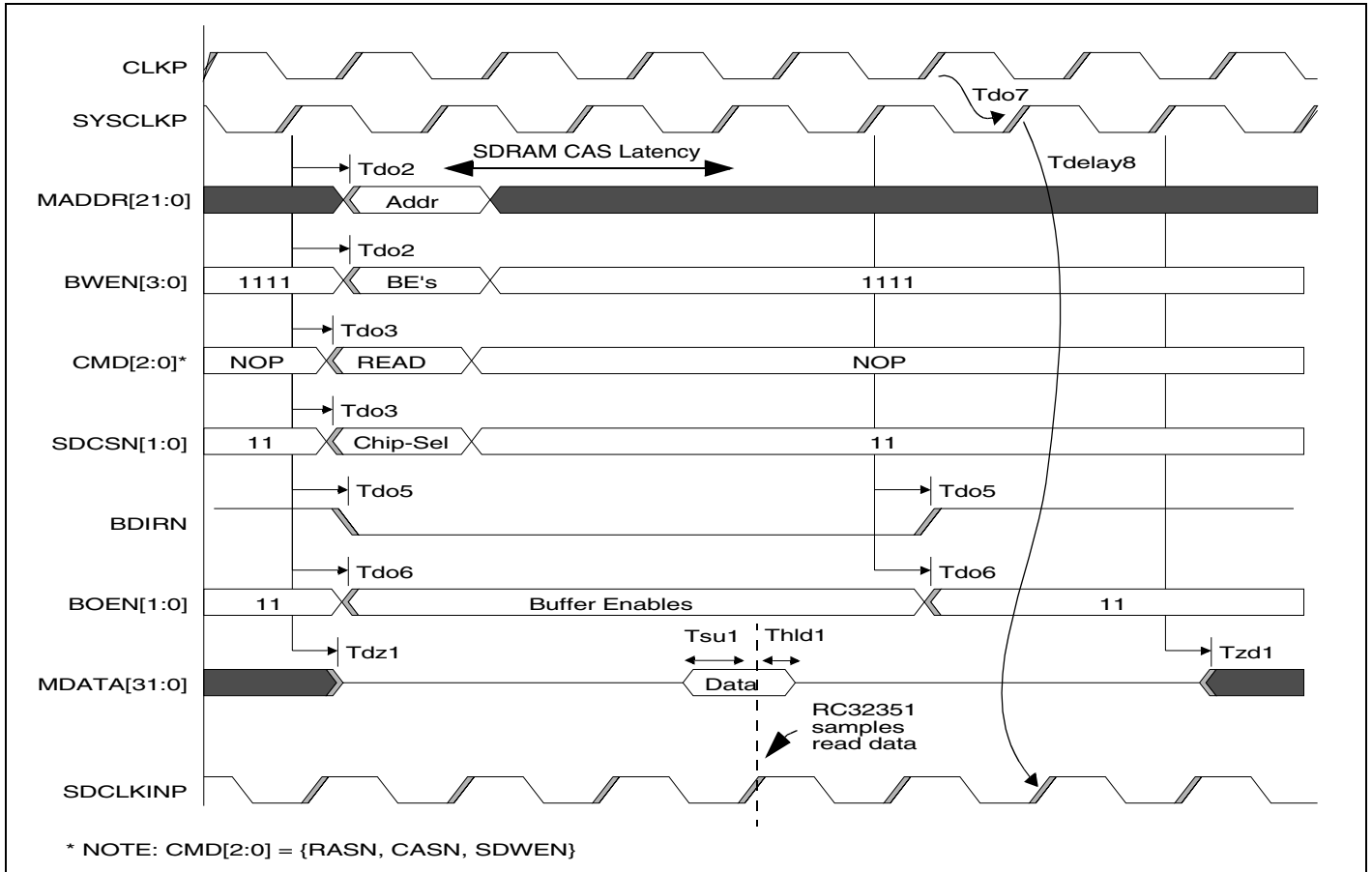


Figure 8 Memory and Peripheral Bus AC Timing Waveform - SDRAM Read Access

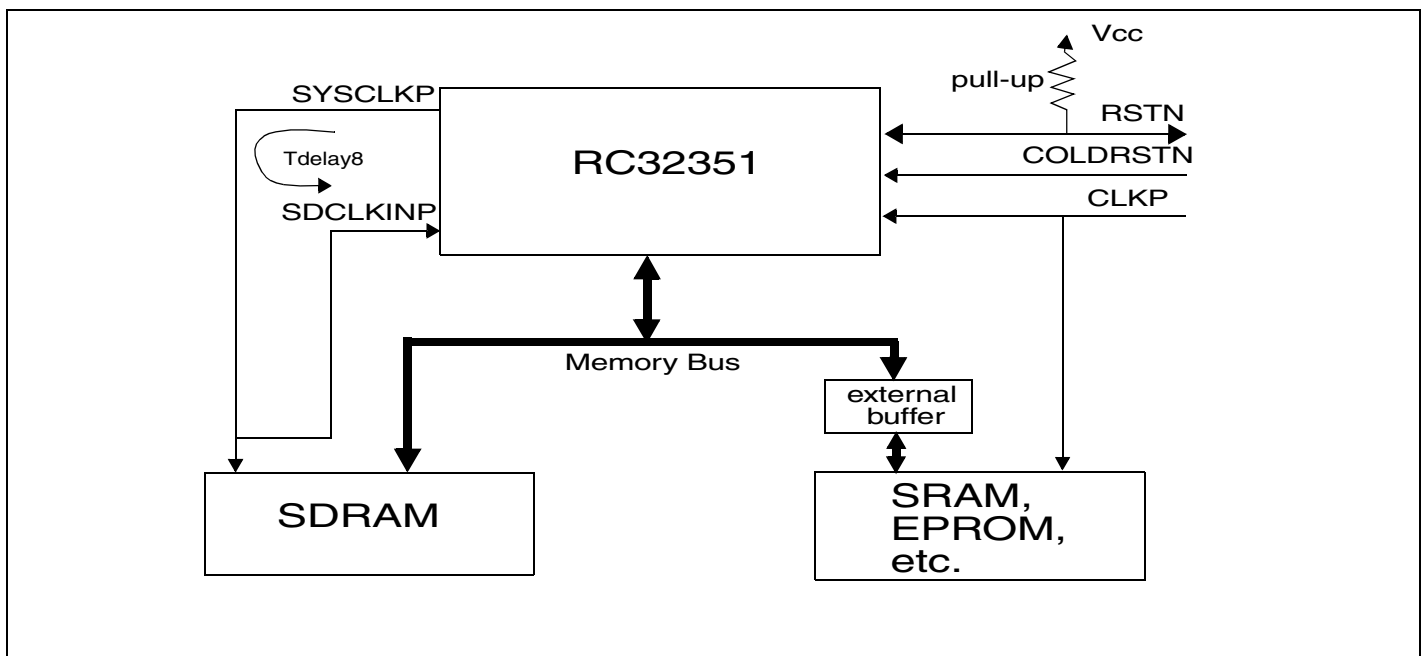


Figure 9 SYSCLKP - SDCLKINP Relationship

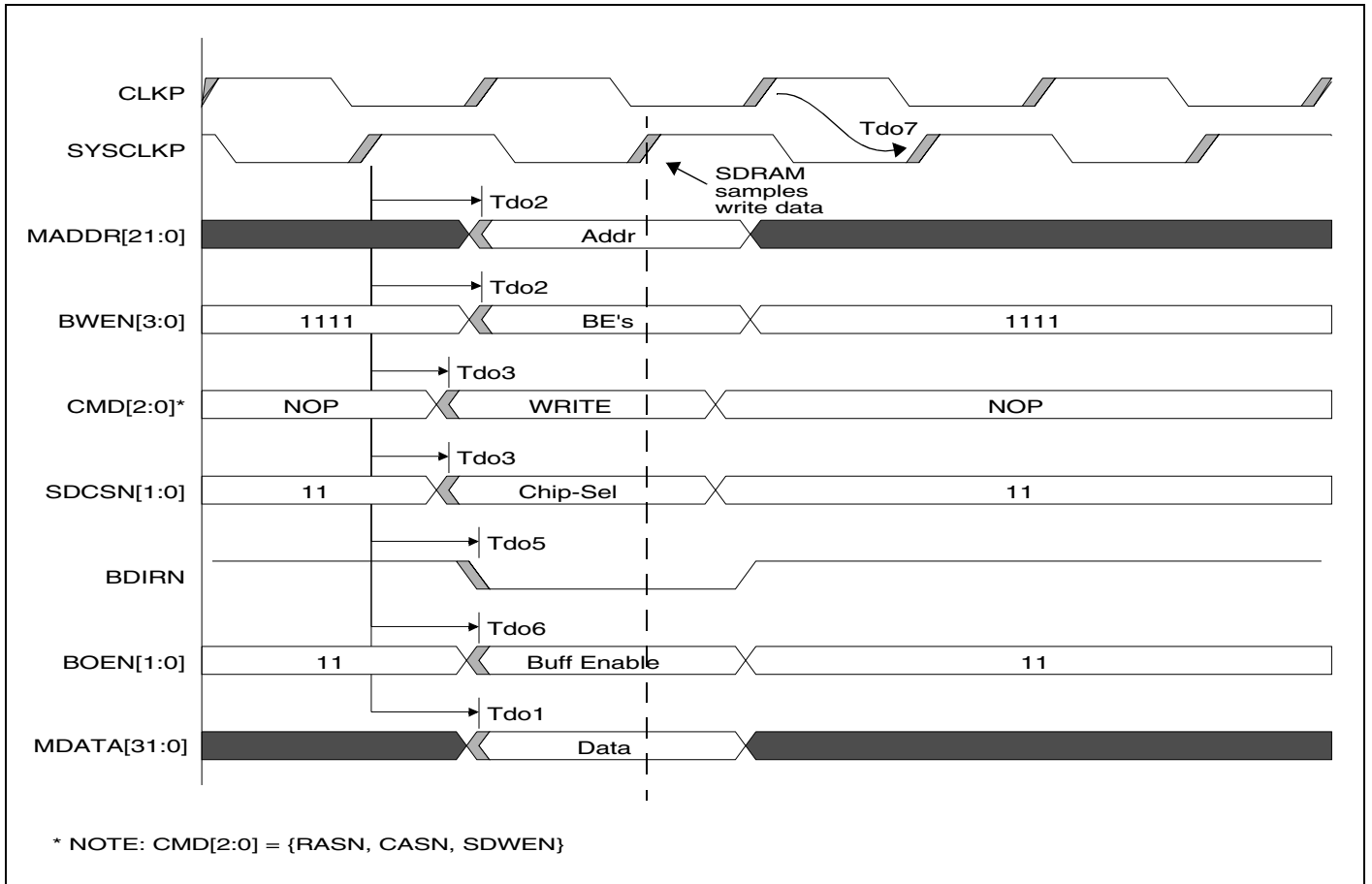


Figure 10 Memory and Peripheral Bus AC Timing Waveform - SDRAM Write Access

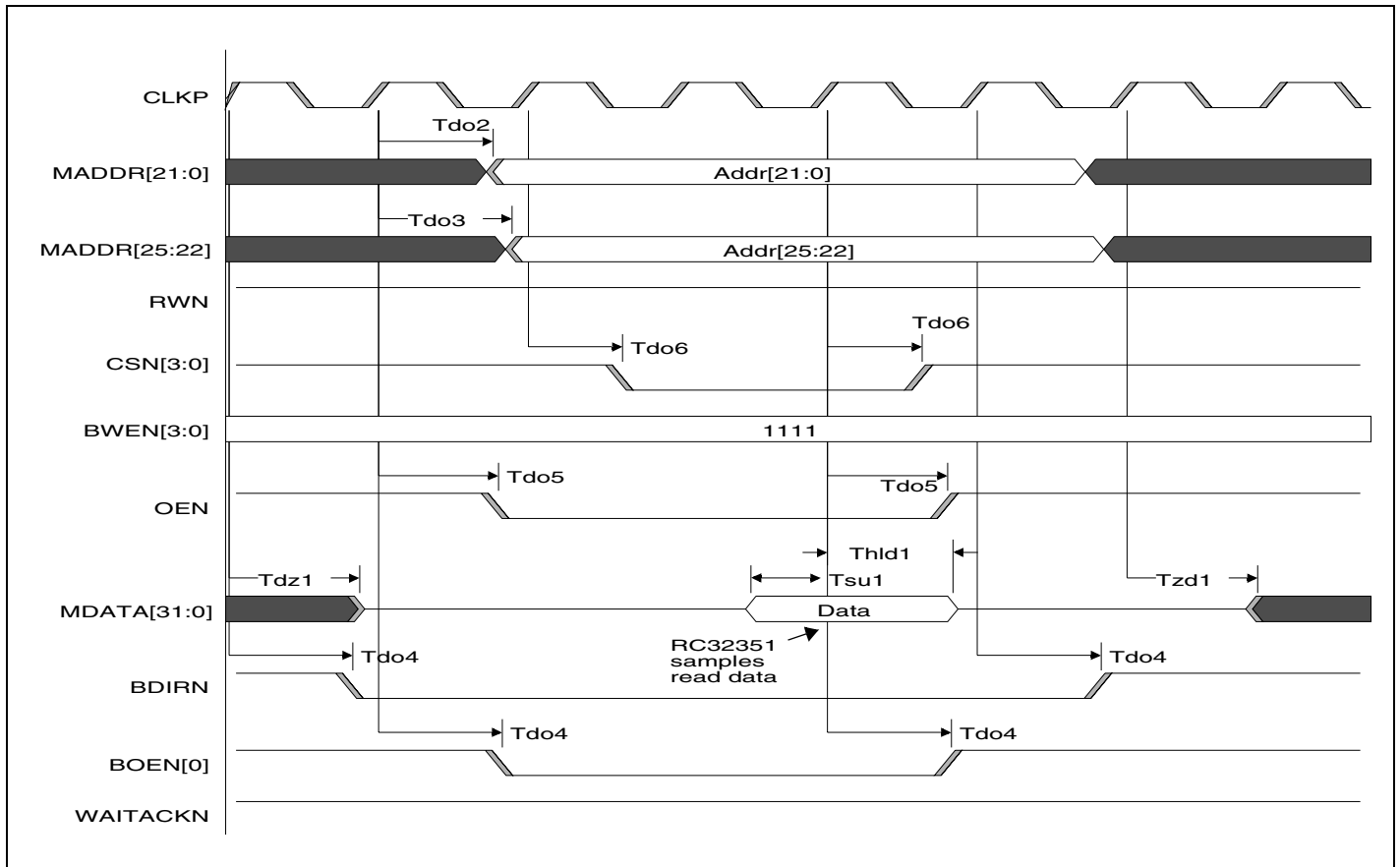


Figure 11 Memory and Peripheral Bus AC Timing Waveform - Device Read Access



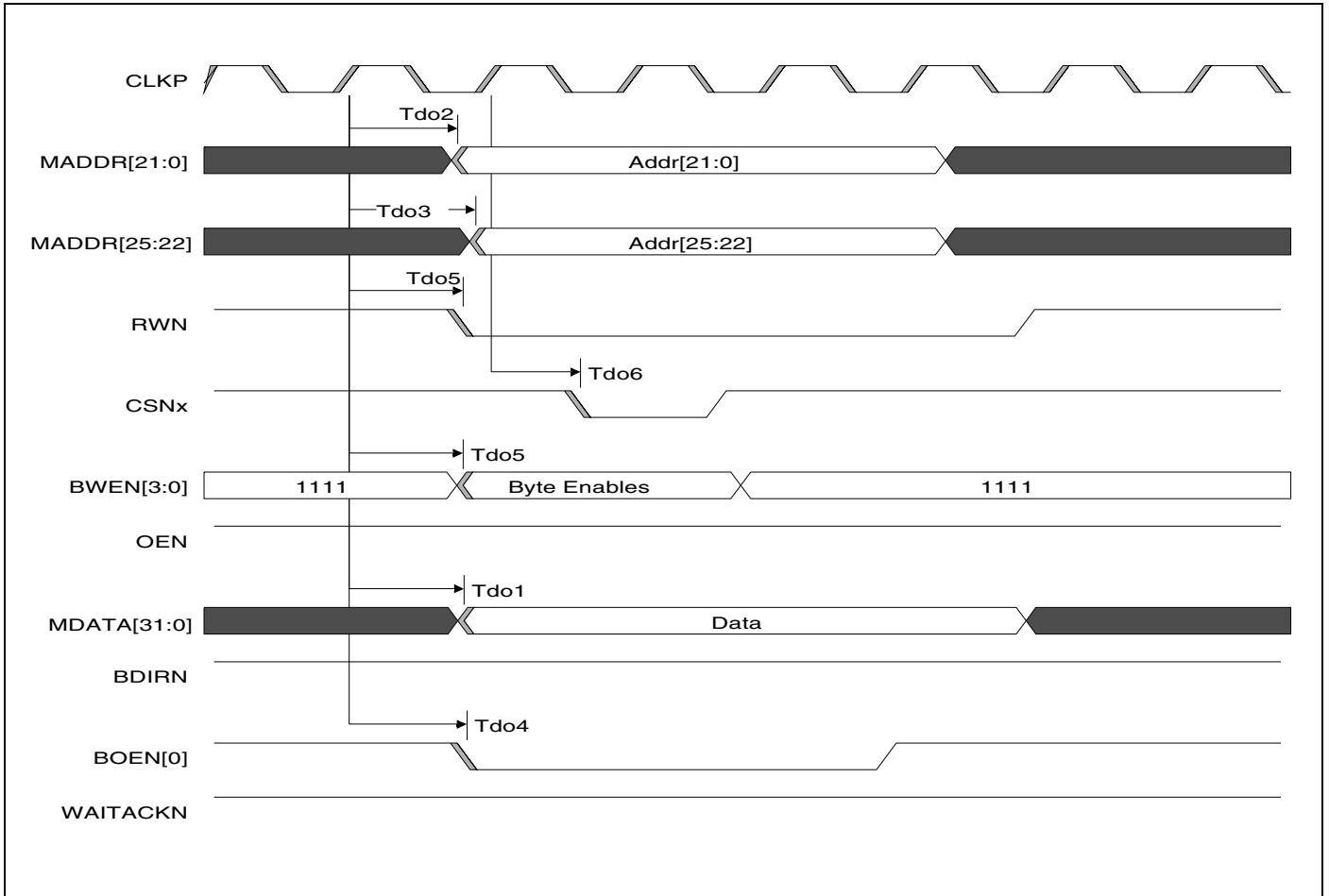


Figure 12 Memory AC and Peripheral Bus Timing Waveform - Device Write Access

Signal	Symbol	Reference Edge	100MHz		133MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max			
Ethernet <sup>1,2</sup>									
MIIRXCLKP, MIITXCLKP	Tperiod1	none	399.96	400.04	399.96	400.04	ns	10 Mbps	Figure 13
	Thigh1, Tlow1		140	260	140	260	ns		
	Trise1, Tfall1		—	3	—	3	ns		
MIIRXCLKP, MIITXCLKP	Tperiod1	none	39.996	40.004	39.996	40.004	ns	100 Mbps	
	Thigh1, Tlow1		14	26	14	26	ns		
	Trise1, Tfall1		—	2	—	2	ns		
MIIRXDP[3:0], MIIRXDVP, MIIRXERP	Tsu2	MIIRXCLKP rising	5	—	5	—	ns		
	Thld2		3	—	3	—	ns		
MIITXDP[3:0], MIITXENP, MIITXERP	Tdo3	MIITXCLKP rising	7	13	7	13	ns		
MIIMDCP	Tperiod4	none	30	—	30	—	ns		
	Thigh4, Tlow4		14	—	14	—	ns		
	Trise4		—	11	—	11	ns		
	Tfall4		—	8	—	8	ns		
MIIMDIOP	Tsu5	MIIMDCP rising	6	—	6	—	ns		
	Thld5		0.5	—	0.5	—	ns		
	Tdo5		3	7	3	7	ns		
<sup>1</sup> Ethernet clock (MIIRXCLKP and MIITXCLKP) frequency must be equal to or less than 1/2 CLKP frequency. <sup>2</sup> MIICOLP and MIICRSP are asynchronous signals.									

Table 7 Ethernet AC Timing Characteristics