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3.3 VOLT M13 MULTIPLEXER
IDT82V8313

Version 3
June 3, 2004

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2. A critical component is any components of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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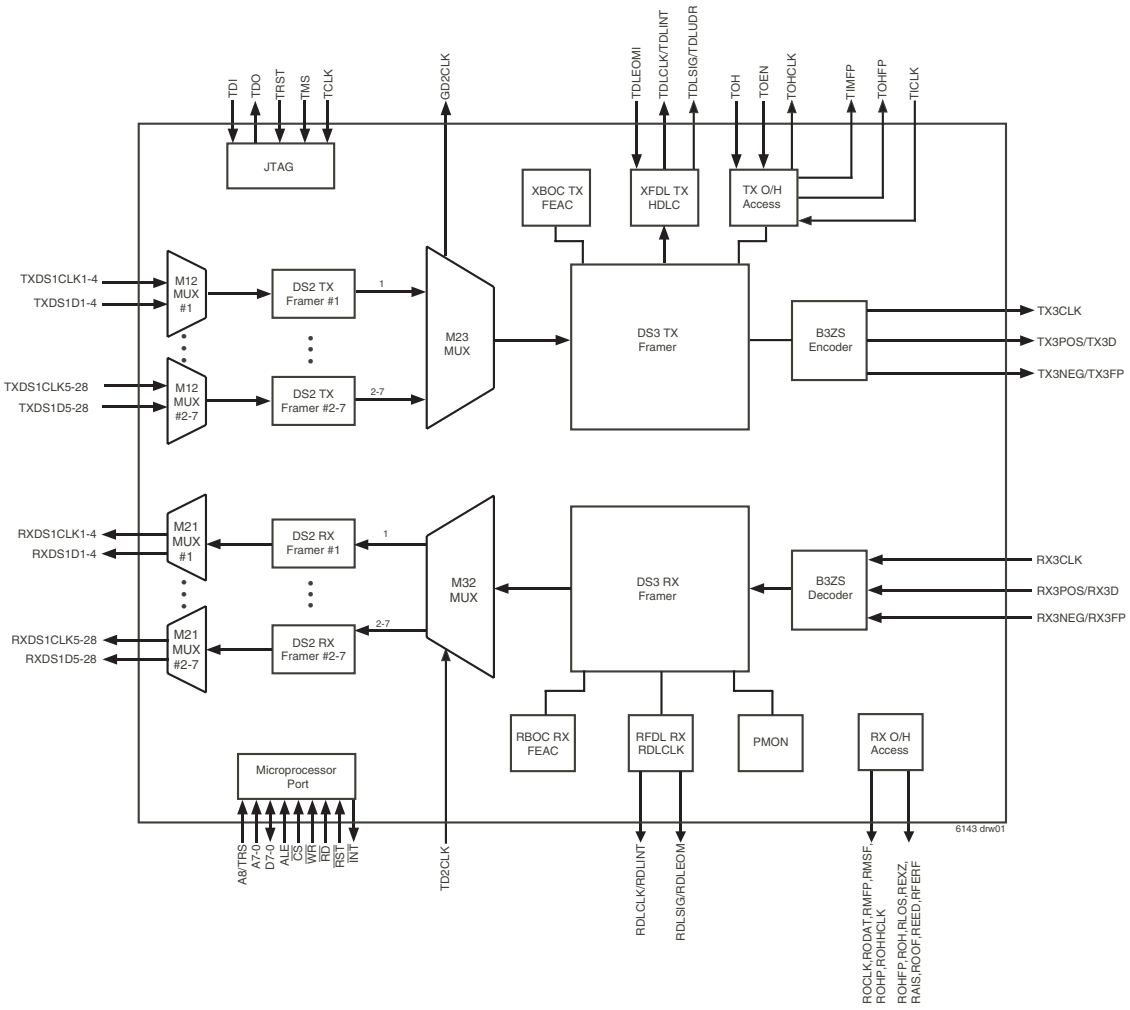
3.3 VOLT M13 MULTIPLEXER

IDT82V8313

FEATURES:

- Full featured single chip M13-ideal for upgrading existing multi-line T1/E1 line cards to single line channelized T3 service
- Small footprint 17mm x 17mm BGA package and 208 pin PQFP packages available
- 3.3V operation with 5V tolerant I/O
- 28 independent DS1 clock inputs each with programmable clock edge adapter
- 28 independent DS1 outputs eatch with programmable clock edge adapter
- M12 bypass for direct input of DS2 in to the M23 multiplexer
- Programmable clock edge
- Supports M23 or C-bit parity format formats
- G.747 formats for E1 to be multiplexed onto a DS3
- DS2 LOF detectors and DS2 AIS DS2 X-bit access
- DS2 transmit/receive X-bit control/status
- DS2 F, M, and X bit insertion
- DS2 FERF and AIS under microprocessor control
- Transmission of RAI and reserved bit under microprocessor control
- Programmable preemptive inversion of C-bits for remote loopback
- DS3 idle signal generators
- DS3 LOS, LOF, P-bit Parity, C-bit Parity, AIS and idle detectors
- DS3 X-bit access
- DS3 transmit and receive AIS generation and detection
- DS3 M-frame and M-subframe boundary indications



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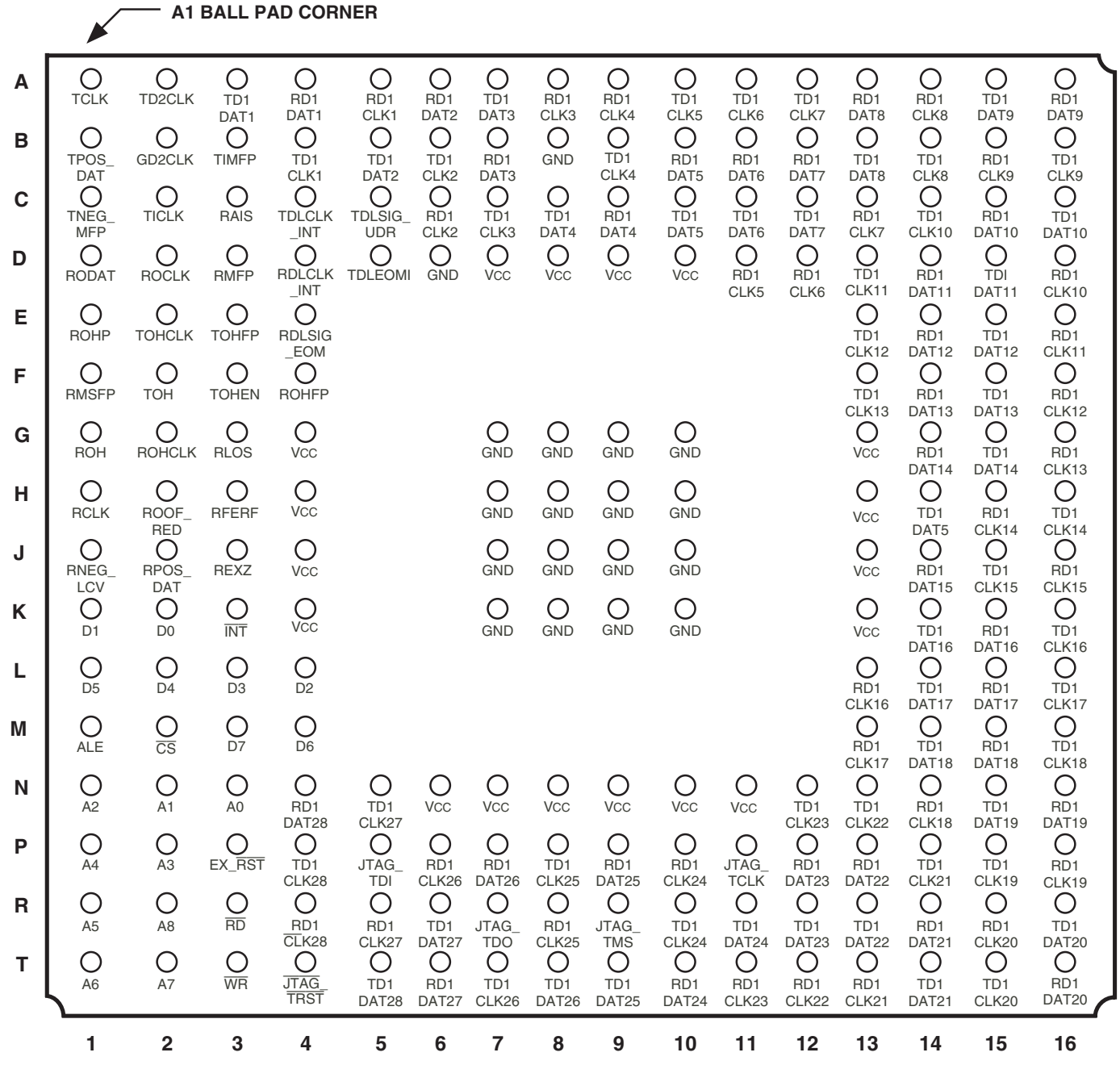
PACKAGE



6143 drw02

PBGA: 1mm pitch, 17mm x 17mm (BB208-1, order code: BB)

TOP VIEW

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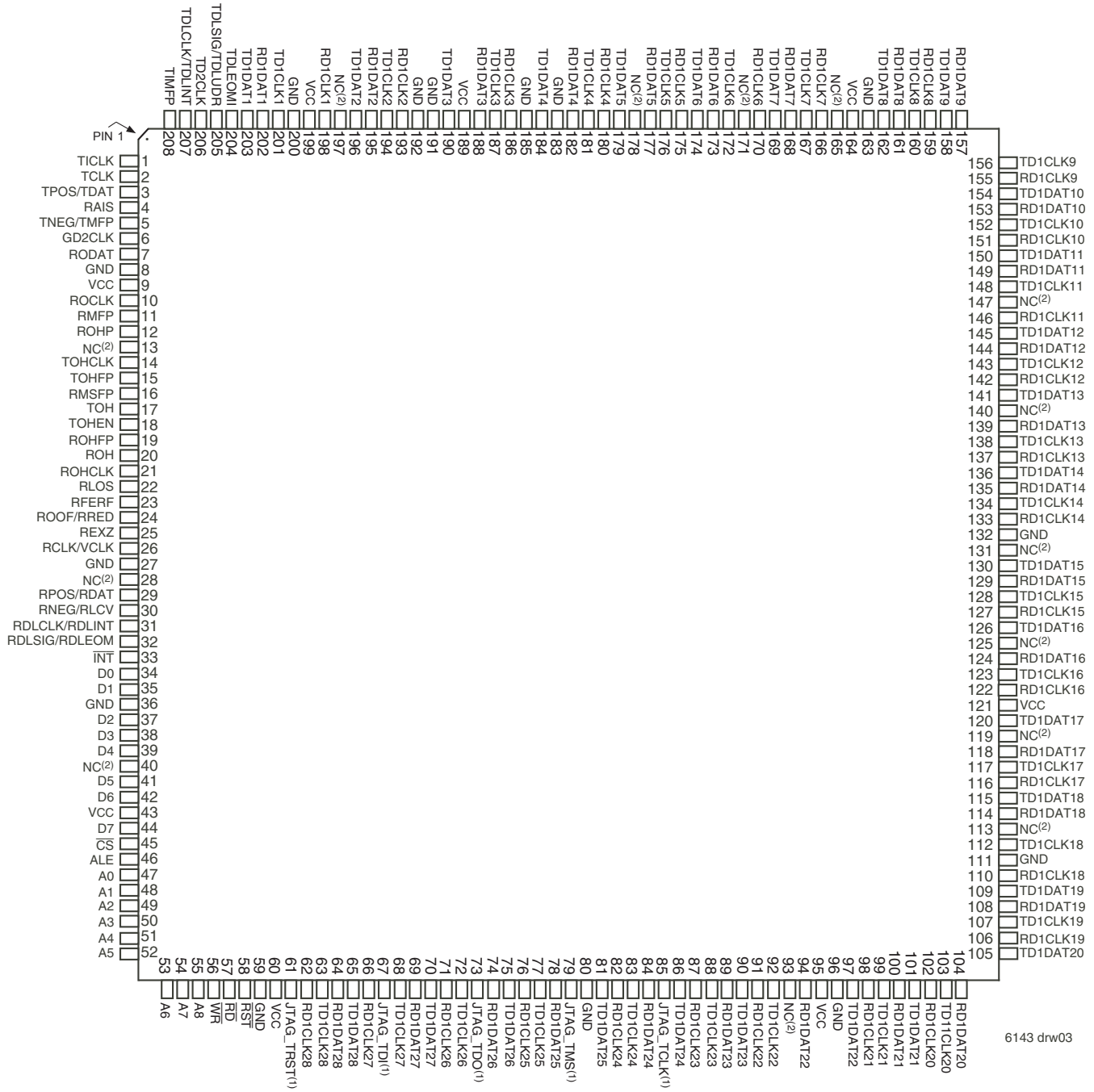

6143 drw03

NOTE:
1. JTAG
2. NC = No Connect

PQFP: 0.50mm pitch, 28mm x 28mm (DS208-1, order code: DS)

TOP VIEW

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PIN DESCRIPTIONS

TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
RCLK	Receive Clock	I	26	H1	This is the DS3 receive clock input. RCLK is nominally a 44.736 MHz, 50% duty cycle clock.
RPOS/RDAT	Receive Positive Pulse/Receive Data	I	29	J2	In dual rail mode, this pin is RPOS and represents the positive pulses of a B3ZS-encoded signal. In single rail mode, this pin is RDAT and represents the unipolar DS3 input data. The M13 can be configured to sample data on either the rising or falling edge of RCLK.
RNEG/RLCV	Receive Negative Pulse/ Receive Line Code Violation	I	30	J1	In dual rail mode, this pin is RNEG and represents the negative pulses of a B3ZS-encoded signal. In single rail mode, this pin is RLCV and can be used to insert line code violations on the DS3 input. The M13 can be configured to sample data on either the rising or falling edge of RCLK.
ROCLK	Receive Output Clock	O	10	D2	The DS3 receive output clock is a buffered version of the input RCLK. Like the RCLK, this is nominally a 44.736 MHz, 50% duty cycle clock. REXZ, RLOS, RMFP, RMSFP, and RODAT are updated on the falling edge of ROCLK.
RODAT	Receive Output Data	O	7	D1	This is a 44.736 Mb/s DS3 NRZ receive data stream decoded from the B3ZS line signal. RODAT is aligned to the frame alignment signals RMFP, RMSFP, and ROHP. RODAT is updated in the falling edge of ROCLK.
RMFP	Receive M-Frame Pulse	O	11	D3	The receive M-frame pulse signal and marks the first bit in the M-frame (X1) of the DS3 data on RODAT. In an OOF (Out Of Frame) condition the M13 internal counters will maintain the old M-frame alignment position. When the framer regains frame alignment the RMFP timing will be updated to the new timing. This may result in a change of frame alignment. RMFP is updated on the falling edge of ROCLK.
RMSFP	Receive M-subframe Frame Pulse	O	16	F1	The receive M-subframe pulse signal and marks the first bit of each M-subframe (X, P, and M) in each M-subframe of the DS3 on RODAT. In an OOF (Out Of Frame) condition the M13 internal counters will maintain the old M-frame alignment position. When the framer regains frame alignment the RMSFP timing will be updated to the new timing. This may result in a change of frame alignment. RMSFP is updated on the falling edge of ROCLK.
ROHP	Receive Overhead Pulse	O	12	E1	The receive overhead pulse signal and marks the overhead bit positions (X, P, M, C, and F) in the DS3 data on RODAT. In an OOF (Out Of Frame) condition the M13 internal counters will maintain the old frame alignment position. When the framer regains frame alignment, the ROHP timing will be updated to the new timing. This may result in a change of frame alignment. ROHP is updated in the falling edge of ROCLK.
ROHCLK	Receive Overhead Clock	O	21	G2	The receive overhead clock and transitions on each overhead bit. ROHCLK is nominally a 526 KHz. RAIS, RFERF, RFERR, RIDL, ROH, ROHFP, and ROOF are updated on the falling edge of ROHCLK.
ROH	Receive Overhead Data	O	20	G1	The receive overhead data signal transmits the overhead bits, C, F, M, P, and X bits from the receive DS3 stream. ROH is updated on the falling edge of ROHCLK.
ROHFP	Receive Overhead Frame Pulse	O	19	F4	The receive overhead frame pulse is used to mark the positions of the overhead bits within the overhead stream, ROH. ROHFP will remain high during the X1 overhead bit. ROHFP is updated on the falling edge of ROHCLK.
RLOS	Receive Loss of Signal	O	22	G3	The receive loss of signal will remain high when the dual rail NRZ format stream is selected or when a loss of signal condition is detected (175 successive zeros on RPOS and RNEG). When the one's density is greater than 33% for 175 +/i 1 bit period on the RPOS and RNEG inputs, RLOS will be set low. RLOS is updated on the falling edge of ROCLK.

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TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
REXZ	Receive Excessive Zeros	O	25	J3	The receive excessive zero indicates the detection of an excessive zero condition. When 3 or more successive zeros are received on the DS3 bipolar stream REXZ pulses high for one ROCLK cycle. In the uni-polar mode, REXZ is low. REXZ is updated on the falling edge of ROCLK.
RAIS	Receive Alarm Indication Signal	O	4	C3	The receive alarm indication signal is used to indicate and AIS (alarm indication) in the received DS3 signal. The RAIS will be set high when the AIS pattern has been detected for 2.23 ms or 13.5 ms as programmed by software. When the AIS pattern is absent in the DS3 signal for 2.23 ms or 13.5 ms the RAIS will be set low. RAIS is updated on the falling edge of ROHCLK.
ROOF/RRED	Receive Out of Frame/Receive Red Alarm	O	24	H2	ROOF/RREF will be ROOF when the REDO bit in the Master Alarm Enable register is 0 and will indicate an receive out-of-frame error. When no out-of-frame errors exist the ROOF will be low. ROOF will be high when there is an out-of-frame condition: 3 out of 16 (default) or 3 out of 8 consecutive F-bit errors are detected, or when more M-bit errors are detected in 3 out of 4 consecutive M-frames. ROOF is updated on the falling edge of ROHCLK. ROOF/RRED will be RRED when the REDO bit the Master Alarm Enable register is 1 and will indicate an out-of-frame condition or a DS3 loss of signal condition. A DS3 out-of-frame condition is considered when there are no transitions for 2.23 ms or 13.5 ms (software programmable) and RRED will be set high. RRED will be reset low when the out-of-frame condition or loss of signal condition are absent for 2.23 or 13.5 ms. RRED is updated on the falling edge of ROHCLK.
RFERF	Receive Far End Receive Failure	O	23	H3	The receive far end receive failure reflects the internal state of the internal FERF but the RFERF state is delayed by two M-frames. FERF is set high when both X1 and X2 are 0 in the M-frame. When X1 and X2 are both high in the M-frame, FERF is set low. Otherwise, FERF remains in its previous state when X1 • X2 in the current frame. The RFERF latency is used to provide better than 99.99% chance of freezing (holding FERF in its previous state) upon a valid state value during an out-of-frame. RFERF is updated every M-frame on the falling edge on ROHCLK.
RDLCLK/ RDLINT	Receive Data Link Clock/ Receive Data Link Interrupt	O	31	D4	RDLCLK/RDLINT will be RDLCLK when the REXHDLC bit in the Master HDLC Configuration Register is set to 1 and is used as the receive data link clock when an external HDLC receiver is selected. The RDLCLK is the clock for the external processing of the data link signal extracted by the DS3 framer. RDLCLK is nominally a 28.2 kHz clock that is low for at least 1.9us per cycle and is updated 3 times per M-frame. RDLCLK is updated on the falling edge of the ROHCLK. RDLCLK/RDLINT will be RDLINT when the REXHDLC bit in the Master HDLC Configuration Register is set to 0 and is used as the data link interrupt when an internal HDLC receiver is selected. When an HDLC receiver event occurs the RDLINT will reflect a change in status. By reading the Interrupt Enable/Status register, the interrupt will be cleared, both the register and the RDLINT pin. RDLINT is updated on the falling edge of ROHCLK. RDLINT is a configurable active low open-drain out or active high open-drain output. In the case where an external DMA device is used, RDLINT would be directly connected, however if the interrupt is being handled by a microprocessor, the RFDL may be wired-ORed with the $\overline{INT}$ output. In this later case, RDLINT should be configured as a active-low open drain output.

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TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
RDLSIG/ RDLEOM	Receive Data Link Signal/ Receive Data Link End Of Message	O	32	E4	RDLSIG/RDLEOM will be RDLSIG when the REXHDLC bit in the Master HDLC Configuration Register is set to 1 and is used as the receive data link signal when an external HDLC receiver is selected. The RDLSIG is the C-bit message used in C-bit parity mode and transmits the three C-bits from the fifth M-subframe in the DS3 frame. RDLSIG is updated on the falling edge of the RDLCLK. RDLSIG/RDLEOM will be RDLEOM when the REXHDLC bit in the Master HDLC Configuration Register is set to 0 and is used as the receive end of message signal when an internal HDLC receiver is selected. RDLEOM is used to denote the last byte of a sequence that is read from the HDLC receiver or to denote an overflow condition in the receive HDLC buffer. RDLEOM is updated on the falling edge of ROHCLK. In order to clear/deassert the RDLEOM the supervising microprocessor must read the Interrupt Enable/Status Register. In the case where RDLEOM would be connected to a supervising microprocessor, an external DMA is used. The RDLEOM would be programmed to be active-low, open-drain and wired-ORed with the $\overline{INT}$ to signal the microprocessor that the a complete message is ready.
RD1CLK1-28	Receive DS1 Clock	O	*See TQFP table below for details.	*See BGA table below for details,	RD1CLK1-28 are the receive DS1 clocks used in conjunction with the RD1DAT. These clocks are at the T1 nominal rate of 1.544MHz, but will have jitter due to the demultiplexing and destuffing processes. RD1DAT28-1 can be programmed to update on either the rising or falling edge of RD1CLK. For G.747, the internal M12 multiplexers still uses the RD1CLKs to clock RD1DAT out, however every fourth clock, RD1CLK4, 8, 12, 16, 20, 24, and 28 clocks, is unused and in turn output LOW. These clocks run at the nominal rate of 2.048MHz but will have jitter due to the demultiplexing and destuffing processes. If a DS2 is inserted into the M13, thereby bypassing the M12 multiplexer, every fourth clock RD1CLK4, 8, 12, 16, 20, 24, and 28 can be used as a DS2 clock. In this case the unused clocks for that group will output LOW. The DS2 clock has a nominal rate of 6.312MHz.
RD1DAT1-28	Receive DS1 Data	O	*See TQFP table below for details.	*See BGA table below for details	RD1DAT1-28 is the DS1 data demultiplexed from the incoming DS3 stream. RD1DAT1-28 are updated on either the rising or falling edge of the corresponding RD1CLK1-28. In G.747, where the M12 multiplexers mux E1 data, RD1DAT 4, 8, 12, 16, 20, 24, and 28 are held low, while the remaining streams operate at a nominal 2.048MHz data rate. M12 multiplexers are bypassed and DS2 data is output the fourth stream of the group is used to output data. The remaining three streams of the group will be held low.
TD1CLK1-28	Transmit DS1 Clock	I	*See TQFP table below for details.	*See BGA table below for deatils	The transmit DS1 clock, TD1CLK1-28 is used to sample incoming data on TD1DAT1-28 to be multiplexed into a DS3. The M13 expects a nominal 1.544MHz clocks and expects minimal jitter and wander of a standard DS1. TD1DAT1-28 are sampled on either the rising or falling edge of TD1CLK1-28. In G.747 multiplexing not all TD1 inputs are used. In this case, every fourth input (TD1CLK4, 8, 12, 16, 20, 24, and 28) is unused, ignored and must be tied to GND. The remaining clocks should be running at a nominal rate of 2.048MHz and expects minimal jitter and wander of a standard DS1. When the internal M12 multiplexers are bypassed, the M13 device will use every fourth clock (TD1CLK4, 8, 12, 16, 20, 24, and 28) as the DS2 input clock. In this case, the remaining clocks are unused, ignored and the unused inputs must be tied to GND.
TD1DAT1-28	Transmit DS1 Data	I	*See TQFP table below for details.	*See BGA table below fo details	The transmit DS1 data TD1DAT is the input data that is multiplexed in to a DS3. Input data can be programmed to sample on either the rising or falling edges of TD1CLK1-28. In G.747, where the M12 multiplexers mux E1 data, every fourth data stream (TD1DAT4, 8, 12, 16, 20, 24, and 28) is ignored and must be tied to GND. In cases where a DS2 is inserted directly into the M23 stage, every fourth TD1DAT (TD1DAT4, 8, 12, 16, 20, 24, and 28) can be used. In this case the remaining TD1DAT streams of the group are ignored and must be tied to GND.

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TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
GD2CLK	Generated DS2 Clock	O	6	B2	In M13 and C-bit parity modes, this is the transmit generated DS2 clock. In M13 operation this clock is nominally a 6.311993 MHz clock which translates to a 39.1% stuffing ratio. In C-bit parity mode this clock is nominally a 6.3062723 MHz clock, which translates to a stuffing rate of 100% (used for C-bit parity). The GD2CLK may be tied directly to the TD2CLK clock.
TD2CLK	Transmit DS2 Clock	I	206	A2	The TD2CLK is the transmit DS2 clock and is the clock used in the M12 multiplexer. TD2CLK is nominally a 6.312 MHz, 50% duty cycle clock and can be derived from the GD2CLK.
TDLSIG/ TDLUDR	Transmit Data Link Signal/ Transmit Data Underrun	O	205	C5	The TDLSIG/TDLUDR will be transmit data link, TDLSIG, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 1. When an external HDLC receiver is selected, TDLSIG will carry the the three C-bits in M-subframe #5 in the DS3. When C-bit parity mode is not enabled TDLSIG is ignored. TDLSIG is sampled on the rising edge of TDLCLK.The TDLSIG/TDLUDR will be the transmit data link underrun, TDLUDR, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 0. When an internal HDLC receiver is selected, TDLUDR is asserted when an internal HDLC transmitter underruns. TDLUDR can be cleared (deasserted) by writing to the XFDL Interrupt Status Register. TDLUDR is a programmable polarity, open-drain output. On reset, TDLSIG/TDLUDR is TDLSIG. The TEXHDLC register should be programmed after reset to the appropriate mode. When an external DMA is used, TDLUDR will be configured as an active-low output and wired-ORed with the $\overline{INT}$ output and routed to the supervising microprocessor. In that way, in the case of a transmit buffer underrun the supervising microprocessor will be notified.
TDLCLK/ TDLINT	Transmit Data Link Clock/ Transmit Data Link Interrupt	O	207	C4	The TDLCLK/TDLINT will be transmit data link clock, TDLCLK, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 1. When an external HDLC receiver is selected, TDLCLK will provide the timing for the external maintenance data link inserted by the DS3. TDLCLK is nominally a 28.2 KHz clock which is low for at least 1.9us per cycle. TDLCLK is updated on the falling edge of the TOHCLK and cycles three times per M-frame (one for each C-bit). The TDLCLK/TDLINT will be the transmit data link interrupt, TDLINT, when the TEXHDLC bit in the Master HDLC Configuration Register is a logic 0. When an internal HDLC receiver is selected, TDLINT is asserted when the last data byte is written to the internal HDLC transmitter. A write to the XFDL Configuration Register will end the current message transmission while a write to the XFDL Transmit Data Register will provide more data. TDLINT is a programmable polarity, open-drain output. On reset, TDLCLK/TDLINT is TDLINT. The TEXHDLC register should be programmed after reset to the appropriate mode. When an external DMA is used, TDLINT will be configured as an active-low output and wired-ORed with the $\overline{INT}$ output and routed to the supervising microprocessor. In that way, the supervising microprocessor will be notified and can service the XFDL.
TDLEMOI	Transmit Data Link End Of Message Input	I	204	D5	The transmit data link end of message input, TDLEMOI, is an alternate method for an external DMA controller to signal the end of the transmitted message to the HDLC transmitter. As the TDLEMOI is an alternative to writing the XFDL configuration register, appropriately the TDLEMOI will set the EOM bit in the XFD: Configuration register. The TDLEMOI input may be asserted before or after the write of the last byte, but must be asserted before the next byte (within 210 us of the last assertion of TDLINT or the $\overline{INT}$ bit in the XFDL Status Register). If no data transmission is pending, TDLEMOI is ignored.

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TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
TICLK	Transmit Input Clock	I	1	C2	The transmit input clock, TICLK, provides the timing for the DS3 input. TICLK is nominally a 44.736 MHz, 50% duty cycle clock. TIMFP is sampled on the rising edge of TICLK.
TIMFP	Transmit Input M-frame Frame Pulse	I	208	B3	The transmit M-frame pulse, TIMFP, provides the timing/alignment of the M-frame within the DS3 data, TDAT. The first bit (X1) of the M-frame on TDAT will occur within several TICLK cycle and will be confirmed by the output on TMFP. TIMFP may be pulled low if this kind of feedback is not required. TIMFP is sampled on the rising edge of TICLK.
TOH	Transmit Overhead Data	I	17	F2	The transmit overhead data, TOH, represents the overhead bits (C, F, M, P, and X) that may be inserted into the transmitted DS3. TOH is sampled on the rising edge of TOHCLK.
TOHEN	Transmit Overhead Enable	I	18	F3	The transmit overhead insertion, TOHEN, is the enable signal that is used in conjunction with the TOH, data input. When TOHEN is high the associated data on TOH will be inserted in to the DS3. When the TOHEN is low, the internal DS3 framer generates and inserts the DS3 overhead bits into the output DS3 stream. TOHEN is sampled on the rising edge of TOHCLK.
TOHFP	Transmit Overhead Frame Pulse	O	15	E3	The transmit overhead frame position, TOHFP, marks the beginning of the first M-frame, and aligns the TOH data to the DS3 M-frame. TOHFP will be high during the X1 overhead bit position. TOHFP is updated on the falling edge of TOHCLK.
TOHCLK	Transmit Overhead Clock	O	14	E2	The transmit overhead clock, TOHCLK, provides the timing transmit overhead bits. TOHCLK is nominally a 526 KHz clock. TOHFP is updated on the falling edge of TOHCLK. TOH and TOHEN are sampled on the rising edge of TOHCLK.
JCLK	Transmit DS3 Clock	O	2	A1	The transmit clock, TCLK, provides timing for other circuitry to synchronize with the DS3 transmitter. TCLK is nominally a 44.736 MHz, 50% duty cycle clock.
TPOS/TDAT	Transmit DS3 Positive Pulse/ Transmit DS3 Data	O	3	B1	In dual rail mode, TPOS/TDAT, is TPOS and represents the positive pulses of a B3ZS-encoded line. TPOS is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK. In single rail mode, TPOS/TDAT, is TDAT and represents the unipolar DS3 output data. Like the TPOS, TDAT is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK.
TNEG/TMFP	Transmit DS3 Negative Pulse/ Transmit Multi-frame Pulse	O	5	C1	In dual rail mode, TNEG/TMFP, is TNEG and represents the negative pulses of a B3ZS-encoded line. TNEG is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK. In single rail mode, TNEG/TMFP, is TMFP and represents the transmit multi-frame pulse. TMFP will be high during the first bit of the DS3 multiframe output on TDAT. TMFP is updated on the falling edge of TCLK by default but may be configured to update on the rising edge of TCLK.
$\overline{INT}$	Interrupt	O	33	K3	$\overline{INT}$ is the output interrupt pin. When an interrupt occurs in any of the TSBs, DS2 FRMR, DS3 FRMR, MX12, MX23, PMON, or RBOC, $\overline{INT}$ will go low, unless the interrupt is masked. In order to clear $\overline{INT}$, all pending interrupt TSBs must be read and cleared, otherwise $\overline{INT}$ will remain low. $\overline{INT}$ is an open drain output so it can be wired-ORed with other active-low open-drain output pins of the device.
$\overline{CS}$	Chip Select	I	45	M2	This active LOW input is used by a microprocessor to activate the microprocessor port. $\overline{CS}$ must go low for at least once after powerup. If $\overline{CS}$ is not used it must be tied to an inverted version of $\overline{RST}$.
$\overline{RD}$	Microprocessor Read	I	57	R3	This active low input controls the direction of the data bus lines (D0-7) during a microprocessor access. When $\overline{RD}$ is low, D0-7 are output.
$\overline{WR}$	Microprocessor Write	I	56	T3	This active low input controls the direction of the data bus lines (D0-7) during a microprocessor access. When $\overline{WR}$ is low, D0-7 are input.

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TABLE 1 — PIN DESCRIPTIONS

SYMBOL	NAME	I/O	TQFP PIN NO.	BGA Pin No.	DESCRIPTION
D0-7	Microprocessor Data	I/O	*See TQFP table below for details	*See BGA table below for deatils	These pins are the data bits of the microprocessor port.
A0-8	Microprocessor Address	I	*See TQFP table below for details	*See BGA table below for details	These address lines access all internal memories.
$\overline{RST}$	Reset	I	58	P3	This input puts the IDT82V8313 into a reset state that clears the device internal counters and registers. The RESET pin must be held LOW for a minimum of 100ns to properly reset the device. This pin has a weak internal pull-up resistor.
ALE	Address Latch Enable	I	46	M1	The address latch enable is an active high input that will latch the A0-7 address bus. The ALE is used in a multiplexed address/data microprocessor environment. The ALE has a weak internal pull-up resistor.
VCC	VCC	I	*See TQFP table below for details	*See BGA table below for details	This is the +3.3 Volt power supply for the core of the device.
VCC	VCC	I	*See TQFP table below for details	*See BGA table below for details	This is the +3.3 Volt power supply for the i/o of the device.
GND	Ground	I	*See TQFP table below for details	*See BGA table below for details	Ground Rail.
TDI	JTAG Test Serial Data In	I		P5	JTAG serial test instructions and data are shifted in on this pin. This pin is pulled HIGH by an internal pull-up when not driven.
TDO	JTAG Test Serial Data Out	O		R7	JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in high-impedance state when JTAG scan is not enabled.
TRST	JTAG Test Reset	I		T4	Asynchronously initializes the JTAG Test Access Port controller by putting it in the Test-Logic-Reset state. This pin is pulled HIGH by an internal pull-up when not driven. This pin should be pulsed LOW on power-up, or held LOW, to ensure that the IDT72V71660 is in the normal functional mode.
TCLK	JTAG Test Clock	I		P11	Provides the clock to the JTAG test logic.
TMS	JTAG Test Mode Select	I		R9	JTAG signal that controls the state transitions of the Test Access Port controller. This pin is pulled HIGH by an internal pull-up when not driven.

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TQFP PIN NUMBER TABLE

SYMBOL	NAME	I/O	PIN NUMBER
RD1CLK1-28	Receive DS1 Clock	O	198, 193, 186, 180, 175, 170, 166, 159, 155, 151, 146, 142, 137, 133, 127, 122, 116, 110, 106, 102, 98, 91, 87, 82, 76, 71, 66, 62.
RD1DAT1-28	Receive DS1 Data	O	202, 195, 188, 182, 177, 173, 168, 161, 157, 153, 149, 144, 139, 135, 129, 124, 118, 114, 108, 104, 100, 94, 89, 84, 78, 74, 69, 64.
TD1CLK1-28	Transmit DS1 Clock	I	201, 194, 187, 181, 176, 172, 167, 160, 156, 152, 148, 143, 138, 134, 128, 123, 117, 112, 107, 103, 99, 92, 88, 83, 77, 72, 68, 63.
TD1DAT1-28	Transmit DS1 Data	I	203. 196, 190, 184, 179, 174, 169, 162, 158, 154, 150, 145, 141, 136, 130, 126, 120, 115, 109, 105, 101, 97, 90, 86, 81, 75, 70, 65.
D0-7	Microprocessor Data	I/O	34, 35, 37, 38, 39, 41, 42, 44.
A0-8	Microprocessor Address	I	47, 48, 49, 50, 51, 52, 53, 54, 55.
Vcc	Vcc	I	9, 43, 60, 95, 121, 164, 189, 199.
GND	Ground	I	8, 11, 27, 36, 59, 80, 96, 111, 132, 163, 183, 185, 191, 192, 200.

BGA PIN NUMBER TABLE

SYMBOL	NAME	I/O	PIN DESCRIPTION
RD1CLK1-28	Receive DS1 Clock	O	A 5, C6, A8, A9, D11, D12, C13, A14, B15, D16, E16, F16, G16, H16, J16, L13, M13, N14, R16, R15, T13, T12, T11, P10, R8, P6, R5, R4.
RD1DAT1-28	Receive DS1 Data	O	A4, A6, B7, C9, B10, B11, B12, A13, A16, C15, D14, E14, J14, K15, L15, M15, N16, J15, R14, P13, T10, P9, P7, T6, N4.
TD1CLK1-28	Transmit DS1 Clock	I	B4, B6, C7, B9, A10, A11, A12, B14, B16, C14, D13, E13, F13, H16, J15, K16, L16, M16, P15, T15, P14, N13, N12, R10, P8, T7, N5, P4.
TD1DAT1-28	Transmit DS1 Transmit	I	A3, B5, A7, C8, C10, C11, C12, B13, A15, C16, D15, E15, F15, G15, H14, K14, L14, M14, N15, R16, T14, R13, R12, R11, T9, T8, R6, T5.
D0-7	Microprocessor Data	I/O	K2, K1, L4, L3, L2, L1, M4, M3.
A0-8	Microprocessor Address	I	N3, N2, P2, P1, R1,T1, T2, R2.
Vcc	Vcc	I	G4, H4, J4, K4, N6, N7, N8, N9, N10, N11, K13, J13, K13, G13, D6, D7, D8, D9, D10.
GND	Ground	I	B8, D6, G7-G10, H7-H10, J7-J10, K7-K10.

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REGISTER MEMORY MAP

TABLE 2 — REGISTER MEMORY MAP

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
00H	R/W	DS3RCACT	DS3TCACT	DS2TCACT	-	-	-	-	Reset	Master Reset/Clock Status
01H	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0	Revision/Global PMON Update
02H	R/W	EXD2CLK	BYP7	BYP6	BYP5	BYP4	BYP3	BYP2	BYP1	Master Bypass Configuration
03H	R/W	REXHDLC	TEXHDLC	-	-	REOMPOL	TUDRPOL	RINTPOL	TINTPOL	Master HDLC Configuration
04H	R/W	-		-	-	LINEAIS1	LINEAIS2	LLBE	DLBE	Master Loopback Configuration
05H	R/W	-	-	-	TINV	TFALL	TUNI	RINV	RFALL	Master Interface Configuration
06H	R/W	TNR	RNR	ALTFEBE	REDO	RED2ALME	DS2ALME	RED3ALME	DS3ALME	Master Alarm Enable/Network Requirement Bit
07H	R/W	-	-	-	-	DBCTRL	-	HIZDATA	HIZIO	Master Test
08H	R	REG2	REG3	XFDLINT	MX23	DS3FRMR	RFDLINT	RFDLEOM	RBOC	Master Interrupt Source #1
09H	R	XFDLUDR	DS2FRMR7	DS2FRMR6	DS2FRMR5	DS2FRMR4	DS2FRMR3	DS2FRMR2	DS2FRMR1	Master Interrupt Source #2
0AH	R	DS3PMON	MX12 7	MX12 6	MX12 5	MX12 4	MX12 3	MX12 2	MX12 1	Master Interrupt Source #3
0BH	-	-	-	-	-	-	-	-	-	Reserved
0CH	R/W	CBTRAN	AIS	IDL	FERF	SBOW	-	-	CBIT	DS3 TRAN Configuration
0DH	R/W	DLOS	DLCV	-	DFERR	DMERR	DCPERR	DPERR	DFEBE	DS3 TRAN Diagnostic
0EH - 11H	-	-	-	-	-	-	-	-	-	Reserved
11H	R/W	-	-	-	-	-	INTE	INTR	OVR	DS3 PMON Interrupt Enable/Status
12H - 13H	-	-	-	-	-	-	-	-		Reserved
14H	R	LCV7	LCV6	LCV5	LCV4	LCV3	LCV2	LCV1	LCV0	DS3 PMON LCV Count (LSB)
15H	R	LCV15	LCV14	LCV13	LCV12	LCV11	LCV10	LCV9	LCV8	DS3 PMON LCV Count (MSB)
16H	R	FERR7	FERR6	FERR5	FERR4	FERR3	FERR2	FERR1	FERR0	DS3 PMON FERR Count (LSB)
17H	R	-	-	-	-	-	-	FERR9	FERR8	DS3 PMON FERR Count (MSB)
18H	R	EXZS7	EXZS6	EXZS5	EXZS4	EXZS3	EXZS2	EXZS1	EXZS0	DS3 PMON EXZS Count (LSB)

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TABLE 2 — REGISTER MEMORY MAP

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
19H	R	EXZS15	EXZS14	EXZS13	EXZS12	EXZS11	EXZS10	EXZS9	EXZS8	DS3 PMON EXZS Count (MSB)
1AH	R	PERR7	PERR6	PERR5	PERR4	PERR3	PERR2	PERR1	PERR0	DS3 PMON PERR Count (LSB)
1BH	R	-	-	PERR13	PERR12	PERR11	PERR10	PERR9	PERR8	DS3 PMON PERR Count (MSB)
1CH	R	CPERR7	CPERR6	CPERR5	CPERR4	CPERR3	CPERR2	CPERR1	CPERR0	DS3 PMON CPERR Count (LSB)
1DH	R	-	-	CPERR13	CPERR12	CPERR11	CPERR10	CPERR9	CPERR8	DS3 PMON CPERR Count (MSB)
1EH	R	FEBE7	FEBE6	FEBE5	FEBE4	FEBE3	FEBE2	FEBE1	FEBE0	DS3 PMON FEBE Count (LSB)
1FH	R	-	-	FEBE13	FEBE12	FEBE11	FEBE10	FEBE9	FEBE8	DS3 PMON FEBE Count (MSB)
20H	R/W	-	-	-	EOM	INTE	ABT	CRC	EN	XFDL TSB Configuration
21H	R/W	-	-	-	-	-	-	INT	UDR	XFDL TSB Interrupt Status
22H	R/W	TD7	TD6	TD5	TD4	TD3	TD2	TD1	TD0	XFDL TSB Transmit Data
23H	--	-	-	-	-	-	-	-	-	Reserved
24H	R/W	-	-	-	-	-	-	TR	EN	RFDL TSB Configuration
25H	R/W	-	-	-	-	-	INTC1	INTC0	INT	RFDL Interrupt Control/Status
26H	R	FE	OVR	FLG	EOM	CRC	NVB2	NVB1	NVB0	RFDL TSB Status
27H	R	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	RFDL TSB Receive Data
28H	R/W	-	-	-	-	LBCOD1	LBCODE0	CBE	INTE	MX23 Configuration
29H	R/W	-	DAIS7	DAIS6	DAIS5	DAIS4	DAIS3	DAIS2	DAIS1	MX23 Demux AIS Insert
2AH	R/W	-	MAIS7	MAIS6	MAIS5	MAIS4	MAIS3	MAIS2	MAIS1	MX23 Mux AIS Insert
2BH	R/W	-	LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	MX23 Loopback Activate
2CH	R/W	0	ILBE7	ILBE6	ILBE5	ILBE4	ILBE3	ILBE23	ILBE1	MX23 Loopback Request Insert
2DH	R	-	LBRD7	LBRD6	LBRD5	LBRD4	LBRD3	LBRD2	LBRD1	MX23 Loopback Request Detect
2EH	R	-	LBRI7	LBRI6	LBRI5	LBRI4	LBRI3	LBRI2	LBRI1	MX23 Loopback Request Interrupt
2FH - 30H	-	-	-	-	-	-	-	-	-	Reserved
31H	R/W	-	-	BC5	BC4	BC3	BC2	BC1	BC0	FEAC XBOC Code

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TABLE 2 — REGISTER MEMORY MAP

Reg	R/W	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register Name
32H	R/W	-	-	-	-	-	IDLE	AVC	BOCE	FEAC RBOC Configuration/ Interrupt Enable
33H	R	IDLEI	BOCI	BOC5	BOC4	BOC3	BOC2	BOC1	BOC0	FEAC RBOC Interrupt Status
34H	R/W	AISPAT	FDET	MBDIS	M3O8	UNI	REFR	AISC	CBE	DS3 FRMR Configuration
35H ACE=0 ACE=1	R/W	COFAE -	REDE -	CBITE AISONES	FERFE BPVO	IDLE EXZSO	AISE EXTYPE	OOFE SALGO	LOSE ALGOTYPE	DS3 FRMR Interrupt Enable/Additional Configuration
36H	R	COFAI	REDI	CBITI	FERFI	IDLI	AISI	OOFI	LOSI	DS3 FRMR Interrupt Status
37H	R/W	ACE	REDV	CBITV	FERFV	IDLV	AISV	OOFV	LOSV	DS3 FRMR Status
38H - 3FH	-	-	-	-	-	-	-	-	-	Reserved
40H	R/W	G747	-	WORD	M2O5	MDBIS	REF	-	-	DS2 #1 FRMR PERR Configuration
41H	R/W	COFAE	-	REDE	FERFE	RESE	AISE	OOFE	-	DS2 #1 FRMR PERR Interrupt Enable
42H	R	COFAI	-	REDI	FERFI	RESI	AISI	OOFI	-	DS2 #1 FRMR PERR Interrupt Status
43H	R	-	-	REDV	FERFV	RESV	AISV	OOFV	-	DS2 #1 FRMR PERR Status
44H	R/W	-	-	-	-	-	INTE	INTR	OVR	DS2 #1 FRMR Monitor Interrupt Enable/Status
45H	R	FERR7	FERR6	FERR5	FERR4	FERR3	FERR2	FERR1	FERR0	DS2 #1 FRMR FERR Count
46H	R	PERR7	PERR6	PERR5	PERR4	PERR3	PERR2	PERR1	PERR0	DS2 #1 FRMR PERR Count (LSB)
47H	R	-	-	-	PERR12	PERR11	PERR10	PERR9	PERR8	DS2 #1 FRMR PERR Count (MSB)
48H	R/W	G747	PINV	MINV	FINV	ZAIS	XFERF	XRES	INTE	DS2 #1 MX12 Configuration and Control
49H	R/W	-	-	-	-	-	-	LBCODE1	LBCODE0	DS2 #1 MX12 Loopback Code Select
4AH	R/W	MAIS4	MAIS3	MAIS2	MAIS1	DAIS4	DAIS3	DAIS2	DAIS1	DS2 #1 MX12 AIS Insert
4BH	R/W	ILBR4	ILBR3	ILBR2	ILBR1	LBA4	LBA3	LBA2	LBA1	DS2 #1 MX12 Loopback Active
4CH	R	LBRI4	LBRI3	LBRI2	LBRI1	LBRD4	LBRD3	LBRD2	LBRD1	DS2 #1 MX12 Loopback Interrupt

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