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4-CHANNEL HD AUDIO CODEC OPTIMIZED FOR LOW POWER

92HD71B7

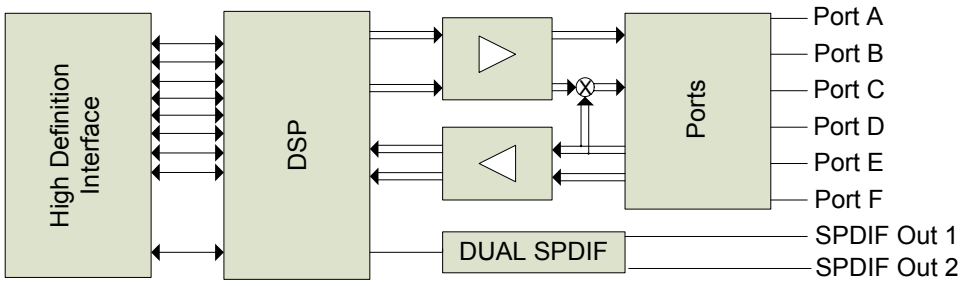
Description

The 92HD71B7 codec is a low power optimized, high fidelity, 4-channel audio codec compatible with Intel's High Definition (HD) Audio Interface. The 92HD71B7 codec provides stereo 24-bit resolution with sample rates up to 192kHz. Dual SPDIF provides connectivity to consumer electronic equipment that is WLP complaint. The 92HD71B7 provides high quality, HD Audio capability to notebook and business desktop PC applications.

Features

- **4 Channels (2 stereo DACs and 2 stereo ADCs) with 24-bit resolution**
  - Supports full-duplex stereo audio and simultaneous VoIP
  - Provides a mono output for laptop sub-woofer
- **Microsoft WLP 3/4 premium logo compliant, as defined in WLP 3.09**
- **Optimized and flexible power management with pop/click mitigation**
- **2 independent S/PDIF Output converters for WLP compliant HDMI/SPDIF support.**
- **Support for 1.5V and 3.3V HDA signaling with runtime selection**
- **Digital microphone input (mono, stereo, or quad array)**
- **3 Adjustable VREF Out pins for microphone bias**
- **High performance analog mixer option**
- **6 analog ports**
- **Supports to 3 stereo microphone inputs**
- **Two-pin volume up/down control**
- **Digital PC Beep to all outputs**
- **Integrated headphone amp**
- **Jack insertion detection**
- **Sample rates up to 192kHz**
- **+3.3 V, +4 V, +4.75 V and +5 V analog power supply options**
- **48-pin QFP and 48-pad QFN RoHS packages**

Block Diagram



Software Support

- Intuitive graphical user interface that allows configurability and preference settings
- SKPI (Kernel Processing Interface)
  - Enables plug-ins that can operate globally on all audio streams of the system
- 12 band fully parametric equalizer (SKPI plug-in)
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing (SKPI plug-in)
  - Enables improved voice articulation
  - Compressor/limiter allows higher average noise level without resonances
- IDT Vista APO wrapper
  - Enables multiple APOs to be used with the IDT Driver
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression
- Dynamic Stream Switching
  - Improved multi-streaming user experience with less support calls
- Dolby PC Entertainment Experience Logo Program
  - Dolby Home Theater™ (HT)
  - Dolby Sound Room™ (SR)
- Dolby Technologies
  - Dolby Headphone™, Dolby Virtual Speaker™
  - Dolby ProLogic II™, Dolby ProLogic IIx™
  - Dolby Digital Live™ (DDL)
- Maxx Player™ from Waves
- WOW™ and Tru Surround™ from SRS

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1. DESCRIPTION

1.1. Overview

The 92HD71B is a family of high fidelity, 4-channel audio codecs compatible with the Intel High Definition (HD) Audio Interface. The 92HD71B codecs provide high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

92HD71B variants:

PartNumber	*DAC SNR*	*# of Ports*	*Digital Mixer*	*Hi-Perf. Analog Mixer*
92HD71B8	103	6	Yes	Yes
92HD71B7	95	6	Yes	Yes
92HD71B5	95	4	Yes	No

The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to notebook and desktop PCs. 92HD71B7 is designed to meet or exceed premium logo requirements for Microsoft's Windows Logo Program (WLP) 3.09 and revision 4 as indicated in WLP 3.09.

The 92HD71B7 provides stereo 24- bit, full duplex resolution supporting sample rates up to 192kHz by the DAC and ADC. The 92HD71B7 SPDIF outputs support sample rates of 192kHz, 96kHz, 88.2kHz, 48kHz, and 44.1kHz. Additional sample rates are supported by the driver software.

The 92HD71B7 supports a wide range of mobile and desktop 4 channel configurations. The 2 independent SPDIF output interfaces provide connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. Simultaneous WLP compliant HDMI and SPDIF output is possible. All analog input pairs support LINE_IN and MIC.

MIC inputs can be programmed with 0/10/20/30dB boost. (40dB boost is available using the IDT driver.) For more advanced configurations, the 92HD71B7 has up to 8 General Purpose I/O (GPIO).

The port presence detect capabilities allow the codecs to detect when audio devices are connected to the codec. The fully parametric IDT SoftEQ can be initiated or disabled upon headphone jack removal and insertion for protection of notebook speakers.

The 92HD71B7 operates with a 3.3V digital supply and either 3.3V, 4V, 4.75V or 5V analog supply. It can also work with 1.5V and 3.3V HDA signaling; the correct signalling level is selected dynamically based on the power supply voltage on the DVDD-IO pin.

Available in a 48-pin QFP or QFN Environmental (ROHS) packages.

1.2. Orderable Part numbers

92HD71B7X5PRGXyyX	6port, 95dB, 5V, 48QFP
92HD71B7X5NLGXyyX	6port, 95dB, 5V, 48QFN
92HD71B7X3PRGXyyX	6port, 95dB, 3.3V, 48QFP
92HD71B7X3NLGXyyX	6port, 95dB, 3.3V, 48QFN

yy = silicon stepping/revision, contact sales for current data.
Add an “8” to the end for tape and reel delivery. Min/Mult order quantitiy 2ku.

1.3. Block Diagram

Figure 1. 92HD71B7 Block Diagram

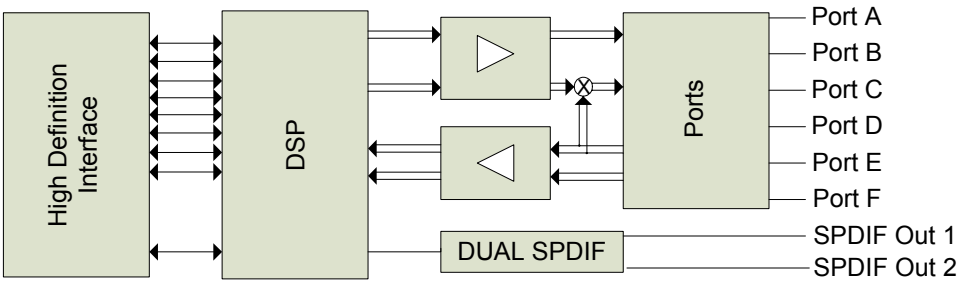
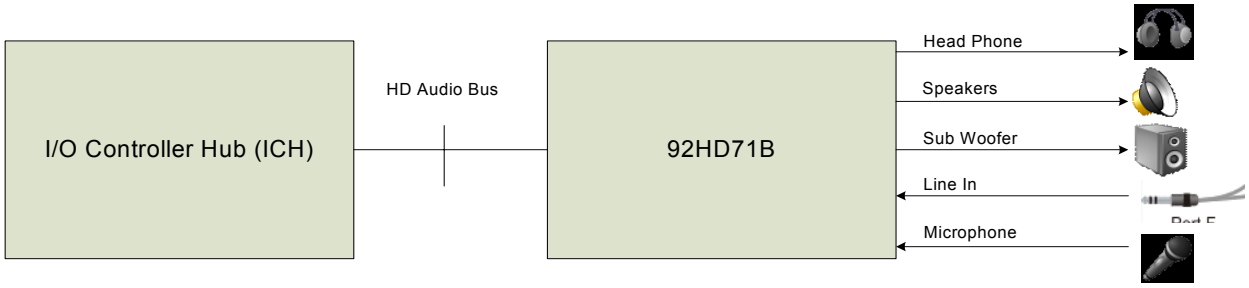


Figure 2. System Diagram



1.4. Detailed Description

1.4.1. Low-voltage High Definition Audio Link Signaling

The 92HD71B is compatible with either 1.5 V or 3.3 V High Definition Audio Link signaling; the voltage selection is performed dynamically based on the input voltage of DVDD_IO. Note that DVDD_IO is not a logic configuration pin but provides the digital power supply to be used for the High Definition Audio Link signals.

When in 1.5 V mode, the 92HD71B can correctly decode BITCLK, SYNC, RESET# and SDO because they operate at 1.5 V. Additionally, it will drive SDI_CODEC at 1.5 V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

1.4.2. Port Functionality

Single function (Input only / output only) ports allow for the highest possible performance.

- Port A supports
  - Headphone Out
  - Line Out
- Port D supports
  - Line Out
- Ports B and C support
  - Line In
  - Mic with 0/10/20/30/40 dB Mic boost[4]
- Mono Output cannot be reconfigured
- Port E supports
  - Line In
  - Mic with 0/10/20/30/40 dB Mic boost[4]
- Port F supports
  - Line Out

Note[4]: 40dB boost requires using the IDT driver. When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

1.4.3. Port Characteristics

Ports are designed to be dedicated inputs or outputs only. Universal (Bi-directional) jacks are not supported. Port A is designed to drive a set of 32 ohm (nominal) headphones or a 10K (nominal) load with on board shunt resistance as low as 20K ohms (typical - used to maintain coupling CAP bias.) Line Level outputs are intended to drive an external 10K speaker load (nominal) and an on board shunt resistor of 20-47K (nominal). However, applications may support load impedances of 5K ohms and above. Input ports are 47K impedance (nominal) at the pin.

DAC full scale outputs and intended full scale input levels are 1V rms. Line output ports and Head-on output ports on the 92HD71B7 may be configured for +3dBV full scale output levels by using a vendor specific verb.

Output ports are always on to prevent pops/clicks associated with charging and discharging output coupling capacitors. This maintains proper bias on output coupling caps even in D3 as long as AVDD is available. Unused ports should be left unconnected. When updating existing designs to use 92HD71B7, ensure that there are no conflicts between the output ports on 92HD71B7 and existing circuitry.

Table 1. Analog Output Port Behavior

AFG Power State	Output Enable	Mute	Port Behavior
D0-D2	1	0	Active - audio enabled
	1	1	Active - audio mute. Port drives silence
	0	-	Inactive -port is powered on (low output impedance) but drives silence only.
D3	-	-	Inactive (lower power) - Port keeps output coupling caps charged and has low output impedance (not necessarily the same as in D0) but consumes less power.

1.4.4. Jack Detect

Plugs inserted to a jack on Ports A, B, C, & D are detected using SENSE_A. Plugs inserted to a jack on Ports E & F are detected using SENSE_B. The following table summarizes the proper resistor tolerances for different analog supply voltages.

Table 2. Jack Detect

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Pull-Up	Resistor Tolerance SENSE_A (If port D is used)	Resistor Tolerance SENSE_A (If port D is not used)	Resistor Tolerance SENSE_B
5V	1%	1%	1%	1%
4.75V	1%	1%	1%	1%
4V	0.50%	0.50%	1%	1%
3.3V	0.10%	0.10%	1%	1%

See reference design for more information on Jack Detect implementation.

1.4.5. SPDIF Output

All SPDIF Outputs can operate at 44.1kHz, 48kHz, 88.2kHz, 96kHz and 192KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

A second independant SPDIF Output is provided as an option for WLP compliant HDMI and SPDIF outputs. Its function is identical to the primary SPDIF output.

Table 3. SPDIF OUT 0 (Pin 48) Behavior

AFG Power State	RESET#	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
	De-Asserted (High)	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down enabled)
	De-Asserted (High)	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down enabled)
	De-Asserted (High)	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut0 data (internal pull-down enabled)

Table 4. SPDIF OUT 1 (Pin 45) Behavior

AFG Power State	RESET#	GPIO7 Enable	Output Enable	Converter Dig Enable	Stream ID	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
	De-Asserted (High)	Enabled	-	-	-	Active - Pin reflects GPIO7 configuration (internal pull-up enabled)
	De-Asserted (High)	Disabled	Disabled	-	-	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Disabled	-	Active - Pin drives 0 (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	0	Active - Pin drives SPDIF-format, but data is zeroes (internal pull-down enabled)
	De-Asserted (High)	Disabled	Enabled	Enabled	1-15	Active - Pin drives SPDIFOut1 data (internal pull-down enabled)

1.4.6. Mono Output

The MONO Output is connected to pin 32 and has an independent mute (see the Widget listing for details). The MONO Output derives its input from the output of the summing node after the mono mux. The following sources are available for the mono pin:

DAC0 Output: When enabled (by using port connection list), both DAC0 Outputs are summed together.

DAC1 Output: When enabled (by using port connection list), both DAC1 Outputs are summed together.

Input Mixer: When enabled (by using mono mix connection list and DAC mixer), both mixer outputs are summed together.

The stereo inputs are scaled by -6dB and then summed to provide an output that is the average of the two inputs. The full scale output at mono out is designed to be about 0dBV. It is not possible to adjust to a +3dBV output level.

1.4.7. Analog Mixer

An analog mixer is available on the 92HD71B7. The mixer supports independent gain (-34.5 to +12dB in 1.5dB steps) on each input as well as independent mutes on each input.

The following inputs are available:

- DAC0
- DAC1
- Analog PC_Beep
- Inport0_Mux
- Inport1_Mux

1.4.8. Input Multiplexers

92HD71B7 implements 2 port input multiplexers. These multiplexers incorporate the microphone boost function (0, 10dB, 20dB, 30dB, and 40dB gain) as an output amp and allow a preselection of one of three possible inputs:

Port B

Port C

Port E

NOTE: Changing the Input multiplexer setting will affect both the analog mixer and the ADC.

1.4.9. ADC Multiplexers

92HD71B7 implements 2 ADC input multiplexers. These multiplexers incorporate the ADC record gain function (0 to +22.5dB gain in 1.5dB steps) as an output amp and allow a preselection of one of four possible inputs:

- DMIC 0
- DMIC1
- InPortMux (ADC0 selects inport0_mux / ADC1 selects inport1_mux)
- Mixer output

1.4.10. Power Management

The following table describes what functionality is active in each power state

The D3-default state is available for HD Audio compliance. The programmable values, exposed via vendor-specific settings, are under the IDT Device Driver control for further power reduction.

The default power state for the Audio Function Group after reset is D3-default..

Table 5. Power Managemen

D0	D1	D2[1]	D3	vendor specific	Function
On	Off	Off	Off	-	DAC
On	Off	Off	Off	-	D2S
On	Off	Off	Off	-	ADC
On	Off	Off	Off	-	ADC Volume Control
On	Off	Off	Off	-	Ref ADC
On	Off	Off	Off	-	Analog Clocks
On	On	Off	Off	-	VrefOut Pins
On	On	Off	Off	-	Input Boost
On	On	Off	Off	-	Analog mixer
On	On	Off	Off	-	Mixer Volumes
On	On	On	Low Drive[2]	Programmable	Lo Amp
On	On	On	Low Drive2	Programmable	HP Amps
On	On	On	Low Drive[3]	Programmable	VAG amp
On	On	On	On[4]	Programmable	Port Sense
On	On	On	On	Programmable[5]	Reference Bias generator
On	On	On	On	Programmable5	Reference Bandgap core
On	On	On	On[6]	-	AZ-Link

1.No DAC or ADC streams are active. Analog mixing and loop thru are supported.
2.VAG is kept active when ports are disabled or in D2/D3. Ports A, D, F and mono may be powered down using vendor specific verbs.
3.VAG is always ramped up and down gradually, except in the case of a sudden power removal. VAG is active in D2/D3 but in a low power state.
4. BITCLK must be active and both AVDD and DVDD must be available for Port Sense to operate.
5.Vendor specific bit for Ref Top controls VAG generator, Bandgap Reference, and Reference bias generator. Place part into D3 and power down all ports (using vendor specific verbs) before powering down Ref Top.
6.Obviously not active if BITCLK is not running (Controller in D3).

1.4.11. Multi-channel capture

The capability to assign multiple “ADC Converters” to the same stream is supported to meet the microphone array requirements of Vista and future operating systems. Single converter streams are still supported and is done by assigning unique non zero Stream IDs to each converter. All capture devices (ADCs 0 and 1) must be used to create a multi-channel input stream. There are no restrictions regarding digital microphones.

The ADC Converters can be associated with a single stream as long the sample rate and the bits per sample are the same. The assignment of converter to channel is done using the “CnvtrID” widget and is restricted to even values. The ADC converters will always put out a stereo sample and therefore require 2 channels per converter.

The stream will not be generated unless all entries for the targeted converters are set identically, and the total number of assigned converter channels matches the value in the NmbrChan field. These are listed the “Multi-Converter Stream Critical Entries.” table.

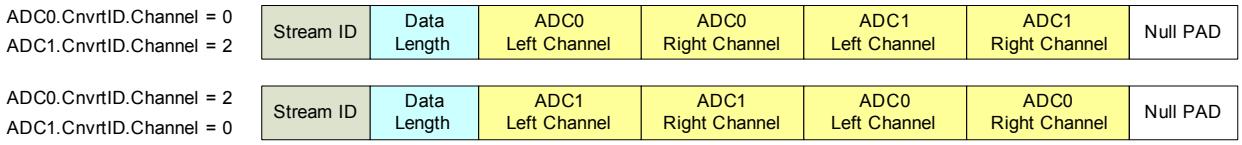
An example of a 4 Channel Steam with ADC0 supplying channels 0&1 and ADC1 supplying channels 2 & 3 is shown below. A 4 Channel stream can be created by assigning the same non-zero

stream id “Strm= N” to both ADC0 and ADC1. The sample rates must be set the same and the number of channels must be set to 4 channels “NmbrChan = 0011”.

Table 6: Example channel mapping

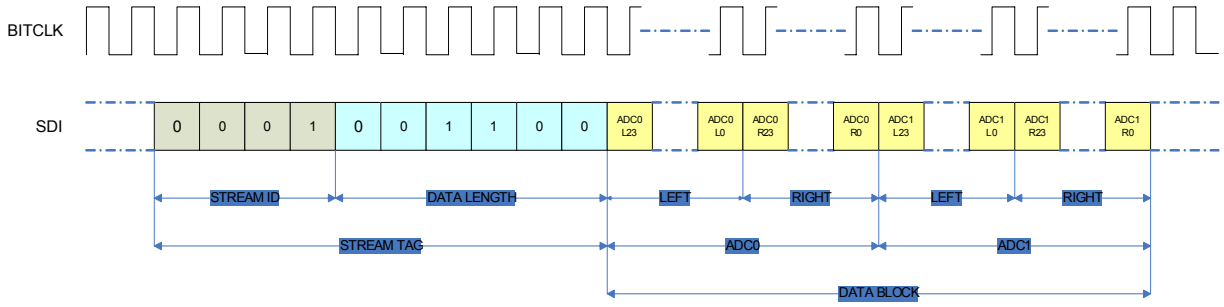
ADC1 CnvtrID	(NID = 0x08)	
	[3:0]	Ch = 2
ADC0 CnvtrID	(NID = 0x07)	
	[3:0]	Ch=0

Figure 3. Multi-channel capture



The following figure describes the bus waveform for a 24-bit, 48KHz capture stream with ID set to 1.

Figure 4. Multi-channel timing diagram



1.4.12. EAPD

The EAPD pin (pin 47) also supports SPDIF and GPIO functions. The pin defaults to EAPD after power on reset and will remain in EAPD mode until either GPIO is enabled for pin 47 or the port I/O is enabled to support SPDIF. The EAPD value is reflected on the EAPD pin; a 1 causes the external amplifier to power up, and a 0 causes it to power down. When the EAPD value = 1, the EAPD pin must be placed in a state appropriate to the current power state of the associated Pin Widget even though the EAPD value may remain 1. The default state of this pin is 0 (driving low) and a Pull-down prevents the line from floating high when the part is in reset.

Table 7. EAPD Behavior

AFG Power State	RESET#	GPIO Enable	Output Enable	EAPD Power State	Pin Behavior
D0-D3	Asserted (Low)	-	-	-	Hi-Z (internal pull-down enabled) immediately after power on, otherwise the previous state is retained until the rising edge of RESET#
	De-Asserted (High)	Enabled	-	-	Active - Pin reflects GPIO0 configuration (internal pull-up enabled)
	De-Asserted (High)	Disabled	Enabled	-	Active - Pin Drives SPDIFOut0/1 output (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D2-D3	Hi-Z (internal pull-down enabled)
	De-Asserted (High)	Disabled	Disabled	D0-D1	Active - Pin drives the value of the EAPD bit (internal pull-down enabled)

1.4.13. Digital Microphone Support

The digital microphone interface permits connection of a digital microphone(s) to the CODEC via the DMIC0, DMIC1, and DMIC_CLK 3-pin interface. The DMIC0 and DMIC1 signals are inputs that carry individual channels of digital Mic data to the ADC. In the event that a single microphone is used, the data is ported to both ADC channels.

The DMIC_CLK output is controllable from 4.704Mhz, 3.528Mhz, 2.352Mhz, 1.176Mhz and is synchronous to the 24Mhz internal clock. The default frequency is 2.352Mhz.

92HD71B7 supports the following digital microphone configurations:

Table 8. Valid Digital Mic Configurations

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones

Table 8. Valid Digital Mic Configurations

Digital Mics	Data Sample	ADC Conn.	Notes
1	Single Edge	0, or 1	Available on either DMIC_0 or DMIC_1 Both ADC Channels produce data, may be in phase or out by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 OR Single Edge on DMIC_0 and 1	0, or 1	Available on either DMIC_0 or DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0, or 1	Requires both DMIC_0 AND DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge	0, or 1	Connected to DMIC_0 and DMIC_1, External logic required to support sampling on a single Digital Mic pin channel on rising edge and second Digital Mic right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 9. DMIC_CLK and DMIC_0,1 Operation During Power States

Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D1	Yes	Clock Disabled	Input Disabled	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 Input Widget is Enabled. Otherwise, the DMIC_CLK remains Low
D2	Yes	Clock Disabled	Input Disabled	DMIC_CLK Remains Low
D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK Remains Low
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with Weak Pull-down

Figure 5. Single Digital Microphone (data is ported to both left and right channels

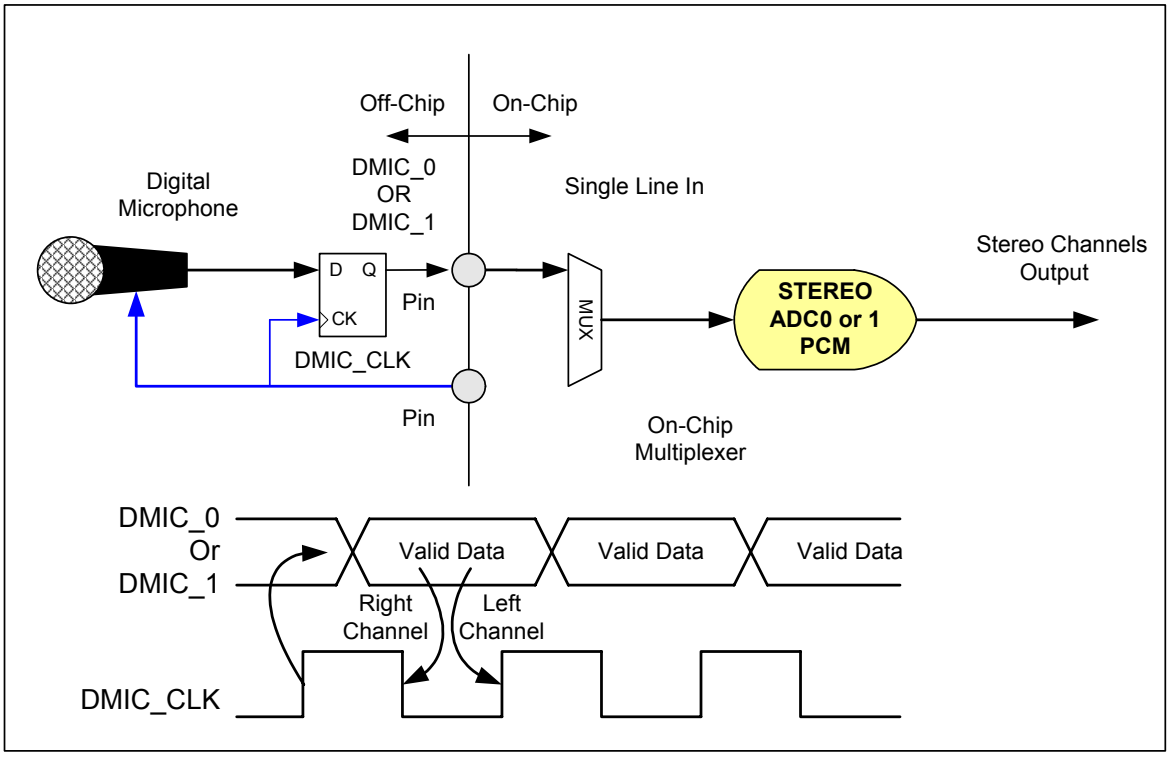
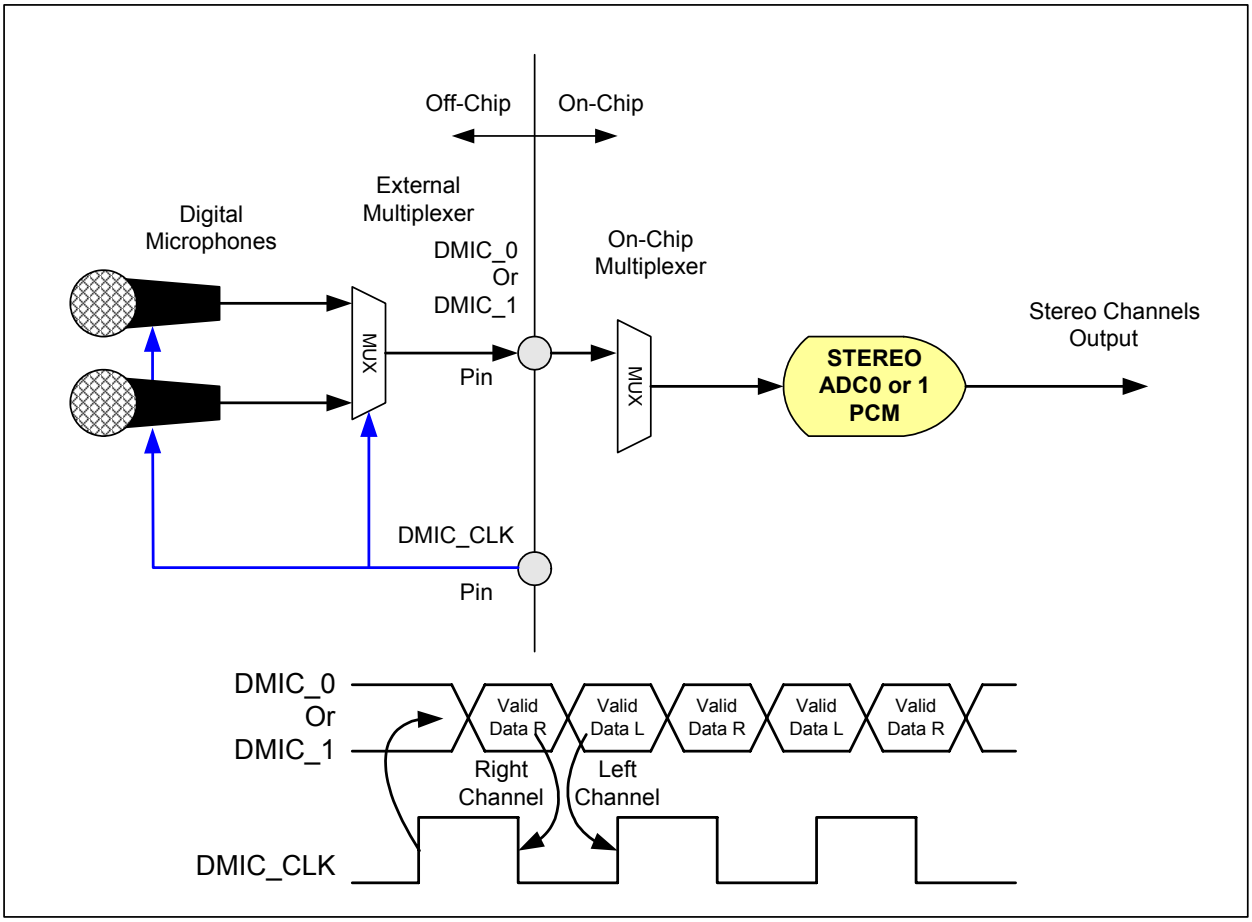
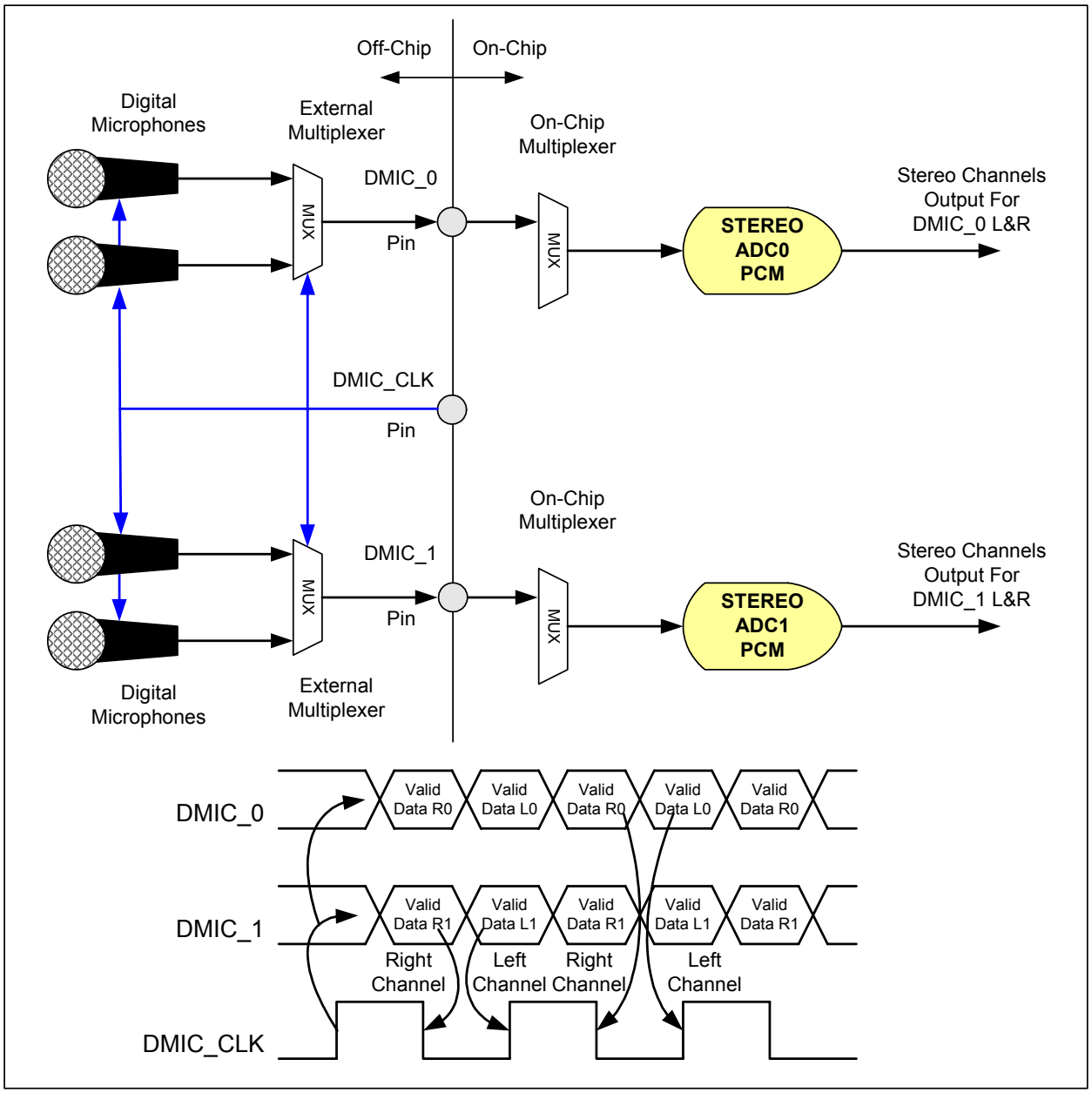


Figure 6. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

Figure 7. Quad Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore, the external mux may not be required.

1.4.14. Analog PC-Beep

92HD71B7 does not support automatic routing of the PC_Beep pin to all outputs when the link is in reset. Analog PC-Beep may be supported during Link Reset if the mixer is present and manually configured for pass-thru. Reset# must be high and Bit_Clk active. Analog PC_Beep is available as an input to the analog mixer.

1.4.15. Headphone Drivers

This product implements a +3dBV output option on headphone capable ports. (HP output and line output levels are defined as 1Vrms with an option to enable +3dBV FSOV using a vendor specific verb.)

1.4.16. GPIO

1.4.16.1. GPIO Pin mapping and shared functions.

Table 10. GPIO Pin mapping and shared functions

GPIO #	Pin	Supply	SPDIF In	SPDIF Out	GPI/O	GPI	GPO	VrefOut	ADAT	DMIC	VOL	Pull Up	Pull Down
1	2	DVDD			YES					YES	YES	50K (GPIO/VOL)	50K (DMIC)
2	4	DVDD			YES					YES	YES	50K (GPIO/VOL)	50K (DMIC)
3	30	AVDD			YES							50K[1]	
4	31	AVDD			YES			YES					
5	43	DVDD			YES							50K<superscript>1	
6	44	DVDD			YES							50K<superscript>1	
7	45	DVDD		YES	YES							50K (GPIO)	50K1 (SPDIF)
0	47	DVDD		YES	YES							50K (GPIO)	50K1 (SPDIF/EAPD)

1.Default condition.

1.4.16.2. Volume/Digital Microphone/GPIO Selection

To determine which function is actually enabled on pins2 and 4, the order of precedence is followed:

1) If the GPIOs are enabled, they override both Volume Control and Digital Mics

2) If the GPIOs are not enabled through the AFG, then at reset, the Volume control is enabled with the weak pull-up.

3) If BIOS or other software application enables either Digital Microphones inputs through the Configuration Default Register, the Volume is disconnected and the pull-ups are disconnected with the weak pull-downs enabled.

1.4.16.3. VRefOut/GPIO Selection

Two functions are available on pin 31. To determine which function is actually enabled, the order of precedence is followed:

1) If the GPIO4 function is enabled, it overrides VRefOut-E

2) If the GPIO4 function is not enabled through the AFG, then, at reset the VrefOut-E is enabled.

3) If using pin 31 as GPIO, make sure to incorporate a 10K ohm external pull-up to AVDD to prevent the pin from floating in GPI mode and to allow proper operation in open-drain GPO mode.

1.4.17. External Volume Control

92HD71B7 incorporates a 2-pin volume control interface. Volume up, down, and mute functions are easily implemented using 2 push-button switches. The CODEC provides internal pull-up resistors simplifying external CODEC circuitry. Also, repeat and direct modes of operation add flexibility to the interface. The typical usage model is for front panel master volume buttons on an entertainment PC, or case mounted hardware volume control for mobile platforms.

1.4.17.1. Theory of Operation

The codec monitors the volume up/down inputs for a change of state from high to low, and waits for the inputs to settle. If the inputs have not settled by the end of the de-bounce period, then the value at the end of the period is used. A 0 (low voltage) on the Down pin will decrement the volume register, while a 0 on the Up pin will increment the volume register. If both inputs are 0 at the same time, then the volume register will be set to its lowest value (mute). Pressing Up, Down, or both buttons at the same time when the volume control interface is in mute mode, will cause the part to un-mute.

The de-bounce / repeat rate is selectable from 2.5Hz to 20Hz in 2.5Hz increments using the Volume Knob VCSR0 verb (FE0) Rate bits (bits 2:0). This value is used for both de-bounce and repeat rates. The de-bounce period is the time that the CODEC waits for the inputs to settle, and the repeat rate is the rate at which the CODEC will increment/decrement the volume if a volume button is pushed and held. When a falling edge is detected on either one of the volume control pins, the codec will wait for (1/Rate) seconds for the input to settle. If the Continuous bit is set in the Volume Knob VCSR0 verb (bit 3), then the codec will wait for the de-bounce period to expire then repeatedly increment or decrement the volume register at the rate specified in the Rate bits until the button is released.

1.4.17.2. Modes of Operation

- DIRECT MODE
  - In Direct mode, the Volume Knob widget directly controls the volume of all of the DACs in the part. The volume in the Volume Knob widget acts as the master volume and limits the maximum volume for each of the DAC amplifiers. The amp gain for each of the DACs can also be adjusted using the DAC amplifiers. However, the actual gain for an individual DAC will be the sum of the Volume Knob volume and the DAC amplifier volume. For example, if the DAC amplifier gain is set to 0x7F (0dB) and the Volume Knob volume is set to 0x3F (-48dB) the resulting gain would be -48dB. If the combination of gains is less than -95.25dB

(the equivalent to a value of 0x0 for the DAC or Volume Knob volume settings) then the actual gain will be -95.25dB. For example, if the Volume Knob is set to 0x3F (-48dB) and the DAC amplifier volume is set to 0x1F (-72dB) then the DAC volume will be set to -95.25dB.

- Direct mode is enabled by setting bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

- INDIRECT MODE
  - In indirect mode, the Volume Knob widget does not directly control the DAC amplifier gains. An event on the volume Up/Down pins will increment/decrement the value in the Volume Knob Cntrl verb (F0F) volume bits (bits 6:0) just as in Direct mode. However, instead of adjusting the DAC amplifier gain, an unsolicited response is generated (if enabled) and the control software must read the volume in the Volume Knob widget and take appropriate action. Indirect mode is particularly useful when it is undesirable to control all of the DAC amplifier volumes at the same time, or when implementing ADC volume control.
  - In indirect mode, there are only 128 volume levels in the Volume Knob Cntrl volume bits, the value will not go beyond the lower and upper limits (0x0 or 0x7F), and an unsolicited response will not be generated if an input event tries to go beyond these limits. Therefore, it is the responsibility of the controlling software to monitor the volume in the Volume Knob Widget and take appropriate action.
  - Indirect mode is enabled by clearing bit 7 in the Volume Knob Cntrl verb (F0F). The volume is reflected in the Volume Knob Cntrl bits 6:0 and the step size is 0.75dB. In direct mode, software can read or write the volume in the Volume Knob widget.

1.4.17.3. Hardware Implementation

The Volume Knob interface is comprised of two input pins, CODEC pins 2 and 4. Both pins have internal pull-up resistors, so only two push button switches are required for most implementations. Typically, a series resistor and shunt capacitor are used to help reduce noise and prevent damage from ESD and other potential faults. An example circuit is shown below.

Figure 8. Volume Knob