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PROGRAMMABLE FLEXPC™ CLOCK FOR P4 PROCESSOR

IDTCV132B ADVANCE INFORMATION

FEATURES:

- **3 PLL architecture**
- **USB48 has 180° phase difference from DOT48 and VCH**
- **3V66 lead PCI 1.5ns to 3.5ns**
- **Band-gap circuit for differential output**
- **High power-noise rejection ratio**
- **100MHz to 200MHz CPU frequency**
- **VCO frequency up to 1.1G**
- **Support index block read/write**
- **All CPU-Stop and PCI-Stop related functions are removed**
- **Available in SSOP package**

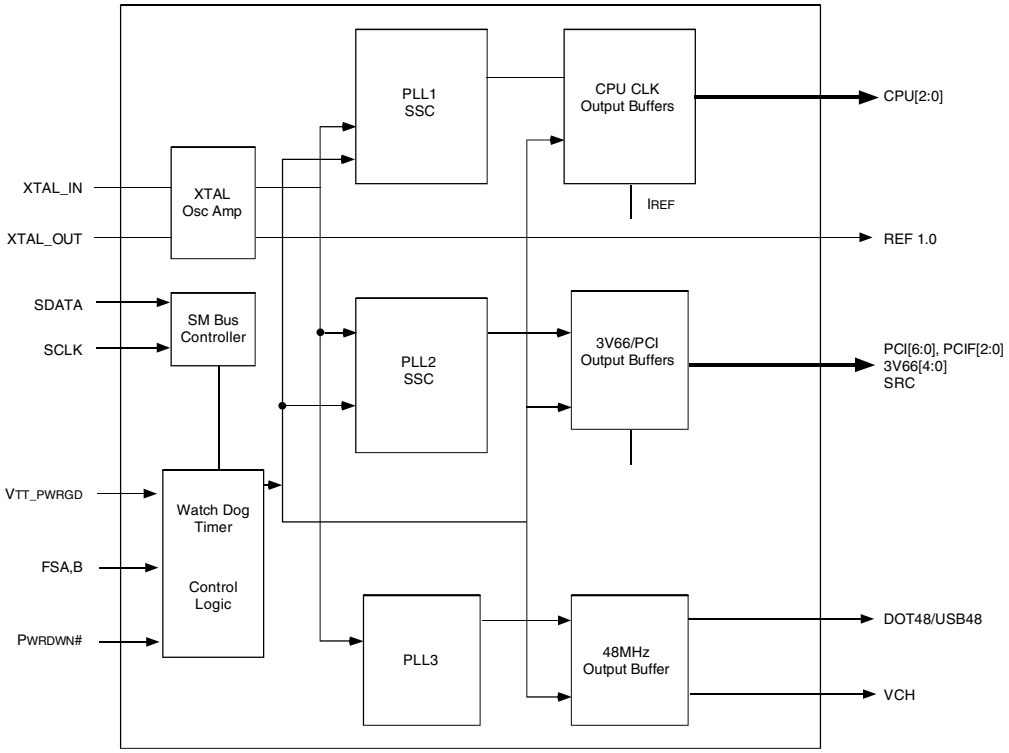
DESCRIPTION:

IDTCV132B is a 56 pin clock device for Intel springdale chip set and for Intel advance P4 processors. This device also implements Band-gap referenced I_{REF} to reduce the impact of V_{DD} variation on differential outputs, which can provide more robust system performance.

KEY SPECIFICATIONS:

- **CPU/SRC CLK cycle to cycle jitter < 125ps**
- **PCI CLK cycle to cycle jitter < 250ps**

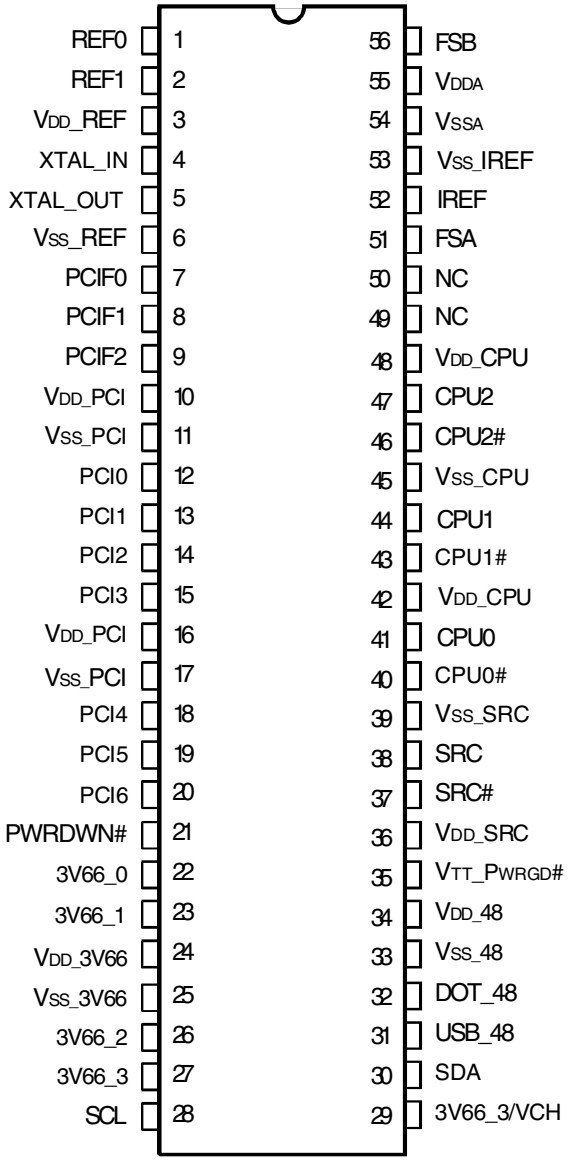
FUNCTIONAL BLOCK DIAGRAM



OUTPUT TABLE

CPU (Pair)	3V66	3V66/VCH	PCI	PCIF	REF	48MHz	SRC (Pair)
3	4	1	7	3	2	2	1

PIN CONFIGURATION



SSOP
TOP VIEW

HW FREQUENCY SELECTION

FSA	FSB	CPU	SRC	3V66	PCI/F	REF0	REF1	USB/DOT
0	0	100	100	66	33	14.318	14.318	48
0	MID	REF/N	REF/N	REF/N	REF/N	REF	REF	REF/N
0	1	200	100	66	33	14.318	14.318	48
1	0	133	100	66	33	14.318	14.318	48
1	1	166	100	66	33	14.318	14.318	48
1	MID	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z

PIN DESCRIPTION

Pin Number	Name	Type	Description
1	REF0	I/O	14.318 MHz reference clock output
2	REF1	I/O	14.318 MHz reference clock output
3	V_{DD}_REF	PWR	3.3V
4	XTAL_IN	IN	Xtal input
5	XTAL_OUT	OUT	Xtal output
6	V_{SS}_REF	GND	GND
7	PCIF0	OUT	PCI free running clock
8	PCIF1	OUT	PCI free running clock
9	PCIF2	OUT	PCI free running clock
10	V_{DD}_PCI	PWR	3.3V
11	V_{SS}_PCI	GND	GND
12	PCI0	OUT	GND
13	PCI1	OUT	PCI clock
14	PCI2	OUT	PCI clock
15	PCI3	OUT	PCI clock
16	V_{DD}_PCI	PWR	3.3V
17	V_{SS}_PCI	GND	GND
18	PCI4	OUT	PCI clock
19	PCI5	OUT	PCI clock
20	PCI6	OUT	PCI clock
21	PWRDWN#	IN	Power down, low active
22	3V66_0	OUT	66MHz
23	3V66_1	OUT	66MHz
24	V_{DD}_3V66	PWR	PWR
25	V_{SS}_3V66	GND	GND
26	3V66_2	OUT	66MHz
27	3V66_3	OUT	66MHz
28	SCL	IN	SMBus clock
29	3V66_4/VCH	GND	66MHz or 48MHz
30	SDA	I/O	SMBus data
31	USB48	OUT	48MHz
32	DOT48	OUT	48MHz
33	V_{SS}_48	GND	GND
34	V_{DD}_48	PWR	3.3V
35	V_{TT}_P_{WRGD}#	IN	Power on assertion to latch FSA, FSB signal. Active LOW.
36	V_{DD}_SRC	PWR	3.3V
37	SRC#	OUT	SATA 0.7V current mode differential clock output
38	SRC	OUT	SATA 0.7V current mode differential clock output
39	V_{SS}_SRC	GND	GND
40	CPU0#	OUT	Used for power on latch, active HIGH. After power on, becomes power down control, active LOW.
41	CPU0	OUT	Used for power on latch, active LOW
42	V_{DD}_CPU	PWR	3.3V
43	CPU1#	OUT	Host 0.7V current mode differential clock output
44	CPU1	OUT	Host 0.7V current mode differential clock output

PIN DESCRIPTION (CONT.)

Pin Number	Name	Type	Description
45	V_{SS}_CPU	GND	GND
46	CPU2#	OUT	Host 0.7V current mode differential clock output
47	CPU2	OUT	Host 0.7V current mode differential clock output
48	V_{DD}_CPU	PWR	3.3V
49	NC		No Connection
50	NC		No Connection
51	FSA	IN	CPU frequency select, latched at V_{TT}_P_{WRGD}# assertion
52	IREF	OUT	Differential reference current
53	V_{SS}_IREF	GND	Host 0.7V current mode differential clock output
54	V_{SSA}	GND	Analog V_{SS}
55	V_{DDA}	PWR	Analog V_{DD}
56	FSB	IN	GND

SM BUS PROTOCOL

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Acknowledge
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Acknowledge
20-27	8	Master	Byte count N (0 is not a valid byte count)
28	1	Slave	Acknowledge
29-36	8	Master	First data byte
37	1	Slave	Acknowledge
38-45	8	Master	Second data byte
46	1	Slave	Acknowledge
			:
			Nth data byte
			Stop

INDEX BLOCK READ PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	D2h
10	1	Slave	Acknowledge
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Acknowledge
20	1	Master	Repeated start
21-28	8	Master	D3h
29	1	Slave	Acknowledge
30-37	8	Slave	Byte count, N, SMBus table byte 8 value. Power on default is 0FH[15].
38	1	Master	Acknowledge
39-46	8	Slave	Offset data byte, specified by bit 11-18
47	1	Master	Acknowledge
48-55	8	Slave	Offset + 1 data byte
			:
		Slave	Offset + N-2
		Master	Acknowledge
		Slave	Offset + N-1
			Not acknowledge
			Stop

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Reserved				R	0
6	Reserved				R	0
5	Reserved				R	0
4	Reserved				R	0
3	Reserved				R	0
2	Reserved				R	0
1		FSB read back			R	
0		FSA read back			R	

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SRC	SRC free run control by Byte 3, bit 7	Free Run	Stoppable	RW	0
6	SRC	Output Enable	Tristate	Enable	RW	1
5	Reserved					1
4	Reserved					1
3	Reserved					1
2	CPU2	Output Enable	Tristate	Enable	RW	1
1	CPU1	Output Enable	Tristate	Enable	RW	1
0	CPU0	Output Enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	SRC_PWRDWN drive mode		Driven	Tristate	RW	0
6	SRC Stop mode		Driven	Tristate	RW	0
5	CPU2_PWRDWN drive mode		Driven	Tristate	RW	0
4	CPU1_PWRDWN drive mode		Driven	Tristate	RW	0
3	CPU0_PWRDWN drive mode		Driven	Tristate	RW	0
2	Reserved				RW	0
1	Reserved				RW	0
0	Reserved				RW	0

BYTE 3

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	PCI and SRC Stop	Stop PCI and SRC, doesn't include free run	Stop	Normal	RW	1
6	PCI6	Output Enable	Tristate	Enable	RW	1
5	PCI5	Output Enable	Tristate	Enable	RW	1
4	PCI4	Output Enable	Tristate	Enable	RW	1
3	PCI3	Output Enable	Tristate	Enable	RW	1
2	PCI2	Output Enable	Tristate	Enable	RW	1
1	PCI1	Output Enable	Tristate	Enable	RW	1
0	PCI0	Output Enable	Tristate	Enable	RW	1

BYTE 4

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	USB x2	Strength	2x	1x	RW	0
6	USB_48	Output Enable	Tristate	Enable	RW	1
5	PCIF2	Free run control	Free Run	controlled by Byte 3, bit 7	RW	0
4	PCIF1	Free run control	Free Run	controlled by Byte 3, bit 7	RW	0
3	PCIF0	Free run control	Free Run	controlled by Byte 3, bit 7	RW	0
2	PCIF2	Output Enable	Tristate	Enable	RW	1
1	PCIF1	Output Enable	Tristate	Enable	RW	1
0	PCIF0	Output Enable	Tristate	Enable	RW	1

BYTE 5

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	DOT_48	Output Enable	Tristate	Enable	RW	1
6	Reserved				RW	1
5	3V66_4/VCH	Mode Select	3V66	48MHz	RW	0
4	3V66_4/VCH	Output Enable	Tristate	Enable	RW	1
3	3V66_3	Output Enable	Tristate	Enable	RW	1
2	3V66_2	Output Enable	Tristate	Enable	RW	1
1	3V66_1	Output Enable	Tristate	Enable	RW	1
0	3V66_0	Output Enable	Tristate	Enable	RW	1

BYTE 6

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Reserved				RW	0
6	Reserved				RW	0
5	Reserved				RW	0
4	Reserved				RW	0
3	Reserved				RW	0
2	Spread Spectrum	Spread Spectrum Enable	Off	On	RW	0
1	REF1	Output Enable	Tristate	Enable	RW	1
0	REF0	Output Enable	Tristate	Enable	RW	1

BYTE 7

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	Vendor ID				R	0
6	Vendor ID				R	0
5	Vendor ID				R	0
4	Vendor ID				R	0
3	Vendor ID				R	0
2	Vendor ID				R	1
1	Vendor ID				R	0
0	Vendor ID				R	1

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	3.3V Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	3.3V Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–5	—	5	µA
I_{IL1}	Input LOW Current	V_{IN} = 0V, inputs with no pull-up resistors	–5	—	—	µA
I_{IL2}	Input LOW Current	V_{IN} = 0V, inputs with pull-up resistors	–200	—	—	µA
$I_{DD3.3OP}$	Operating Supply Current	Full active, C_L = full load	—	—	400	mA
$I_{DD3.3PD}$	Powerdown Current	All differential pairs driven	—	—	70	mA
		All differential pairs tri-stated	—	—	12	
F_I	Input Frequency(1)	V_{DD} = 3.3V	—	14.31818	—	MHz
L_{PIN}	Pin Inductance(2)		—	—	7	nH
C_{IN}	Input Capacitance(2)	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	
C_{INX}		X1 and X2 pins	—	—	5	
T_{STAB}	Clock Stabilization(2,3)	From V_{DD} power-up or de-assertion of PD# to first clock	—	—	1.8	ms
	Modulation Frequency(2)	Triangular modulation	30	—	33	KHz
	T_{DRIVE}_SRC(2)	SRC output enable after PCI_Stop# de-assertion	—	—	15	ns
	T_{DRIVE}_PD#(2)	CPU output enable after PD# de-assertion	—	—	300	us
	T_{FALL}_PD#(2)	Fall time of PD#	—	—	5	ns
	T_{RISE}_PD#(2)	Rise time of PD#	—	—	5	ns
	T_{DRIVE}_CPU_Stop#(2)	CPU output enable after CPU_Stop# de-assertion	—	—	10	us
	T_{FALL}_CPU_Stop#(2)	Fall time of PD#	—	—	5	ns
	T_{RISE}_CPU_Stop#(2)	Rise time of PD#	—	—	5	ns

NOTES:
1. Input frequency should be measured at the REF output pin and tuned to ideal 14.31818MHz to meet ppm frequency accuracy on PLL outputs.
2. This parameter is guaranteed by design, but not 100% production tested.
3. See TIMING DIAGRAMS for timing requirements.

ELECTRICAL CHARACTERISTICS - CPU AND SRC 0.7 CURRENT MODE DIFFERENTIAL PAIR(1)

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Z_O	Current Source Output Impedance(2)	$V_O = V_X$	3000	—	—	Ω
V_{OVS}	Maximum Voltage (Overshoot)		—	—	V_H + 0.3	V
V_{UDS}	Minimum Voltage (Undershoot)		-0.3	—	—	V
V_{HIGH}	Voltage HIGH(2)	Statistical measurement on single-ended signal using	660	—	1150	mV
V_{LOW}	Voltage LOW(2)	oscilloscope math function	–150	—	150	
V_{OVS}	Max Voltage(2)	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{UDS}	Min Voltage(2)		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)(2)		250	—	550	mV
d - V_{CROSS}	Crossing Voltage (var)(2)	Variation of crossing over all edges	—	—	140	mV
ppm	Long Accuracy(2,3)	See T_{PERIOD} Min. - Max. values	–300	—	300	ppm
T_{PERIOD}	Average Period(3)	400MHz nominal, no Intel spec	2.4993	—	2.5008	ns
		333.33MHz nominal, no Intel spec	2.9991	—	3.0009	
		266.66MHz nominal, no Intel spec	3.7489	—	3.7511	
		200MHz nominal	4.9985	—	5.0015	
		166.66MHz nominal	5.9982	—	6.0018	
		133.33MHz nominal	7.4978	—	7.5023	
		100MHz nominal	9.997	—	10.003	
T_{PERIOD}	Average Period(3)	400MHz spread, no Intel spec	2.4993	—	2.5008	ns
		333.33MHz spread, no Intel spec	2.9991	—	3.0009	
		266.66MHz spread, no Intel spec	3.7489	—	3.7511	
		200MHz spread	4.9985	—	5.0266	
		166.66MHz spread	5.9982	—	6.032	
		133.33MHz spread	7.4978	—	7.54	
		100MHz spread	9.997	—	10.0533	
t_R	Rise Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time(2)	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation(2)		—	—	125	ps
d-t_F	Fall Time Variation(2)		—	—	125	ps
d_{T3}	Duty Cycle(2)	Measurement from differential waveform	45	—	55	%
t_{SK3}	Skew, CPU[2:0](2)	V_T = 50%	—	—	100	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle, CPU[2:0](2)	Measurement from differential waveform	—	—	85	ps
	Jitter, Cycle to Cycle, SRC		—	—	125	

NOTES:
1. SRC clock outputs run only at 100MHz or 200MHz.
2. This parameter is guaranteed by design, but not 100% production tested.
3. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - 3V66

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	-300	—	300	ppm
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
T_{PERIOD}	Clock Period(2)	66MHz output nominal	14.9955	—	15.0045	ns
		66MHz output spread	14.9955	—	15.0799	
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising/Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V, 3V66	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS - PCICLK / PCICLK_F

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 30pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	33.33MHz output nominal	29.991	—	30.009	ns
		33.33MHz output spread	29.991	—	30.1598	
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-33	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-33	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	30	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	38	
	Edge Rate(1)	Rising edge rate	1	—	4	V/ns
	Edge Rate(1)	Falling edge rate	1	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.3	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
t_{SK1}	Skew(1)	V_T = 1.5V	—	—	500	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)	V_T = 1.5V	—	—	500	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, 48MHZ, USB AND V_{CH}

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8271	—	20.8396	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	1	—	2	V/ns
	Edge Rate(1)	Falling edge rate	1	—	2	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1.2	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

ELECTRICAL CHARACTERISTICS, DOT 48MHZ

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 10 - 20pF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
ppm	Long Accuracy(1,2)	See Tperiod Min. - Max. values	—	—	300	ppm
T_{PERIOD}	Clock Period(2)	48MHz output nominal	20.8271	—	20.8396	ns
V_{OH}	Output HIGH Voltage	I_{OH} = -1mA	2.4	—	—	V
V_{OL}	Output LOW Voltage	I_{OL} = 1mA	—	—	0.55	V
I_{OH}	Output HIGH Current	V_{OH} at Min. = 1V	-29	—	—	mA
		V_{OH} at Max. = 3.135V	—	—	-23	
I_{OL}	Output LOW Current	V_{OL} at Min. = 1.95V	29	—	—	mA
		V_{OL} at Max. = 0.4V	—	—	27	
	Edge Rate(1)	Rising edge rate	2	—	4	V/ns
	Edge Rate(1)	Falling edge rate	2	—	4	V/ns
t_{R1}	Rise Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1	ns
t_{F1}	Fall Time(1)	V_{OL} = 0.8V, V_{OH} = 2V	0.5	—	1	ns
d_{T1}	Duty Cycle(1)	V_T = 1.5V	45	—	55	%
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle(1)		—	—	350	ps

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. All long term accuracy and clock period specifications are guaranteed with the assumption that the REF output is at 14.31818MHz.

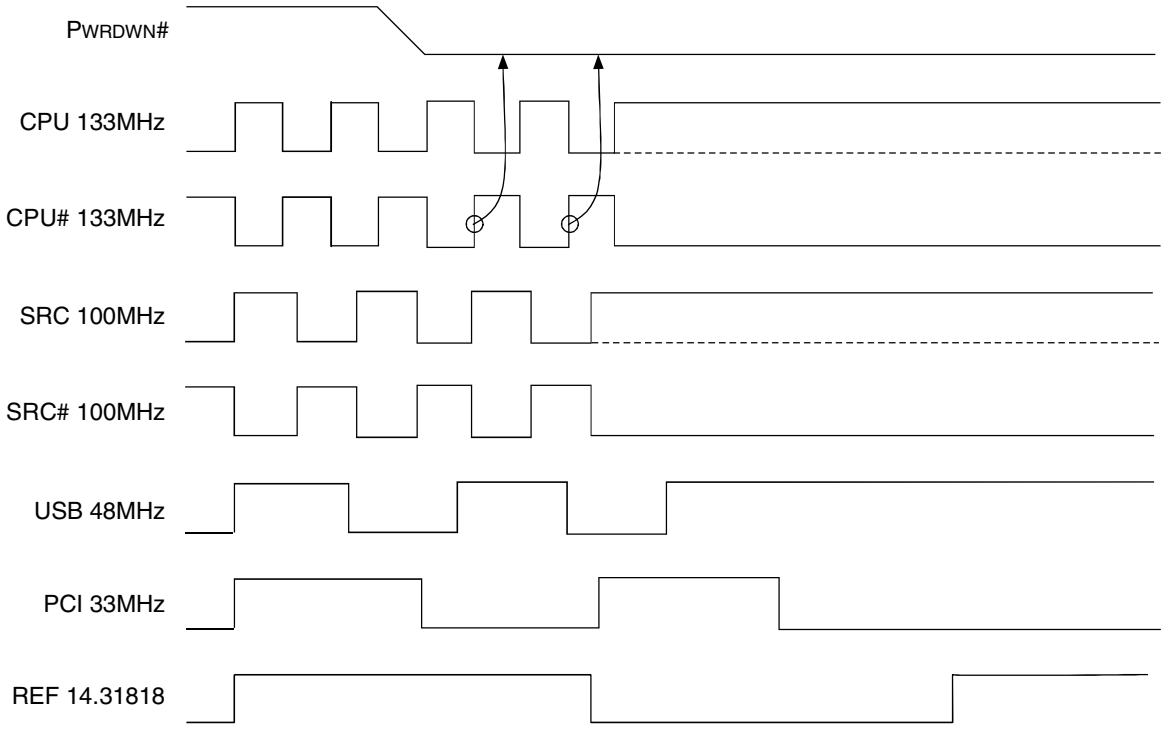
PD#, POWER DOWN

PD# is an asynchronous active low input used to shut off all clocks cleanly prior to clock power. When PD# is asserted low all clocks will be driven low before turning off the VCO. In PD# de-assertion all clocks will start without glitches.

PWRDWN#	CPU	CPU#	SRC	SRC#	PCIF/PCI	USB	3V66	REF
1	Normal	Normal	Normal	Normal	33MHz	48MHz	66MHz	14.318MHz
0	IREF * 2 or float	Float	IREF * 2 or float	Float	Low	High	Low	14.318MHz

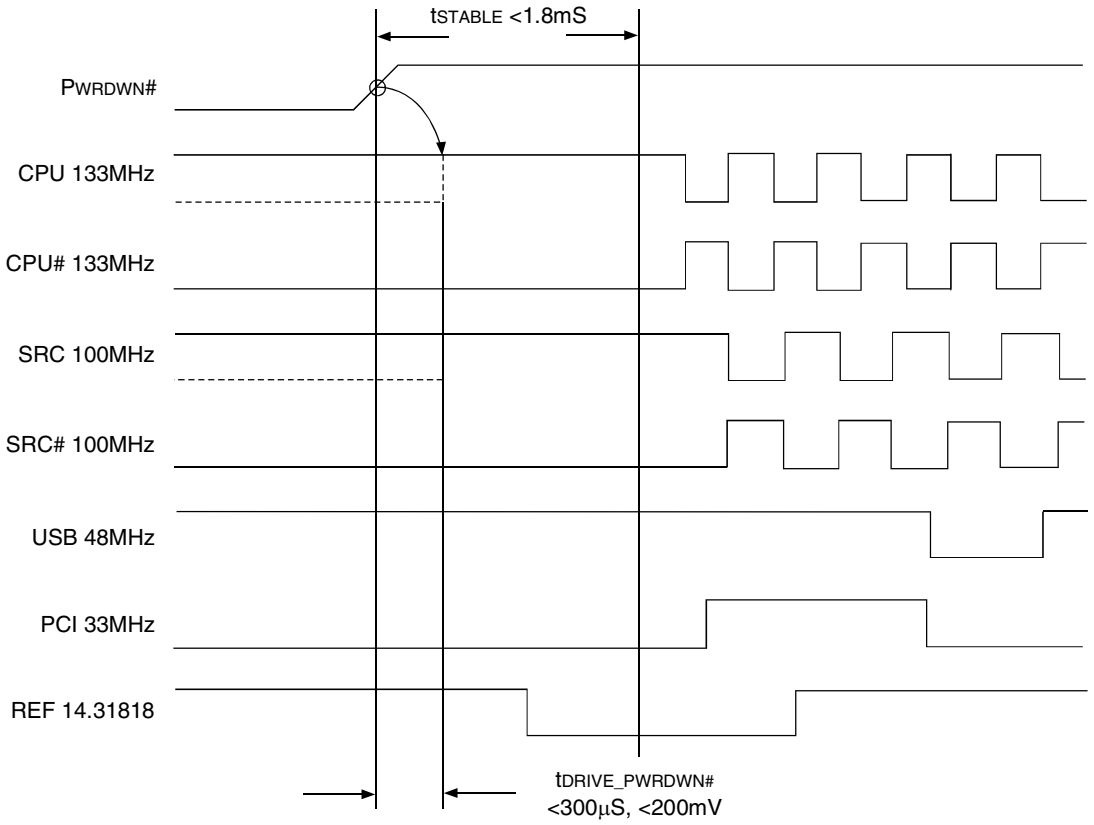
PD# ASSERTION

PD# should be sampled low by two consecutive CPU# rising edges before stopping clocks. All single-ended clocks will be held low on their next high to low transition. All differential clocks will be held high on the next high to low transition of the complimentary clock. If the control register determining to drive mode is set to 'tri-state', the differential pair will be stopped in tri-state mode, undriven. When the drive mode but corresponding to the CPU or SRC clock of interest is set to '0' the true clock will be driven high at 2 x IREF and the complementary clock will be tristated. If the control register is programmed to '1' both clocks will be tristated.

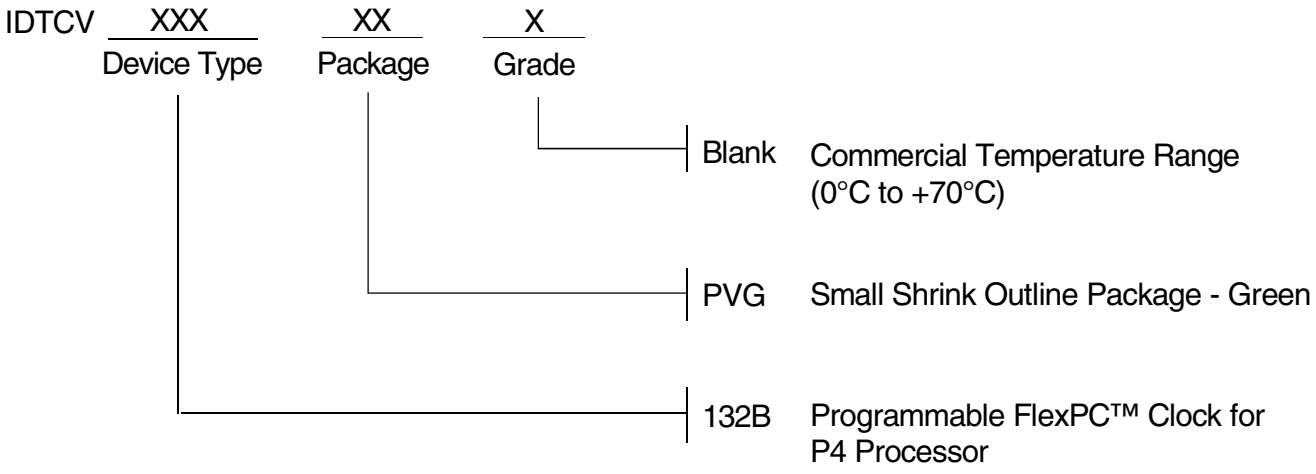


PD# DE-ASSERTION

The time from the de-assertion of PD# or until power supply ramps to get stable clocks will be less than 1.8ms. If the drive mode control bit for PD# tristate is programmed to '1' the stopped differential pair must first be driven high to a minimum of 200mV in less than 300µ s of PD# deassertion.



ORDERING INFORMATION



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