Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

1-TO-8 DIFFERENTIAL CLOCK BUFFER

IDTCV141

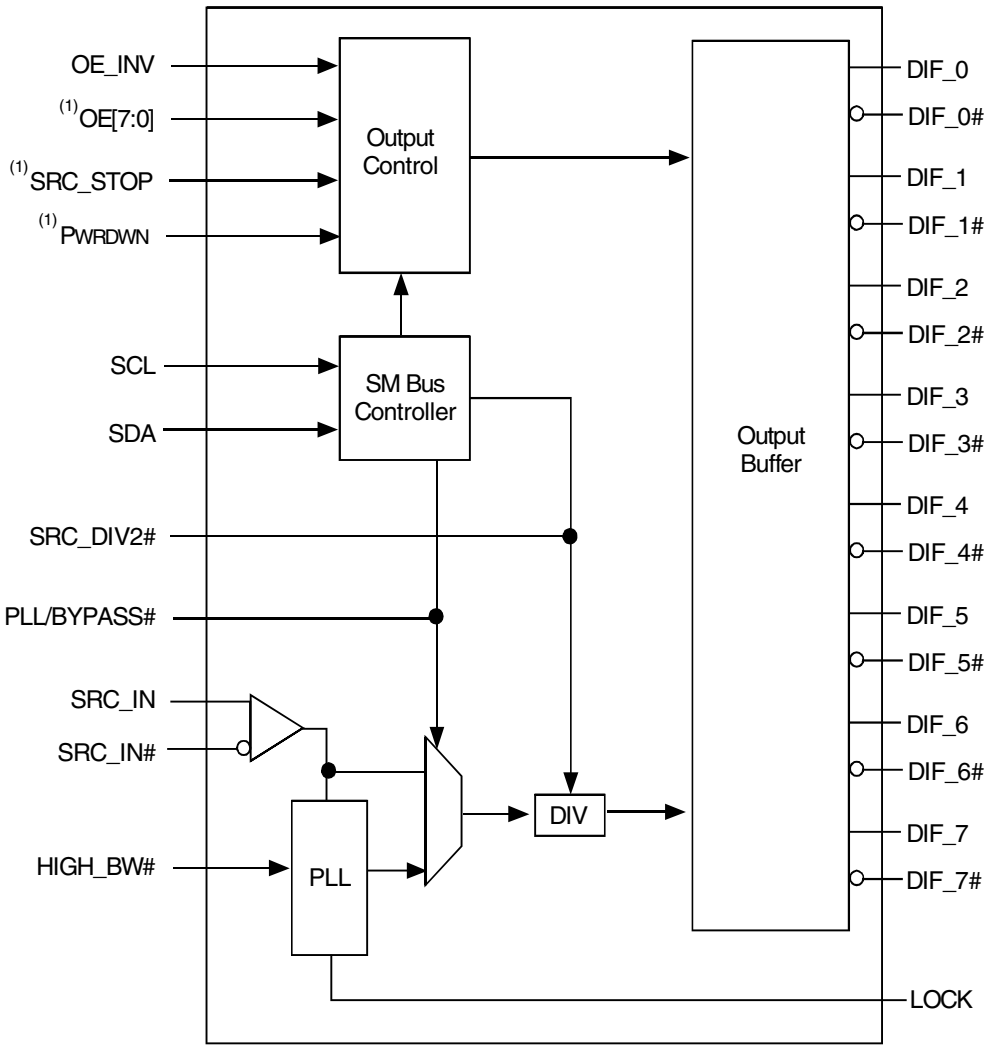
FEATURES:

- **Compliant with Intel DB800 spec**
- **Eight differential clock pairs at 0.7V**
- **50ps skew**
- **50ps cycle-to-cycle jitter**
- **Programmable Bandwidth**
- **PLL bypass configurable**
- **Divide by 2 programmable**
- **Available in SSOP and TSSOP packages**

DESCRIPTION:

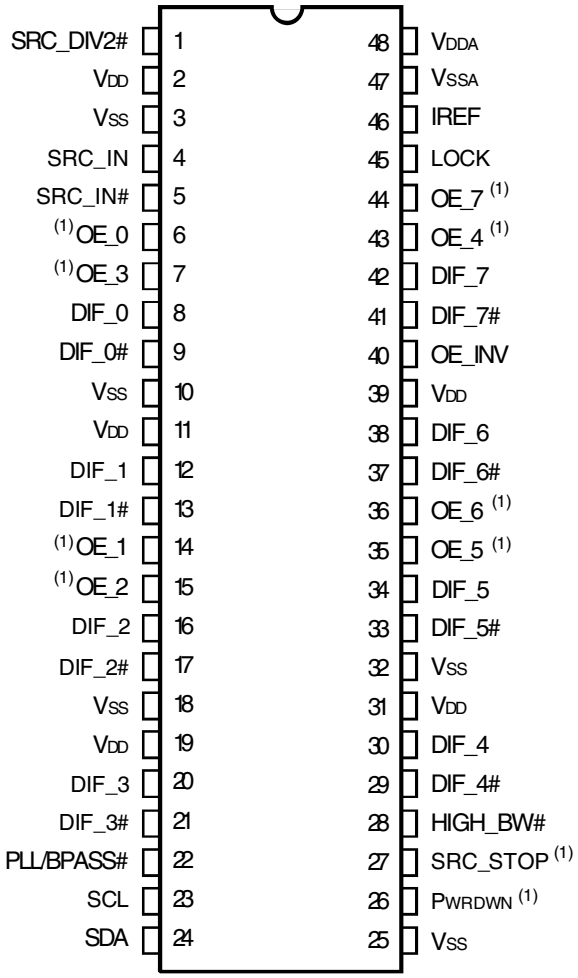
The CV141 differential buffer is compliant with Intel DB800 specifications. It is intended to distribute the SRC (serial reference clock) as a companion chip to the main clock of the CK409, CK410/CK410M, CK410B, etc. PLL is off in bypass mode and has no clock detect.

FUNCTIONAL BLOCK DIAGRAM



NOTE:
1. See OE_INV table for active HIGH or active LOW.

PIN CONFIGURATION



NOTE:
1. See OE_INV table for active HIGH or active LOW.

SSOP/ TSSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Min	Max	Unit
VDDA	3.3V Core Supply Voltage		4.6	V
VDDIN	3.3V Logic Input Supply Voltage	GND - 0.5	4.6	V
TSTG	Storage Temperature	–65	+150	° C
TAMBIENT	Ambient Operating Temperature	0	+70	° C
TCASE	Case Temperature		+115	° C
ESD Prot	Input ESD Protection Human Body Model	2000		V

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OE_INV

	OE_INV = 0	OE_INV = 1
OE_[7:0]	Active HIGH	Active LOW
PWRDWN	Active LOW	Active HIGH
SRC_STOP	Active LOW	Active HIGH

HIGH_BW# SELECTION

	HIGH_BW# = 0			HIGH_BW#=1			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
PLL BW	2	3	4	0.7	1	1.4	MHz
PLL Peaking	—	1	3	—	1	3	dB

OE FUNCTIONALITY [OE_INV = 0]

OE_[7:0] - Pin	OE_[7:0] - SMBus bit	DIF_[7:0]	DIFF_[7:0]#
1	1	Normal	Normal
1	0	Tristate	Tristate
0	1	Tristate	Tristate
0	0	Tristate	Tristate

OE FUNCTIONALITY [OE_INV = 1]

OE_[7:0] - Pin	OE_[7:0] - SMBus bit	DIF_[7:0]	DIFF_[7:0]#
1	1	Tristate	Tristate
1	0	Tristate	Tristate
0	1	Normal	Normal
0	0	Tristate	Tristate

PIN DESCRIPTION

Pin Name	Type	Pin #	Description
SRC_IN, SRC_IN#	IN, DIF	4,5	0.7V differential SRC input
DIF_[7:0], DIF_ [7:0]#	OUT, DIF	8, 9, 12, 13, 16, 17, 20, 21, 29, 30, 33, 34, 37, 38, 41, 42	0.7V differential clock output
OE[7:0]	IN	6, 7, 14, 15, 35, 36, 43, 44	3.3V LVTTL input for enabling differential outputs (see OE_INV table)
PWRDWN	IN	26	3.3V LVTTL for power down (see OE_INV table)
IREF	IN	46	Reference current for differential output
LOCK	OUT	45	HIGH, locked
PLL/Bypass#	IN	22	1 = PLL mode, 0 = bypass, PLL OFF
HIGH_BW#	IN	28	0 = HIGH BW, 1 = LOW BW (see HIGH_BW# Selection table)
SRC_DIV2#	IN	1	LOW = divide by 2 mode
SRC_STOP	IN	27	SRC stop (see OE_INV table)
SCL	IN	23	SMBus clock
SDA	I/O, Open Collector	24	SMBus data
OE_INV	IN	40	(see OE_INV table)

INDEX BLOCK WRITE PROTOCOL

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	DCh
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20-27	8	Master	Byte count, N (0 is not valid)
28	1	Slave	Ack (Acknowledge)
29-36	8	Master	first data byte (Offset data byte)
37	1	Slave	Ack (Acknowledge)
38-45	8	Master	2nd data byte
46	1	Slave	Ack (Acknowledge)
			:
		Master	Nth data byte
		Slave	Acknowledge
		Master	Stop

INDEX BLOCK READ PROTOCOL

Master can stop reading any time by issuing the stop bit without waiting until Nth byte (byte count bit30-37).

Bit	# of bits	From	Description
1	1	Master	Start
2-9	8	Master	DCh
10	1	Slave	Ack (Acknowledge)
11-18	8	Master	Register offset byte (starting byte)
19	1	Slave	Ack (Acknowledge)
20	1	Master	Repeated Start
21-28	8	Master	DDh
29	1	Slave	Ack (Acknowledge)
30-37	8	Slave	Byte count, N (block read back of N bytes), power on is 8
38	1	Master	Ack (Acknowledge)
39-46	8	Slave	first data byte (Offset data byte)
47	1	Master	Ack (Acknowledge)
48-55	8	Slave	2nd data byte
			Ack (Acknowledge)
			:
		Master	Ack (Acknowledge)
		Slave	Nth data byte
			Not acknowledge
		Master	Stop

INDEX BYTE WRITE

Setting bit[11:18] = starting address, bit[20:27] = 01h.

INDEX BYTE READ

Setting bit[11:18] = starting address. After reading back the first data byte, master issues Stop bit.

CONTROL REGISTERS

BYTE 0

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	PowerDown dirve mode		Driven	Tri-state	RW	0
6	SRC_STOP# drive mode		Driven	Tri-state	RW	0
5	Reserved				RW	0
4	Reserved				RW	0
3	Reserved				RW	0
2	High_BW#	Logically AND with HW pin	High band width	Low band width	RW	1
1	PLL/Bypass#	Logically AND with HW pin	Bypass	PLL mode	RW	1
0	SRC_DIV2#	Logically AND with HW pin	Divided by 2	Normal	RW	1

BYTE 1

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	DIFF_7	Output Enable	Tristate	Enable	RW	1
6	DIFF_6	Output Enable	Tristate	Enable	RW	1
5	DIFF_5	Output Enable	Tristate	Enable	RW	1
4	DIFF_4	Output Enable	Tristate	Enable	RW	1
3	DIFF_3	Output Enable	Tristate	Enable	RW	1
2	DIFF_2	Output Enable	Tristate	Enable	RW	1
1	DIFF_1	Output Enable	Tristate	Enable	RW	1
0	DIFF_0	Output Enable	Tristate	Enable	RW	1

BYTE 2

Bit	Output(s) Affected	Description/Function	0	1	Type	Power On
7	DIFF_7	Free Running with SRC_STOP#	Free	stopped	RW	0
6	DIFF_6	Free Running with SRC_STOP#	Free	stopped	RW	0
5	DIFF_5	Free Running with SRC_STOP#	Free	stopped	RW	0
4	DIFF_4	Free Running with SRC_STOP#	Free	stopped	RW	0
3	DIFF_3	Free Running with SRC_STOP#	Free	stopped	RW	0
2	DIFF_2	Free Running with SRC_STOP#	Free	stopped	RW	0
1	DIFF_1	Free Running with SRC_STOP#	Free	stopped	RW	0
0	DIFF_0	Free Running with SRC_STOP#	Free	stopped	RW	0

BYTE 3

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7	Reserved				RW	
6	Reserved				RW	
5	Reserved				RW	
4	Reserved				RW	
3	Reserved				RW	
2	Reserved				RW	
1	Reserved				RW	
0	Reserved				RW	

BYTE 4

Bit	Output(s) Affected	Description / Function	0	1	Type	Power On
7		Revision ID			R	0
6		Revision ID			R	0
5		Revision ID			R	0
4		Revision ID			R	0
3		Vendor ID			R	0
2		Vendor ID			R	1
1		Vendor ID			R	0
0		Vendor ID			R	1

BYTE 62 = 10h
BYTE 63 = 14h

ELECTRICAL CHARACTERISTICS - INPUT / SUPPLY / COMMON OUTPUT PARAMETERS

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{IH}	Input HIGH Voltage	3.3V ± 5%	2	—	V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage	3.3V ± 5%	V_{SS} - 0.3	—	0.8	V
I_{IH}	Input HIGH Current	V_{IN} = V_{DD}	–5	—	5	µA
I_{IL1}	Input LOW Current	V_{IN} = 0V, inputs with no pull-up resistors	–5	—	—	µA
I_{IL2}	Input LOW Current	V_{IN} = 0V, inputs with pull-up resistors	–200	—	—	µA
L_{PIN}	Pin Inductance[2]		—	—	7	nH
C_{IN}	Input Capacitance[2]	Logic inputs	—	—	5	pF
C_{OUT}		Output pin capacitance	—	—	6	

ELECTRICAL CHARACTERISTICS - DIF 0.7 CURRENT MODE DIFFERENTIAL PAIR

Following Conditions Apply Unless Otherwise Specified:
Operating Condition: T_A = 0°C to +70°C, Supply Voltage: V_{DD} = 3.3V ± 5%; C_L = 2pF

Symbol	Parameter[1]	Test Conditions	Min.	Typ.	Max.	Unit
V_{HIGH}	Voltage HIGH		+150	—	—	mV
V_{LOW}	Voltage LOW		—	—	–150	
V_{MAX}	Max Input Voltage	Measurement on single-ended signal using absolute value	—	—	1150	mV
V_{MIN}	Min Input Voltage		–300	—	—	
$V_{CROSS(ABS)}$	Crossing Voltage (abs)		250	—	550	mV
t_R	Rise Time	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
t_F	Fall Time	V_{OL} = 0.175V, V_{OH} = 0.525V	175	—	700	ps
d-t_R	Rise Time Variation		—	—	125	ps
d-t_F	Fall Time Variation		—	—	125	ps
d_{T3}	Duty Cycle	Measurement from differential waveform	45	—	55	%
t_{SK3}	Output Pin-to-Pin Skew	V_T = 50%	—	—	50	ps
$t_{JCYC-CYC}$	Jitter, Cycle to Cycle[2]	Measurement from differential waveform	—	—	50	ps

NOTES:
1. Parameter is guaranteed by design, but not 100% production tested.
2. Bypass mode, additive.

SRC_IN 0.7V AC TIMING CHARACTERISTICS

Symbol	Parameter[1]	Min.	Max.	Unit
Rising Edge Rate	Rising Edge Rate	0.6	4	V/ns
Falling Edge Rate	Falling Edge Rate	0.6	4	V/ns
V_{IH}	Differential Input HIGH Voltage	+150	—	mV
V_{IL}	Differential Input LOW Voltage	—	–150	mV
V_{CROSS}	Absolute Crossing Point Voltages	250	550	mV
V_{MAX}	Absolute Maximum Input Voltage	—	+1.15	V
V_{MIN}	Absolute Minimum Input Voltage	–0.3	—	V
Duty Cycle	SRC_IN Duty Cycle	45	55	%

DIF AC TIMING CHARACTERISTICS

PLL Bandwidth and Peaking

Symbol	Parameter	Min	Typ	Max	Units
$T_{PROP,PLL}$	SRC_IN to DIF Propagation Delay, PLL Mode(1)	-250	—	250	ps
$T_{PROP, BYPASS}$	SRC_IN to DIF Propagation Delay, Bypass Mode(1)	2.5	—	4.5	ns
T_{SKEW}	DIF_[7:0] Pin to Pin Skew(1)	—	—	250	ps
PLL bandwidth	HIGH_BW#=0 (high bandwidth)(1)	2	3	4	MHz
PLL bandwidth	HIGH_BW#=1 (low bandwidth)(1)	0.7	1	1.4	MHz
PLL Peaking	PLL Peaking(1,2)	—	1	3	dB
$T_{CCJITTER}$	Cycle to Cycle Jitter(1)	—	—	50	pS
Duty cycle	PLL Mode(1)	45	—	55	%
Duty cycle	Bypass (assume input is 50%)(1)	40	—	60	%

NOTES:
1. This parameter is guaranteed by design, but not 100% production tested.
2. Measured at 3dB downpoint.

OUTPUT CONTROL

Symbol	Parameter	Min	Typ	Max	Units
T_{DRIVE_PWRDWN}	CLK driven from PD De_Assertion	—	—	300	µs
T_{ACTIVE_PWRDWN}	CLK Toggling from PD De_Assertion	—	—	1	ms
T_{ACTIVE_OE}	CLK toggling from OE_[7:0] Assertion	2	—	6	Clock Periods
$T_{INACTIVE\_OE}$	CLK Tri-stated from OE_[7:0] De_Assertion	2	—	6	Clock Periods

PWRDWN (OE_INV = 0)

The P_{WRDWN} signal is a de-bounced signal in that its state must remain unchanged during two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

P_{WRDWN}	DIF	DIF#
1	Normal	Normal
0	Iref*2 or Float	Float

SRC_STOP (OE_INV = 0)

The SRC_STOP signal is a de-bounced signal in that its state must remain unchanged during two consecutive rising edges of DIF# to be recognized as a valid assertion or de-assertion.

SRC_STOP	DIF	DIF#
1	Normal	Normal
0	Iref*6 or Float	Float

PWRDWN (OE_INV = 1)

P_{WRDWN}	DIF	DIF#
1	Iref*2 or Float	Float
0	Normal	Normal

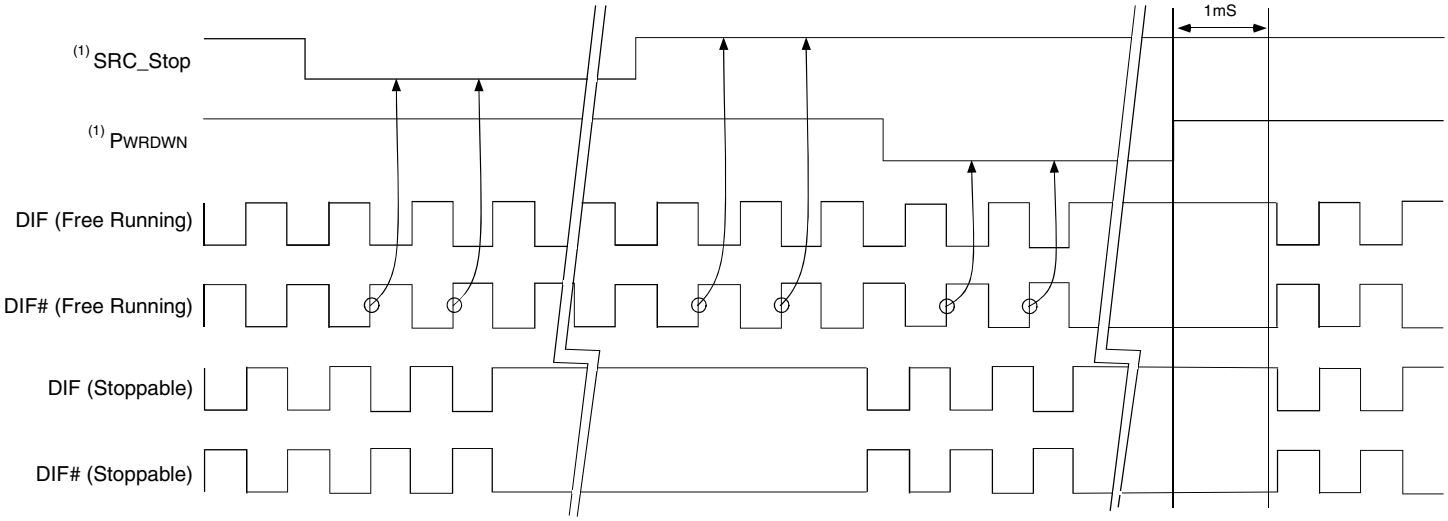
SRC_STOP (OE_INV = 1)

SRC_STOP	DIF	DIF#
1	Iref*6 or Float	Float
0	Normal	Normal

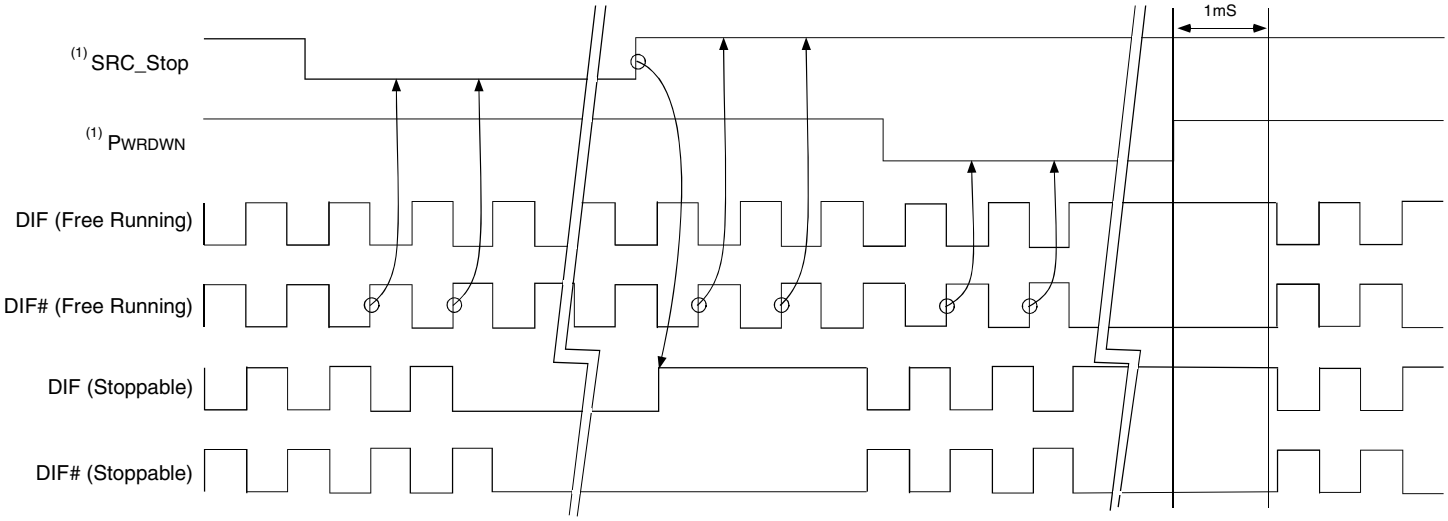
SRC STOP FUNCTIONALITY

The SRC_STOP signal is an input controlling DIF[7:0] and DIF[7:0] # outputs. This signal can be asserted asynchronously. SRC_STOP is active high when OE_INV = HIGH (see OE_INV table).

SRC_STOP = DRIVEN, PWRDWN = DRIVEN

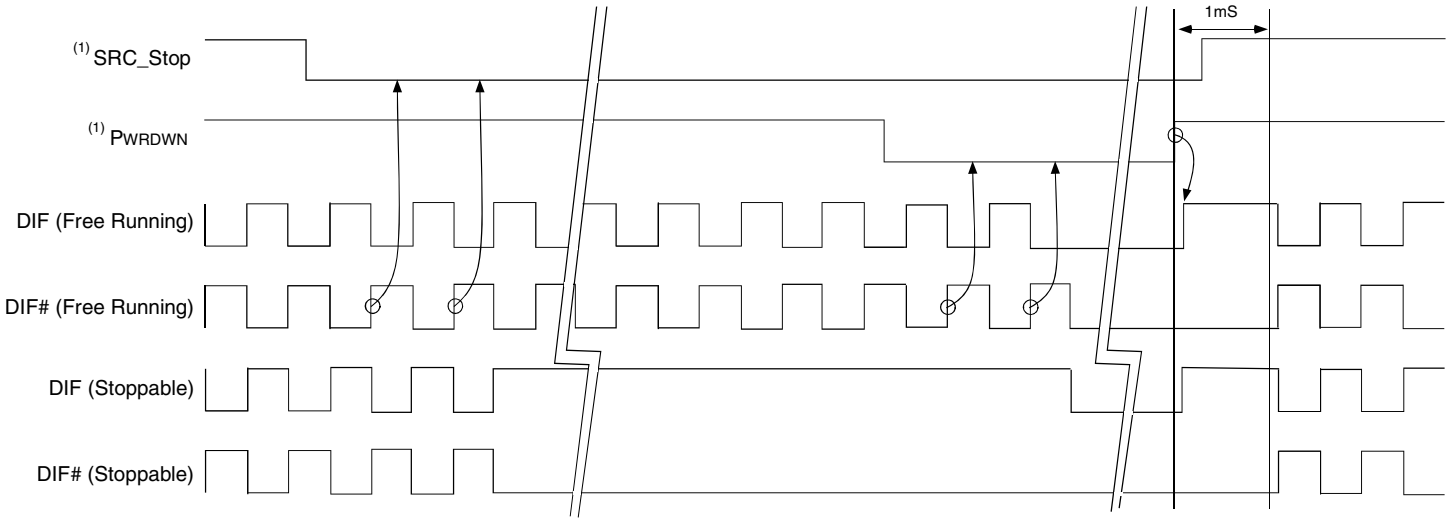


SRC_STOP = TRISTATE, PWRDWN = DRIVEN

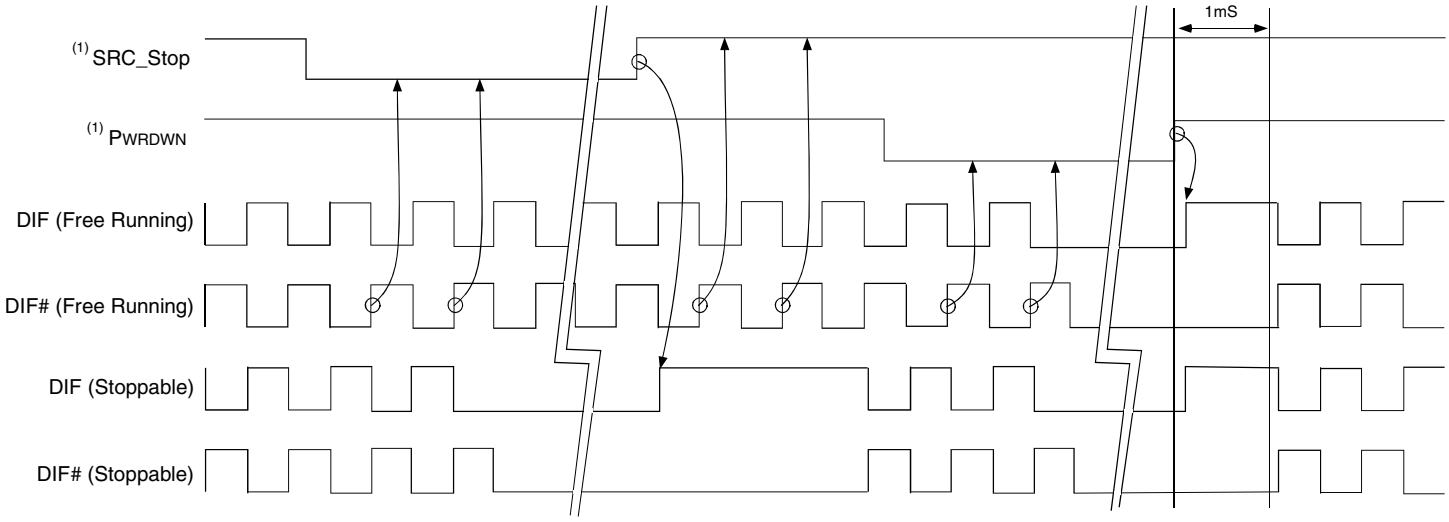


NOTE:
1. The polarity depends on OE_INV.

SRC_STOP = DRIVEN, PWRDWN = TRISTATE

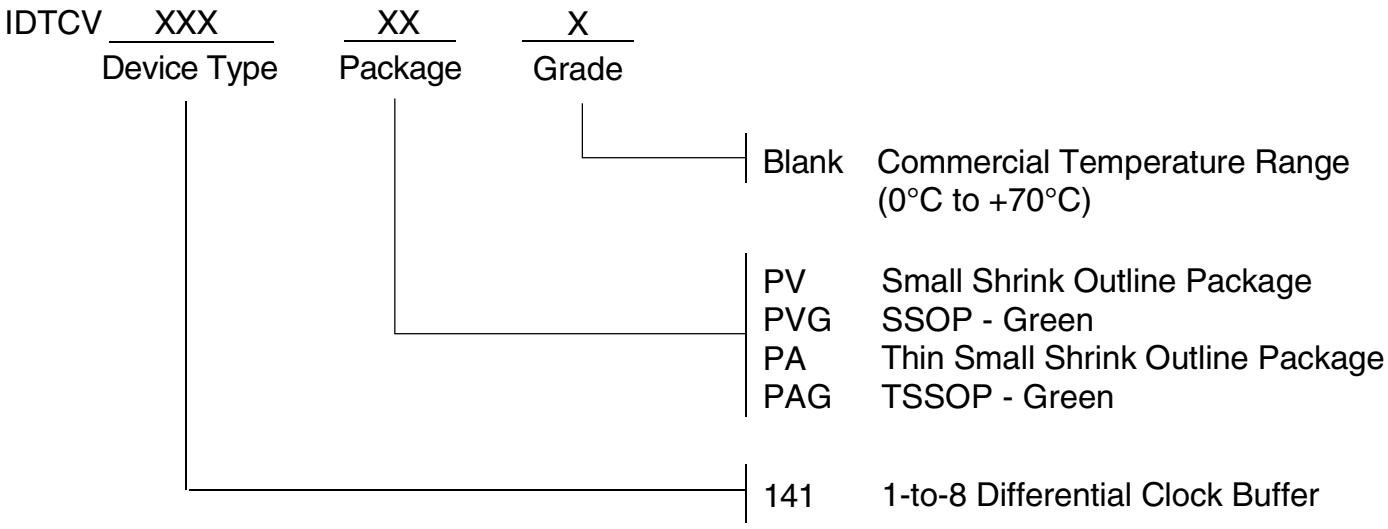


SRC_STOP = TRISTATE, PWRDWN = TRISTATE



NOTE:
1. The polarity depends on OE_INV.

ORDERING INFORMATION



CORPORATE HEADQUARTERS
6024 Silver Creek Valley Road
San Jose, CA 95138

for SALES:
800-345-7015 or 408-284-8200
fax: 408-284-2775
www.idt.com

for Tech Support:
logichelp@idt.com