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DATA SHEET

2-CHANNEL HIGH DEFINITION AUDIO CODEC WITH STAC9202

DESCRIPTION

The STAC9202 is a high fidelity, 2-channel audio CODEC compliant with the High Definition Audio (HD Audio) specification defined by Intel. The STAC9202 implements direct interface to two digital microphones supporting advanced beam forming applications resulting in increased quality of applications requiring voice input.

FEATURES

- **High-integration HD Audio Product**
  - 2-channel PC Audio CODEC
  - Dual Digital Microphone interface
- **Two-Channel DACs and ADCs with 24-bit sample resolution**
  - High performance ΣΔ technology
  - Sample rates up to 192 Hz
  - 100dB DAC SNR
- **Integrated Headphone Amps**
- **Stereo Analog Microphone**
  - Supports Stereo Microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
- **Dual Digital Microphone Interface optimized for use with Akustica Digital Microphones**
- **S/PDIF In and Out**
- **Universal Jacks™ Functionality for jack retasking**
- **Adjustable VREF Out**
- **Digital PC Beep to all outputs**
- **+3.3 V, +4 V and +5 V analog power supply options**
- **48-pin LQFP Environmental Package**

DESCRIPTION

The STAC9202 is a high fidelity, 2-channel, audio CODEC compliant with the High Definition Audio (HD Audio) specification defined by Intel. The STAC9202 provides high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

The STAC9202 incorporates IDT's proprietary ΣΔ technology to achieve a DAC SNR of 100 dB. The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9202 provides stereo, 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9202 SPDIF In/Out support sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF_OUT supports 88.2 KHz. Additional sample rates are supported by the driver software.

The STAC9202 supports flexible configurations including switchable Headphone Out and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC.

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1. DESCRIPTION

1.1. Overview

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The STAC9202 provides stereo, 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9202 SPDIF_IN/SPDIF_OUT support sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF_OUT supports 88.2 KHz. Additional sample rates are supported by the driver software.

The STAC9202 supports flexible configurations including switchable Headphone Out and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC.

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9202 has four General Purpose I/O (GPIO) pins. The STAC9202 also provides a single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9202 integrates a headphone amplifier which is available on Ports A and D. The headphone amplifier is switchable between these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs.

The Universal Jack capabilities allow the CODECs to detect when audio devices are connected to the CODEC, and allow the CODECs to be reconfigured to support these devices, regardless of which port they are plugged into. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

Note: The Jack Detect circuit and component selection are critical for accurate detection of audio jacks on individual ports. Please see the IDT STAC9202 reference design for circuit implementation details.

The STAC9202 operates with a 3.3 V digital supply and a 3.3 V, 4 V and 5 V analog supply.

The STAC9202 is available in a 48-pin LQFP Environmental (ROHS) package.

The STAC9202 implements a direct interface to two digital microphones, supporting advanced beam forming applications resulting in increased quality of applications requiring voice input.

1.2. Features

- High-integration HD Audio Product
  - Two-channel PC Audio CODEC
  - Dual Digital Microphone interface
- Two-Channel DACs and ADCs with 24-bit sample resolution
  - High performance ΣΔ technology
  - Sample rates up to 192 KHz
  - 100dB DAC SNR
- Integrated Headphone Amps
- Stereo Analog Microphone
  - Supports Stereo Mic
  - Microphone Boost 0, 10, 20, 30, 40dB
- Dual Digital Microphone Interface optimized for use with Akustica Digital Microphones
- S/PDIF In and Out
- Universal Jacks™ Functionality for jack retasking
- Adjustable VREF Out
- Digital PC Beep to all outputs
- +3.3 V, 4 V and +5 V analog power supply options
- 48-pin LQFP Environmental Package

2. CHARACTERISTICS

2.1. Audio Fidelity

DAC SNR: 100dB
ADC SNR: 90dB

2.2. Electrical Specifications

2.2.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9202. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0^{o}C to +70^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		260 ^{o}C for 10 seconds * Soldering temperature information for all available packages begins on page 132.

2.2.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: The +4 V Analog voltage is supported by the +5 V version of the STAC9202.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C

ESD: The STAC9202 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9202 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.3. STAC9202 5V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0 V ± 5%, DVdd = 3.3 V ± 5%, AVss = DVss = 0 V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 VRMS, 10 KΩ / 50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here. Specific system characteristics, such as layout, routing and external CODEC component selection influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results.

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel	-	50	-	mWpk
Dynamic Range: -60dB signal level (Note 2)				
PCM to All Analog Outputs	-	99	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	88	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-87	-	dB
HEADPHONE_OUT (32 Ω load)	-	-87	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-90	-	dB
SNR (idle channel) (Note 5)				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	89	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejcn (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-90	-	dB
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-90	-	dB

Parameter	Min	Typ	Max	Unit
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KW
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	5	10	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μsec
PLL (or HD Audio Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured “A weighted” over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured “A weighted” over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.4. STAC9202 4V Analog Performance Characteristics

If you are interested in using the STAC9202 at 4V Analog, please contact IDT for more information.

2.5. STAC9202 3.3V Analog Performance Characteristics

If you are interested in using the STAC9202 at 3.3V Analog, please contact IDT for more information.

2.6. Power Consumption

2.6.1. Digital

Table 1. Digital Power Consumption

Power State	Typical	Max	units
D0	20	25	mA
D1	14	17	mA
D2	14	17	mA
D3	14	17	mA

2.6.2. 5V Analog

Table 2. 5 V Analog Power Consumption

Power State	Typical	Max	units
D0	30	36	mA
D1	12	26	mA
D2	12	26	mA
D3	11	26	mA

3. DETAILED DESCRIPTION

3.1. SPDIF Input

SPDIF_IN can operate at 44.1 KHz, 48 KHz or 96 KHz and implements internal Jack Sensing. A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to accept consumer SPDIF voltage levels directly eliminates the need for costly external receiver ICs. Advanced features such as record slot select and SPDIF_IN routing to the DAC allows for simultaneous record and play.

3.2. SPDIF Output

SPDIF_OUT can operate at 44.1 KHz, 48 KHz, 88.2 KHz and 96 KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

3.3. Digital Microphone Support

The STAC9202 has a three-pin digital microphone interface that accepts high-rate, single-bit data streams from two digital microphones. Each microphone requires only one data line, and both microphones share a single clock line. This robust digital interface gives designers the flexibility to place the microphones in the optimum physical location on a system (such as along the top of the screen bezel) and use a simple, 3-wire ribbon cable to directly connect the microphones to the STAC9202 CODEC.

3.4. Mono Out

The MONO Output is connected to pin 37 and has independent volume and mute control (see the Widget listing for details). The MONO Output derives its input from the output of the summing node that drives PORT A and PORT D. The following analog signals feed the summing amplifier that feeds the MONO Out summing amplifier:

- DAC Output: When enabled, both DAC Outputs are summed together.
- Analog PC BEEP: Source from Pin 12
- ADC Input: Stereo analog feed into the stereo ADC input.

The signals of the stereo channels from the DAC are combined into a single analog signal with a -6dB degradation in signal strength.

3.5. Headphone Drivers Restrictions

It is not recommended that users operate both Port A and Port D as headphone drivers simultaneously. The operation of the two ports as headphone drivers degrades the signal quality of both outputs.[1]

Note: 1) Headphone capabilities are on Port A (pins 39/41) and Port D (pins 35/36). Do NOT put headphone loads on both sets of pins at the same time.

3.6. Universal Jacks

IDT's Universal Jacks technology allows for flexibility in board design and implementation.

On the STAC9202, only one function can be selected at a time. A set of pins cannot be set as input and output at the same time. However, the selected function can be changed at any time.

For the STAC9202 the Universal Jacks capabilities are as follows

- All of the STAC9202 ports support:
  - Line Out
  - Line In
  - Mic with 0/10/20/30/40[2] dB Mic Boost
- Ports A and D also support:
  - Headphone Out[1]

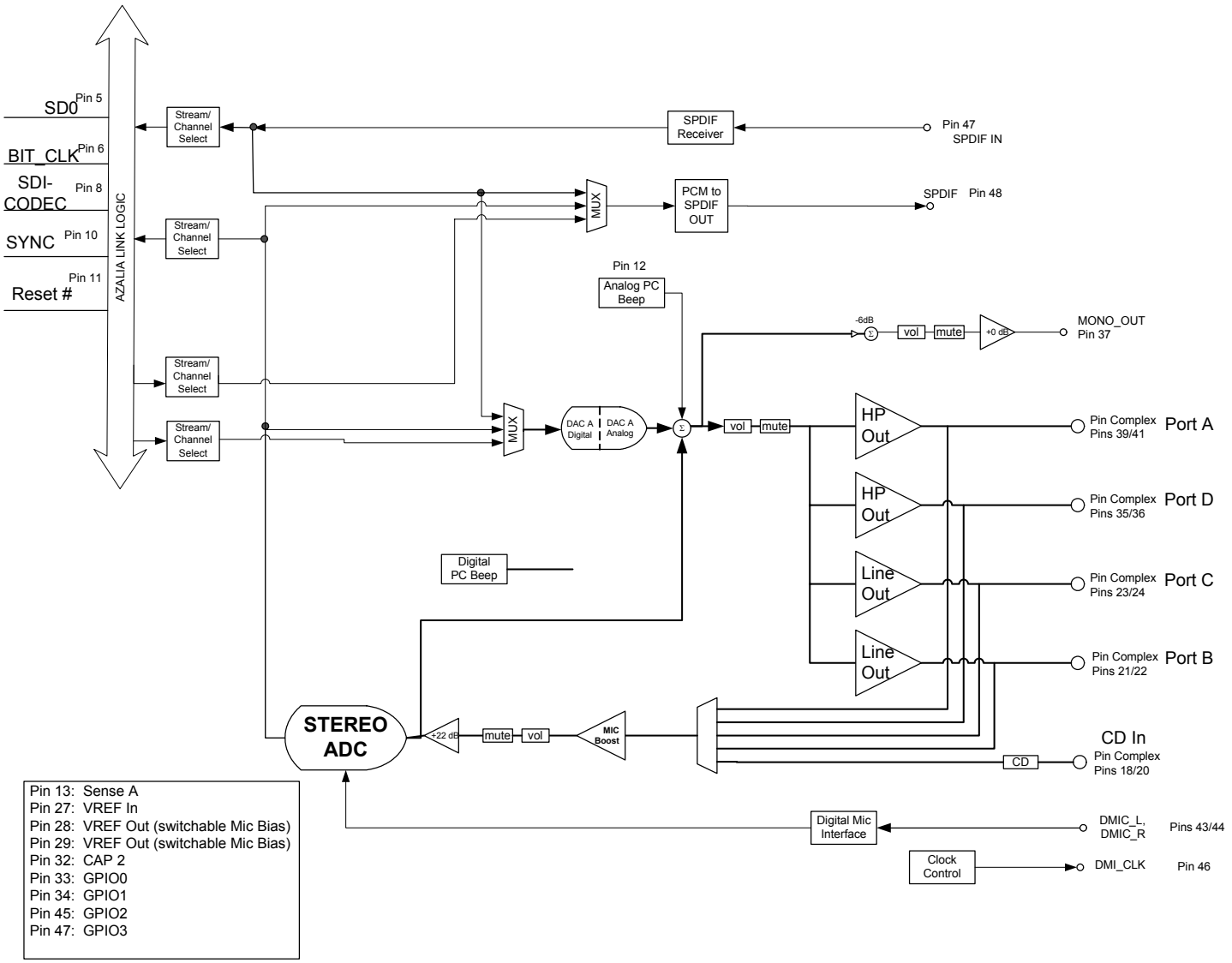
Note: 1) Headphone capabilities are on Port A (pins 39/41) and Port D (pins 35/36). Do NOT put headphone loads on both sets of pins at the same time.

Note: 2) When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

4. FUNCTIONAL BLOCK DIAGRAM

4.1. STAC9202

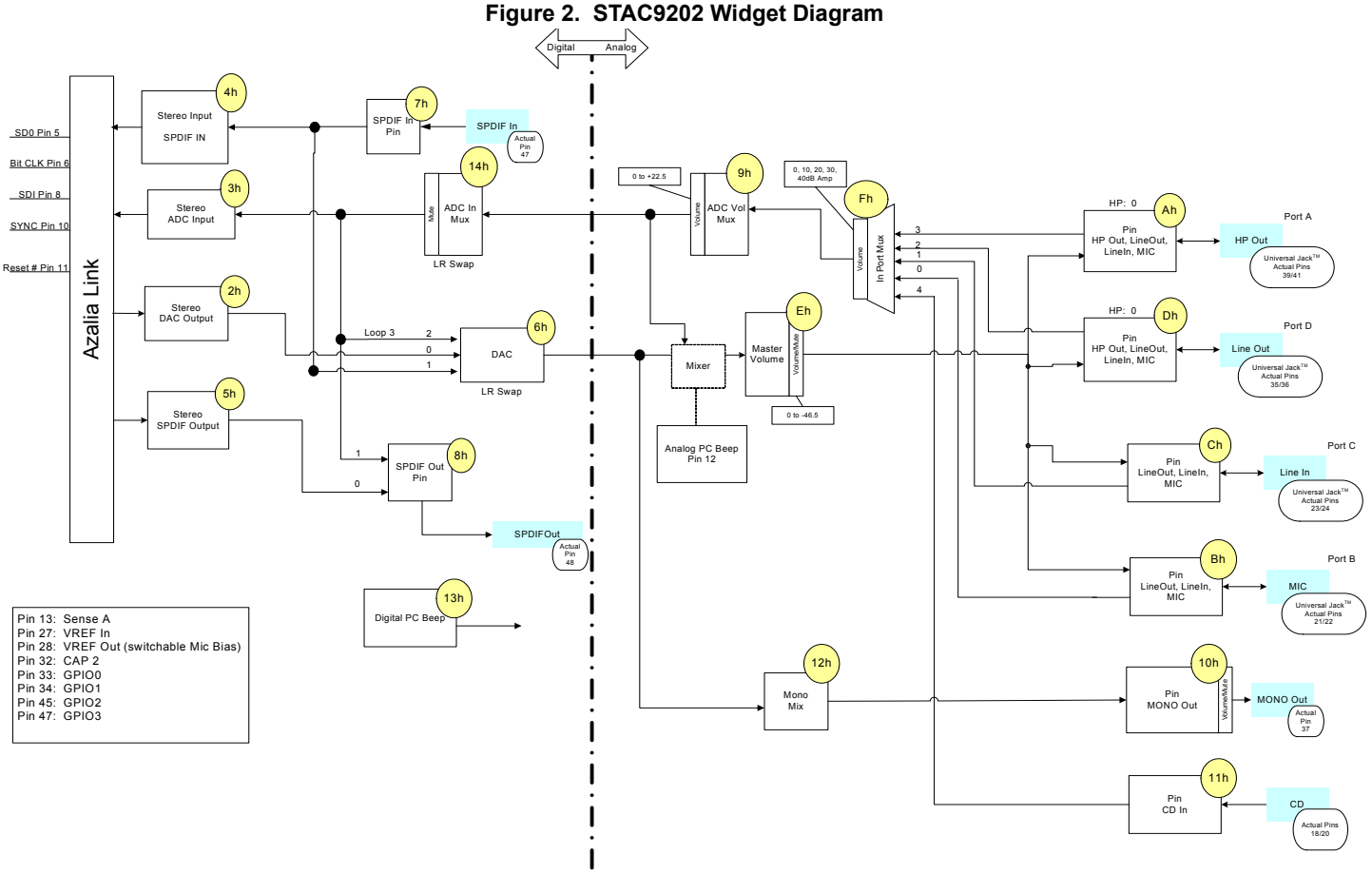
Figure 1. STAC9202 Functional Block Diagram



5. WIDGET DIAGRAM

5.1. STAC9202 Widget Diagram

Figure 2. STAC9202 Widget Diagram



5.2. STAC9202 Widget List

Table 3. High Definition Audio Widget

ID	Widget Name	Description
00h	Root	Root Node
01h	Audio Function Group	Audio Function Group
02h	DAC0	Stereo Ouput to DAC
03h	ADC0	Stereo Input from ADC
04h	SPDIF_IN	Stereo Input for SPDIF_IN
05h	SPDIF_OUT	Stereo Output for SPDIF_OUT
06h	DAC0Mux	DAC Mux and Boost for outputs for DAC
07h	DigPin1	Pin Widget for SPDIF_IN pin 47
08h	DigPin0	Pin Widget for SPDIF_OUT pin 48
09h	ADC0VolMux	ADC0 Volume
0Eh	MasterVolume	Master Volume Controls
0Fh	InPortMux	Port Mux for ADC0
0Ah	Port A	Port A Pin Widget (Pins 39/41, configurable as HP, Line In, Line Out, Mic)
0Dh	Port D	Port D Pin Widget (Pins 35/36, configurable as HP, Line In, Line Out, Mic)
0Ch	Port C	Port C Pin Widget (Pins 23/24, configurable as Line Out, Mic)
0Bh	Port B	Port B Pin Widget (Pins 21/22, configurable as Line Out, Mic)
10h	MonoOut	Mono Output from DAC
11h	CD	CD Pin Widget pins 18/19/20
12h	MonoOutMix	Mixer for Mono Output
13h	Digital PC Beep	Digital PC Beep
14h	ADC0InMux	Input Mux for ADC converter
15h	DigMicPin	Pin Widget for Digital Microphone (Pins 43/44/46 configurable as a Mic)

5.3. Root Node (NID = 0x00)

5.3.1. Root PnpID

Table 4. Root PnpID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table

Table 5. Root PnpID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Vendor	R	0x8384	Vendor ID = 8384h
[15:0]	Device	R	0x7630	Device ID for: STAC9202 = 7632

5.3.2. Root RevID

Table 6. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table

Table 7. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd	R	0x00	Reserved
[23:20]	Major	R	0x1	Major rev number of compliant HD Audio specification
[19:16]	Minor	R	0x0	Minor rev number of compliant HD Audio specification
[15:8]	Vendor	R	0x01	Vendor rev number for this device ID
[7:0]	Stepping	R	0x01	Vendor stepping number within the given Vendor RevID

5.3.3. Root NodeInfo

Table 8. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 9. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x00	Reserved
[23:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15:8]	Rsvd1	R	0x00	Reserved
[7:0]	TotalNodes	R	0x01	Total number of nodes

5.4. AFG Node (NID = 0x01)

5.4.1. AFG Reset

Table 10. AFG Reset Command Verb Format

	Verb ID	Payload	Response
Get	7FF	00	See bitfield table
Set1	7FF	See bits [7:0] of bitfield table	0000_0000h

Table 11. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

5.4.2. AFG NodeInfo

Table 12. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 13. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:16]	StartNID	R	0x02	Starting node number for function group subordinate nodes.
[15:8]	Rsvd1	R	0x0	Reserved
[7:0]	TotalNodes	R	0x14	Total number of nodes. 14h = STAC9202

5.4.3. AFG Type

Table 14. AFG Type Command Verb Format

	Verb ID	Payload	Response
Get	F00	05	See bitfield table

Table 15. AFG Type Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:9]	Rsvd	R	0x0	Reserved
[8]	Unsol	R	0x1	This node is capable of generating an unsolicited response, and will respond to the Unsolicited Response verb (Verb ID 708h).
[7:0]	NodeType	R	0x01	Node type = Audio Function Group

5.4.4. AFG GrpCap

Table 16. AFG GrpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	08	See bitfield table

Table 17. AFG GrpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd3	R	0x0	Reserved
[16]	BeepGen	R	0x1	Optional Beep Generator is present
[15:12]	Rsvd2	R	0x0	Reserved
[11:8]	InputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.

Table 17. AFG GrpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7:4]	Rsvd1	R	0x0	Reserved
[3:0]	OutputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.

5.4.5. AFG FrmtCap

Table 18. AFG FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 19. AFG FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported