



Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!



## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



**2-CHANNEL HIGH DEFINITION AUDIO CODEC WITH****STAC9202****DESCRIPTION**

The STAC9202 is a high fidelity, 2-channel audio CODEC compliant with the High Definition Audio (HD Audio) specification defined by Intel. The STAC9202 implements direct interface to two digital microphones supporting advanced beam forming applications resulting in increased quality of applications requiring voice input.

**FEATURES**

- **High-integration HD Audio Product**
  - 2-channel PC Audio CODEC
  - Dual Digital Microphone interface
- **Two-Channel DACs and ADCs with 24-bit sample resolution**
  - High performance  $\Sigma\Delta$  technology
  - Sample rates up to 192 Hz
  - 100dB DAC SNR
- **Integrated Headphone Amps**
- **Stereo Analog Microphone**
  - Supports Stereo Microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
- **Dual Digital Microphone Interface optimized for use with Akustica Digital Microphones**
- **S/PDIF In and Out**
- **Universal Jacks™ Functionality for jack retasking**
- **Adjustable VREF Out**

- **Digital PC Beep to all outputs**
- **+3.3 V, +4 V and +5 V analog power supply options**
- **48-pin LQFP Environmental Package**

**DESCRIPTION**

The STAC9202 is a high fidelity, 2-channel, audio CODEC compliant with the High Definition Audio (HD Audio) specification defined by Intel. The STAC9202 provides high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

The STAC9202 incorporates IDT's proprietary  $\Sigma\Delta$  technology to achieve a DAC SNR of 100 dB. The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9202 provides stereo, 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9202 SPDIF In/Out support sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF\_OUT supports 88.2 KHz. Additional sample rates are supported by the driver software.

The STAC9202 supports flexible configurations including switchable Headphone Out and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. All analog I/O pairs support LINE\_IN, LINE\_OUT and MIC.

## Table of Contents

<b>1. DESCRIPTION</b>	<b>9</b>
1.1. Overview	9
1.2. Features	10
<b>2. CHARACTERISTICS</b>	<b>11</b>
2.1. Audio Fidelity	11
2.2. Electrical Specifications	11
2.3. STAC9202 5V Analog Performance Characteristics	13
2.4. STAC9202 4V Analog Performance Characteristics	14
2.5. STAC9202 3.3V Analog Performance Characteristics	14
2.6. Power Consumption	15
<b>3. DETAILED DESCRIPTION</b>	<b>16</b>
3.1. SPDIF Input	16
3.2. SPDIF Output	16
3.3. Digital Microphone Support	16
3.4. Mono Out	16
3.5. Headphone Drivers Restrictions	16
3.6. Universal Jacks	17
<b>4. FUNCTIONAL BLOCK DIAGRAM</b>	<b>18</b>
4.1. STAC9202	18
<b>5. WIDGET DIAGRAM</b>	<b>19</b>
5.1. STAC9202 Widget Diagram	19
5.2. STAC9202 Widget List	20
5.3. Root Node (NID = 0x00)	21
5.4. AFG Node (NID = 0x01)	22
5.5. DAC0Cnvtr Node (NID = 0x02)	37
5.6. ADC0Cnvtr Node (NID = 0x03)	41
5.7. SPDIFinCnvtr Node (NID = 0x04)	46
5.8. SPDIFoutCnvtr Node (NID = 0x05)	52
5.9. DAC0Mux Node (NID = 0x06)	57
5.10. DigInPin Node (NID = 0x07)	60
5.11. DigOutPin Node (NID = 0x08)	66
5.12. ADC0VolMux Node (NID = 0x09)	71
5.13. MasterVol Node (NID = 0x0E)	75
5.14. InPortMux Node (NID = 0x0F)	78
5.15. PortAPin Node (NID = 0x0A)	82
5.16. PortDPin Node (NID = 0x0D)	88
5.17. PortCPin Node (NID = 0x0C)	93
5.18. PortBPin Node (NID = 0x0B)	99
5.19. MonoOutPin Node (NID = 0x10)	105
5.20. CDPin Node (NID = 0x11)	110
5.21. MonoOutMix Node (NID = 0x12)	113
5.22. PCBeep Node (NID = 0x13)	115
5.23. ADC0InMux Node (NID = 0x14)	118
5.24. DigMicPin Node (NID = 0x15)	123
<b>6. ORDERING INFORMATION</b>	<b>127</b>
6.1. STAC9202 Options and Part Numbers	127
<b>7. PIN INFORMATION</b>	<b>128</b>
7.1. STAC9202 Pin Diagram	128
7.2. Pin Table for STAC9202	128
<b>8. PACKAGE DRAWINGS</b>	<b>131</b>
8.1. 48-Pin LQFP	131
<b>9. SOLDER REFLOW PROFILE</b>	<b>132</b>
9.1. Standard Reflow Profile Data	132

9.2. Pb Free Process - Package Classification Reflow Temperatures .....	133
<b>10. REVISION HISTORY .....</b>	<b>134</b>

## List of Figures

Figure 1. STAC9202 Functional Block Diagram .....	18
Figure 2. STAC9202 Widget Diagram .....	19
Figure 3. STAC9202 Pin Diagram .....	128
Figure 4. 48-Pin LQFP Package Outline and Package Dimensions .....	131
Figure 5. Solder Reflow Profile .....	132

## List of Tables

Table 1. Digital Power Consumption .....	15
Table 2. 5 V Analog Power Consumption .....	15
Table 3. High Definition Audio Widget .....	20
Table 4. Root PnpID Command Verb Format .....	21
Table 5. Root PnpID Command Response Format .....	21
Table 6. Root RevID Command Verb Format .....	21
Table 7. Root RevID Command Response Format .....	21
Table 8. Root NodeInfo Command Verb Format .....	22
Table 9. Root NodeInfo Command Response Format .....	22
Table 10. AFG Reset Command Verb Format .....	22
Table 11. AFG Reset Command Response Format .....	23
Table 12. AFG NodeInfo Command Verb Format .....	23
Table 13. AFG NodeInfo Command Response Format .....	23
Table 14. AFG Type Command Verb Format .....	24
Table 15. AFG Type Command Response Format .....	24
Table 16. AFG GrpCap Command Verb Format .....	24
Table 17. AFG GrpCap Command Response Format .....	24
Table 18. AFG FrmtCap Command Verb Format .....	25
Table 19. AFG FrmtCap Command Response Format .....	25
Table 20. AFG StreamCap Command Verb Format .....	26
Table 21. AFG StreamCap Command Response Format .....	26
Table 22. AFG PwrCap Command Verb Format .....	26
Table 23. AFG PwrCap Command Response Format .....	27
Table 24. AFG GPIOCap Command Verb Format .....	27
Table 25. AFG GPIOCap Command Response Format .....	28
Table 26. AFG OutAmpCap Command Verb Format .....	28
Table 27. AFG OutAmpCap Command Response Format .....	28
Table 28. AFG PwrState Command Verb Format .....	29
Table 29. AFG PwrState Command Response Format .....	29
Table 30. AFG UnsolResp Command Verb Format .....	29
Table 31. AFG UnsolResp Command Response Format .....	30
Table 32. AFG GPIO Command Verb Format .....	30
Table 33. AFG GPIO Command Response Format .....	30
Table 34. AFG GPIOEn Command Verb Format .....	31
Table 35. AFG GPIOEn Command Response Format .....	31
Table 36. AFG GPIODir Command Verb Format .....	32
Table 37. AFG GPIODir Command Response Format .....	32
Table 38. AFG GPIOWake Command Verb Format .....	33
Table 39. AFG GPIOWake Command Response Format .....	33



Table 40. AFG GPIOUnsolEn Command Verb Format .....	33
Table 41. AFG GPIOUnsolEn Command Response Format .....	34
Table 42. AFG GPIOSticky Command Verb Format .....	34
Table 43. AFG GPIOSticky Command Response Format .....	35
Table 44. AFG SysID Command Verb Format .....	35
Table 45. AFG SysID Command Response Format .....	36
Table 46. AFG DigMic Command Verb Format .....	36
Table 47. AFG DigMic Command Response Format .....	36
Table 48. DAC0Cnvtr Frmt Command Verb Format .....	37
Table 49. DAC0Cnvtr Frmt Command Response Format .....	37
Table 50. DAC0Cnvtr WCap Command Verb Format .....	38
Table 51. DAC0Cnvtr WCap Command Response Format .....	38
Table 52. DAC0Cnvtr PwrState Command Verb Format .....	39
Table 53. DAC0Cnvtr PwrState Command Response Format .....	39
Table 54. DAC0Cnvtr Stream Command Verb Format .....	40
Table 55. DAC0Cnvtr Stream Command Response Format .....	40
Table 56. ADC0Cnvtr Frmt Command Verb Format .....	41
Table 57. ADC0Cnvtr Frmt Command Response Format .....	41
Table 58. ADC0Cnvtr WCap Command Verb Format .....	42
Table 59. ADC0Cnvtr WCap Command Response Format .....	42
Table 60. ADC0Cnvtr ConnLen Command Verb Format .....	43
Table 61. ADC0Cnvtr ConnLen Command Response Format .....	43
Table 62. ADC0Cnvtr ConnLst Command Verb Format .....	44
Table 63. ADC0Cnvtr ConnLst Command Response Format .....	44
Table 64. ADC0Cnvtr ProcState Command Verb Format .....	44
Table 65. ADC0Cnvtr ProcState Command Response Format .....	44
Table 66. ADC0Cnvtr PwrState Command Verb Format .....	45
Table 67. ADC0Cnvtr PwrState Command Response Format .....	45
Table 68. ADC0Cnvtr Stream Command Verb Format .....	45
Table 69. ADC0Cnvtr Stream Command Response Format .....	45
Table 70. SPDIFinCnvtr Frmt Command Verb Format .....	46
Table 71. SPDIFinCnvtr Frmt Command Response Format .....	46
Table 72. SPDIFinCnvtr WCap Command Verb Format .....	47
Table 73. SPDIFinCnvtr WCap Command Response Format .....	47
Table 74. SPDIFinCnvtr FrmtCap Command Verb Format .....	48
Table 75. SPDIFinCnvtr FrmtCap Command Response Format .....	48
Table 76. SPDIFinCnvtr StreamCap Command Verb Format .....	49
Table 77. SPDIFinCnvtr StreamCap Command Response Format .....	50
Table 78. SPDIFinCnvtr ConnLen Command Verb Format .....	50
Table 79. SPDIFinCnvtr ConnLen Command Response Format .....	50
Table 80. SPDIFinCnvtr ConnLst Command Verb Format .....	50
Table 81. SPDIFinCnvtr ConnLst Command Response Format .....	51
Table 82. SPDIFinCnvtr Stream Command Verb Format .....	51
Table 83. SPDIFinCnvtr Stream Command Response Format .....	51
Table 84. SPDIFinCnvtr DigCtl Command Verb Format .....	51
Table 85. SPDIFinCnvtr DigCtl Command Response Format .....	52
Table 86. SPDIFoutCnvtr Frmt Command Verb Format .....	52
Table 87. SPDIFoutCnvtr Frmt Command Response Format .....	53
Table 88. SPDIFoutCnvtr WCap Command Verb Format .....	54
Table 89. SPDIFoutCnvtr WCap Command Response Format .....	54
Table 90. SPDIFoutCnvtr FrmtCap Command Verb Format .....	55
Table 91. SPDIFoutCnvtr FrmtCap Command Response Format .....	55
Table 92. SPDIFoutCnvtr StreamCap Command Verb Format .....	56
Table 93. SPDIFoutCnvtr StreamCap Command Response Format .....	56
Table 94. SPDIFoutCnvtr Stream Command Verb Format .....	56

Table 95. SPDIFoutCnvtr Stream Command Response Format .....	56
Table 96. SPDIFoutCnvtr DigCtl Command Verb Format .....	57
Table 97. SPDIFoutCnvtr DigCtl Command Response Format .....	57
Table 98. DAC0Mux WCap Command Verb Format .....	57
Table 99. DAC0Mux WCap Command Response Format .....	58
Table 100. DAC0Mux ConnLen Command Verb Format .....	58
Table 101. DAC0Mux ConnLen Command Response Format .....	59
Table 102. DAC0Mux ConnSel Command Verb Format .....	59
Table 103. DAC0Mux ConnSel Command Response Format .....	59
Table 104. DAC0Mux ConnLst Command Verb Format .....	59
Table 105. DAC0Mux ConnLst Command Response Format .....	59
Table 106. DAC0Mux LR Command Verb Format .....	60
Table 107. DAC0Mux LR Command Response Format .....	60
Table 108. DigInPin WCap Command Verb Format .....	60
Table 109. DigInPin WCap Command Response Format .....	61
Table 110. DigInPin Cap Command Verb Format .....	61
Table 111. DigInPin Cap Command Response Format .....	62
Table 112. DigInPin PwrState Command Verb Format .....	62
Table 113. DigInPin PwrState Command Response Format .....	62
Table 114. DigInPin Ctl Command Verb Format .....	63
Table 115. DigInPin Ctl Command Response Format .....	63
Table 116. DigInPin UnsolResp Command Verb Format .....	63
Table 117. DigInPin UnsolResp Command Response Format .....	64
Table 118. DigInPin Sense Command Verb Format .....	64
Table 119. DigInPin Sense Command Response Format .....	64
Table 120. DigInPin EAPD Command Verb Format .....	65
Table 121. DigInPin EAPD Command Response Format .....	65
Table 122. DigInPin Config Command Verb Format .....	65
Table 123. DigInPin Config Command Response Format .....	66
Table 124. DigOutPin WCap Command Verb Format .....	66
Table 125. DigOutPin WCap Command Response Format .....	66
Table 126. DigOutPin Cap Command Verb Format .....	67
Table 127. DigOutPin Cap Command Response Format .....	67
Table 128. DigOutPin ConnLen Command Verb Format .....	68
Table 129. DigOutPin ConnLen Command Response Format .....	68
Table 130. DigOutPin ConnSel Command Verb Format .....	69
Table 131. DigOutPin ConnSel Command Response Format .....	69
Table 132. DigOutPin ConnLst Command Verb Format .....	69
Table 133. DigOutPin ConnLst Command Response Format .....	69
Table 134. DigOutPin Ctl Command Verb Format .....	70
Table 135. DigOutPin Ctl Command Response Format .....	70
Table 136. DigOutPin Config Command Verb Format .....	70
Table 137. DigOutPin Config Command Response Format .....	70
Table 138. ADC0VolMux VolRight Command Verb Format .....	71
Table 139. ADC0VolMux VolRight Command Response Format .....	71
Table 140. ADC0VolMux VolLeft Command Verb Format .....	72
Table 141. ADC0VolMux VolLeft Command Response Format .....	72
Table 142. ADC0VolMux WCap Command Verb Format .....	72
Table 143. ADC0VolMux WCap Command Response Format .....	72
Table 144. ADC0VolMux OutAmpCap Command Verb Format .....	73
Table 145. ADC0VolMux OutAmpCap Command Response Format .....	73
Table 146. ADC0VolMux ConnLen Command Verb Format .....	74
Table 147. ADC0VolMux ConnLen Command Response Format .....	74
Table 148. ADC0VolMux ConnLst Command Verb Format .....	74
Table 149. ADC0VolMux ConnLst Command Response Format .....	74

Table 150. MasterVol Right Command Verb Format .....	75
Table 151. MasterVol Right Command Response Format .....	75
Table 152. MasterVol Left Command Verb Format .....	75
Table 153. MasterVol Left Command Response Format .....	75
Table 154. MasterVol WCap Command Verb Format .....	76
Table 155. MasterVol WCap Command Response Format .....	76
Table 156. MasterVol ConnLen Command Verb Format .....	77
Table 157. MasterVol ConnLen Command Response Format .....	77
Table 158. MasterVol ConnLst Command Verb Format .....	77
Table 159. MasterVol ConnLst Command Response Format .....	77
Table 160. InPortMux VolRight Command Verb Format .....	78
Table 161. InPortMux VolRight Command Response Format .....	78
Table 162. InPortMux VolLeft Command Verb Format .....	78
Table 163. InPortMux VolLeft Command Response Format .....	78
Table 164. InPortMux WCap Command Verb Format .....	78
Table 165. InPortMux WCap Command Response Format .....	79
Table 166. InPortMux ConnLen Command Verb Format .....	79
Table 167. InPortMux ConnLen Command Response Format .....	80
Table 168. InPortMux AmpCap Command Verb Format .....	80
Table 169. InPortMux AmpCap Command Response Format .....	80
Table 170. InPortMux ConnSel Command Verb Format .....	81
Table 171. InPortMux ConnSel Command Response Format .....	81
Table 172. InPortMux ConnLst0 Command Verb Format .....	81
Table 173. InPortMux ConnLst0 Command Response Format .....	81
Table 174. InPortMux ConnLst4 Command Verb Format .....	81
Table 175. InPortMux ConnLst4 Command Response Format .....	82
Table 176. PortAPin WCap Command Verb Format .....	82
Table 177. PortAPin WCap Command Response Format .....	82
Table 178. PortAPin Cap Command Verb Format .....	83
Table 179. PortAPin Cap Command Response Format .....	83
Table 180. PortAPin ConnLen Command Verb Format .....	84
Table 181. PortAPin ConnLen Command Response Format .....	84
Table 182. PortAPin ConnLst Command Verb Format .....	84
Table 183. PortAPin ConnLst Command Response Format .....	84
Table 184. PortAPin Ctl Command Verb Format .....	85
Table 185. PortAPin Ctl Command Response Format .....	85
Table 186. PortAPin UnsolResp Command Verb Format .....	85
Table 187. PortAPin UnsolResp Command Response Format .....	85
Table 188. PortAPin Sense Command Verb Format .....	86
Table 189. PortAPin Sense Command Response Format .....	86
Table 190. PortAPin Config Command Verb Format .....	87
Table 191. PortAPin Config Command Response Format .....	87
Table 192. PortDPin WCap Command Verb Format .....	88
Table 193. PortDPin WCap Command Response Format .....	88
Table 194. PortDPin Cap Command Verb Format .....	89
Table 195. PortDPin Cap Command Response Format .....	89
Table 196. PortDPin ConnLen Command Verb Format .....	89
Table 197. PortDPin ConnLen Command Response Format .....	90
Table 198. PortDPin ConnLst Command Verb Format .....	90
Table 199. PortDPin ConnLst Command Response Format .....	90
Table 200. PortDPin Ctl Command Verb Format .....	90
Table 201. PortDPin Ctl Command Response Format .....	91
Table 202. PortDPin UnsolResp Command Verb Format .....	91
Table 203. PortDPin UnsolResp Command Response Format .....	91
Table 204. PortDPin Sense Command Verb Format .....	92

Table 205. PortDPin Sense Command Response Format .....	92
Table 206. PortDPin Config Command Verb Format .....	92
Table 207. PortDPin Config Command Response Format .....	93
Table 208. PortCPin WCap Command Verb Format .....	93
Table 209. PortCPin WCap Command Response Format .....	93
Table 210. PortCPin Cap Command Verb Format .....	94
Table 211. PortCPin Cap Command Response Format .....	94
Table 212. PortCPin ConnLen Command Verb Format .....	95
Table 213. PortCPin ConnLen Command Response Format .....	95
Table 214. PortCPin ConnLst Command Verb Format .....	96
Table 215. PortCPin ConnLst Command Response Format .....	96
Table 216. PortCPin Ctl Command Verb Format .....	96
Table 217. PortCPin Ctl Command Response Format .....	96
Table 218. PortCPin UnsolResp Command Verb Format .....	97
Table 219. PortCPin UnsolResp Command Response Format .....	97
Table 220. PortCPin Sense Command Verb Format .....	98
Table 221. PortCPin Sense Command Response Format .....	98
Table 222. PortCPin Config Command Verb Format .....	98
Table 223. PortCPin Config Command Response Format .....	99
Table 224. PortBPin WCap Command Verb Format .....	99
Table 225. PortBPin WCap Command Response Format .....	99
Table 226. PortBPin Cap Command Verb Format .....	100
Table 227. PortBPin Cap Command Response Format .....	100
Table 228. PortBPin ConnLen Command Verb Format .....	101
Table 229. PortBPin ConnLen Command Response Format .....	101
Table 230. PortBPin ConnLst Command Verb Format .....	102
Table 231. PortBPin ConnLst Command Response Format .....	102
Table 232. PortBPin Ctl Command Verb Format .....	102
Table 233. PortBPin Ctl Command Response Format .....	102
Table 234. PortBPin UnsolResp Command Verb Format .....	103
Table 235. PortBPin UnsolResp Command Response Format .....	103
Table 236. PortBPin Sense Command Verb Format .....	104
Table 237. PortBPin Sense Command Response Format .....	104
Table 238. PortBPin Config Command Verb Format .....	104
Table 239. PortBPin Config Command Response Format .....	105
Table 240. MonoOutPin Vol Command Verb Format .....	105
Table 241. MonoOutPin Vol Command Response Format .....	105
Table 242. MonoOutPin WCap Command Verb Format .....	106
Table 243. MonoOutPin WCap Command Response Format .....	106
Table 244. MonoOutPin Cap Command Verb Format .....	107
Table 245. MonoOutPin Cap Command Response Format .....	107
Table 246. MonoOutPin ConnLen Command Verb Format .....	108
Table 247. MonoOutPin ConnLen Command Response Format .....	108
Table 248. MonoOutPin ConnLst Command Verb Format .....	108
Table 249. MonoOutPin ConnLst Command Response Format .....	108
Table 250. MonoOutPin Ctl Command Verb Format .....	109
Table 251. MonoOutPin Ctl Command Response Format .....	109
Table 252. MonoOutPin Config Command Verb Format .....	109
Table 253. MonoOutPin Config Command Response Format .....	109
Table 254. CDPin WCap Command Verb Format .....	110
Table 255. CDPin WCap Command Response Format .....	110
Table 256. CDPin Cap Command Verb Format .....	111
Table 257. CDPin Cap Command Response Format .....	111
Table 258. CDPin Ctl Command Verb Format .....	112
Table 259. CDPin Ctl Command Response Format .....	112



Table 260. CDPin Config Command Verb Format .....	112
Table 261. CDPin Config Command Response Format .....	113
Table 262. MonoOutMix WCap Command Verb Format .....	113
Table 263. MonoOutMix WCap Command Response Format .....	114
Table 264. MonoOutMix ConnLen Command Verb Format .....	114
Table 265. MonoOutMix ConnLen Command Response Format .....	115
Table 266. MonoOutMix ConnLst Command Verb Format .....	115
Table 267. MonoOutMix ConnLst Command Response Format .....	115
Table 268. PCBeep Vol Command Verb Format .....	115
Table 269. PCBeep Vol Command Response Format .....	116
Table 270. PCBeep WCap Command Verb Format .....	116
Table 271. PCBeep WCap Command Response Format .....	116
Table 272. PCBeep OutAmpCap Command Verb Format .....	117
Table 273. PCBeep OutAmpCap Command Response Format .....	117
Table 274. PCBeep Gen Command Verb Format .....	117
Table 275. PCBeep Gen Command Response Format .....	118
Table 276. ADC0InMux WCap Command Verb Format .....	118
Table 277. ADC0InMux WCap Command Response Format .....	118
Table 278. ADC0InMux ConnLen Command Verb Format .....	119
Table 279. ADC0InMux ConnLen Command Response Format .....	119
Table 280. ADC0InMux ConnSel Command Verb Format .....	120
Table 281. ADC0InMux ConnSel Command Response Format .....	120
Table 282. ADC0InMux ConnLst Command Verb Format .....	120
Table 283. ADC0InMux ConnLst Command Response Format .....	120
Table 284. ADC0InMux LR Command Verb Format .....	121
Table 285. ADC0InMux LR Command Response Format .....	121
Table 286. ADC0InMux OutAmpCap Command Verb Format .....	121
Table 287. ADC0InMux OutAmpCap Command Response Format .....	121
Table 288. ADC0InMux VolRight Command Verb Format .....	122
Table 289. ADC0InMux VolRight Command Response Format .....	122
Table 290. ADC0InMux VolLeft Command Verb Format .....	122
Table 291. ADC0InMux VolLeft Command Response Format .....	122
Table 292. DigMicPin WCap Command Verb Format .....	123
Table 293. DigMicPin WCap Command Response Format .....	123
Table 294. DigMicPin Cap Command Verb Format .....	124
Table 295. DigMicPin Cap Command Response Format .....	124
Table 296. DigMicPin Ctl Command Verb Format .....	125
Table 297. DigMicPin Ctl Command Response Format .....	125
Table 298. DigMicPin Config Command Verb Format .....	125
Table 299. DigMicPin Config Command Response Format .....	125

## 1. DESCRIPTION

### 1.1. Overview

The STAC9202 is a high fidelity, 2-channel, audio CODEC compliant with the High Definition Audio (HD Audio) specification defined by Intel. The STAC9202 provides high quality, HD Audio capability to notebook and cost sensitive desktop PC applications.

The STAC9202 incorporates IDT's proprietary  $\Sigma\Delta$  technology to achieve a DAC SNR of 100 dB. The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9202 provides stereo, 24-bit, full duplex resolution supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9202 SPDIF\_IN/SPDIF\_OUT support sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF\_OUT supports 88.2 KHz. Additional sample rates are supported by the driver software.

The STAC9202 supports flexible configurations including switchable Headphone Out and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to Consumer Electronic equipment like Dolby Digital decoders, powered speakers, mini disk drives or to a home entertainment system. All analog I/O pairs support LINE\_IN, LINE\_OUT and MIC.

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9202 has four General Purpose I/O (GPIO) pins. The STAC9202 also provides a single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9202 integrates a headphone amplifier which is available on Ports A and D. The headphone amplifier is switchable between these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs.

The Universal Jack capabilities allow the CODECs to detect when audio devices are connected to the CODEC, and allow the CODECs to be reconfigured to support these devices, regardless of which port they are plugged into. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

*Note: The Jack Detect circuit and component selection are critical for accurate detection of audio jacks on individual ports. Please see the IDT STAC9202 reference design for circuit implementation details.*

The STAC9202 operates with a 3.3 V digital supply and a 3.3 V, 4 V and 5 V analog supply.

The STAC9202 is available in a 48-pin LQFP Environmental (ROHS) package.

The STAC9202 implements a direct interface to two digital microphones, supporting advanced beam forming applications resulting in increased quality of applications requiring voice input.

## 1.2. Features

- High-integration HD Audio Product
  - Two-channel PC Audio CODEC
  - Dual Digital Microphone interface
- Two-Channel DACs and ADCs with 24-bit sample resolution
  - High performance  $\Sigma\Delta$  technology
  - Sample rates up to 192 KHz
  - 100dB DAC SNR
- Integrated Headphone Amps
- Stereo Analog Microphone
  - Supports Stereo Mic
  - Microphone Boost 0, 10, 20, 30, 40dB
- Dual Digital Microphone Interface optimized for use with Akustica Digital Microphones
- S/PDIF In and Out
- Universal Jacks™ Functionality for jack retasking
- Adjustable VREF Out
- Digital PC Beep to all outputs
- +3.3 V, 4 V and +5 V analog power supply options
- 48-pin LQFP Environmental Package

## 2. CHARACTERISTICS

### 2.1. Audio Fidelity

DAC SNR: 100dB

ADC SNR: 90dB

### 2.2. Electrical Specifications

#### 2.2.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9202. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0°C to +70°C
Storage temperature		-55 °C to +125 °C
Soldering temperature		260 °C for 10 seconds * Soldering temperature information for all available packages begins on page 132.

#### 2.2.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: The +4 V Analog voltage is supported by the +5 V version of the STAC9202.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T <sub>case</sub> (48-LQFP)			+90	°C

***ESD:*** The STAC9202 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9202 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

### 2.3. STAC9202 5V Analog Performance Characteristics

( $T_{\text{ambient}} = 25\text{ }^{\circ}\text{C}$ ,  $AV_{\text{dd}} = 5.0\text{ V} \pm 5\%$ ,  $DV_{\text{dd}} = 3.3\text{ V} \pm 5\%$ ,  $AV_{\text{ss}} = DV_{\text{ss}} = 0\text{ V}$ ; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0 dB = 1 VRMS, 10 K $\Omega$  / 50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0dB settings on all gain stages)

Min and Max performance targets are not included here. Specific system characteristics, such as layout, routing and external CODEC component selection influence the performance of the CODEC. To receive min/max levels for your system, please send us a unit and IDT will perform a full audio test suite and provide you with the results.

Parameter	Min	Typ	Max	Unit
<b>Full Scale Input Voltage:</b>				
All Analog Inputs with out boost	-	1.00	-	Vrms
All Analog Inputs with boost (Note 1)	-	0.03	-	Vrms
<b>Full Scale Output:</b>				
PCM (DAC) to All Analog Outputs	-	1.00	-	Vrms
HEADPHONE_OUT (32 $\Omega$ load) per channel	-	50	-	mWpk
<b>Dynamic Range: -60dB signal level (Note 2)</b>				
PCM to All Analog Outputs	-	99	-	dB
All Analog Inputs to A/D (1 VRMS Input Referenced)	-	88	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
<b>Total Harmonic Distortion + Noise (-3dB): (Note 4)</b>				
PCM to All Analog Outputs	-	-90	-	dB
All Analog Inputs to A/D (-3dBV input Level)	-	-87	-	dB
HEADPHONE_OUT (32 $\Omega$ load)	-	-87	-	dB
HEADPHONE_OUT (10 K $\Omega$ load)	-	-90	-	dB
<b>SNR (idle channel) (Note 5)</b>				
DAC to All Analog Outputs	-	100	-	dB
All Analog Inputs to A/D with High Pass Filter enabled	-	89	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejcn (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to ADC (10 KHz Signal Frequency) Crosstalk	-	-90	-	dB
Any Analog Input to ADC (1 KHz Signal Frequency) Crosstalk	-	-90	-	dB



Parameter	Min	Typ	Max	Unit
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size ANALOG	-	1.5	-	dB
Attenuation, Gain Step Size DIGITAL	-	0.75	-	dB
Input Impedance	-	50	-	KW
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45X AVdd	0.5	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	-	dB
Gain Drift	-	100	-	ppm/°C
DAC Offset Voltage	-	5	10	mV
Deviation from Linear Phase	-	10	1	deg.
All Analog Outputs Load Resistance	-	10	-	KΩ
All Analog Outputs Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	100	-	pF
Mute Attenuation	-	-	-	dB
PLL lock time	-	96	200	μsec
PLL (or HD Audio Bit CLK) 24.576 MHz clock jitter	-	100	300	psec

1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Amplitude of THD+N, measured with A-weighting filter, over 20 Hz to 20 KHz bandwidth.
5. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

#### 2.4. STAC9202 4V Analog Performance Characteristics

If you are interested in using the STAC9202 at 4V Analog, please contact IDT for more information.

#### 2.5. STAC9202 3.3V Analog Performance Characteristics

If you are interested in using the STAC9202 at 3.3V Analog, please contact IDT for more information.

## 2.6. Power Consumption

### 2.6.1. Digital

Table 1. Digital Power Consumption

Power State	Typical	Max	units
D0	20	25	mA
D1	14	17	mA
D2	14	17	mA
D3	14	17	mA

### 2.6.2. 5V Analog

Table 2. 5 V Analog Power Consumption

Power State	Typical	Max	units
D0	30	36	mA
D1	12	26	mA
D2	12	26	mA
D3	11	26	mA

### 3. DETAILED DESCRIPTION

#### 3.1. SPDIF Input

SPDIF\_IN can operate at 44.1 KHz, 48 KHz or 96 KHz and implements internal Jack Sensing. A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to accept consumer SPDIF voltage levels directly eliminates the need for costly external receiver ICs. Advanced features such as record slot select and SPDIF\_IN routing to the DAC allows for simultaneous record and play.

#### 3.2. SPDIF Output

SPDIF\_OUT can operate at 44.1 KHz, 48 KHz, 88.2 KHz and 96 KHz as defined in the Intel High Definition Audio Specification with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

#### 3.3. Digital Microphone Support

The STAC9202 has a three-pin digital microphone interface that accepts high-rate, single-bit data streams from two digital microphones. Each microphone requires only one data line, and both microphones share a single clock line. This robust digital interface gives designers the flexibility to place the microphones in the optimum physical location on a system (such as along the top of the screen bezel) and use a simple, 3-wire ribbon cable to directly connect the microphones to the STAC9202 CODEC.

#### 3.4. Mono Out

The MONO Output is connected to pin 37 and has independent volume and mute control (see the Widget listing for details). The MONO Output derives its input from the output of the summing node that drives PORT A and PORT D. The following analog signals feed the summing amplifier that feeds the MONO Out summing amplifier:

- DAC Output: When enabled, both DAC Outputs are summed together.
- Analog PC BEEP: Source from Pin 12
- ADC Input: Stereo analog feed into the stereo ADC input.

The signals of the stereo channels from the DAC are combined into a single analog signal with a -6dB degradation in signal strength.

#### 3.5. Headphone Drivers Restrictions

It is not recommended that users operate both Port A and Port D as headphone drivers simultaneously. The operation of the two ports as headphone drivers degrades the signal quality of both outputs.<sup>1</sup>

*Note: 1) Headphone capabilities are on Port A (pins 39/41) and Port D (pins 35/36). Do NOT put headphone loads on both sets of pins at the same time.*

### 3.6. Universal Jacks

IDT's Universal Jacks technology allows for flexibility in board design and implementation.

On the STAC9202, only one function can be selected at a time. A set of pins cannot be set as input and output at the same time. However, the selected function can be changed at any time.

For the STAC9202 the Universal Jacks capabilities are as follows

- All of the STAC9202 ports support:
  - Line Out
  - Line In
  - Mic with 0/10/20/30/40<sup>2</sup> dB Mic Boost
- Ports A and D also support:
  - Headphone Out<sup>1</sup>

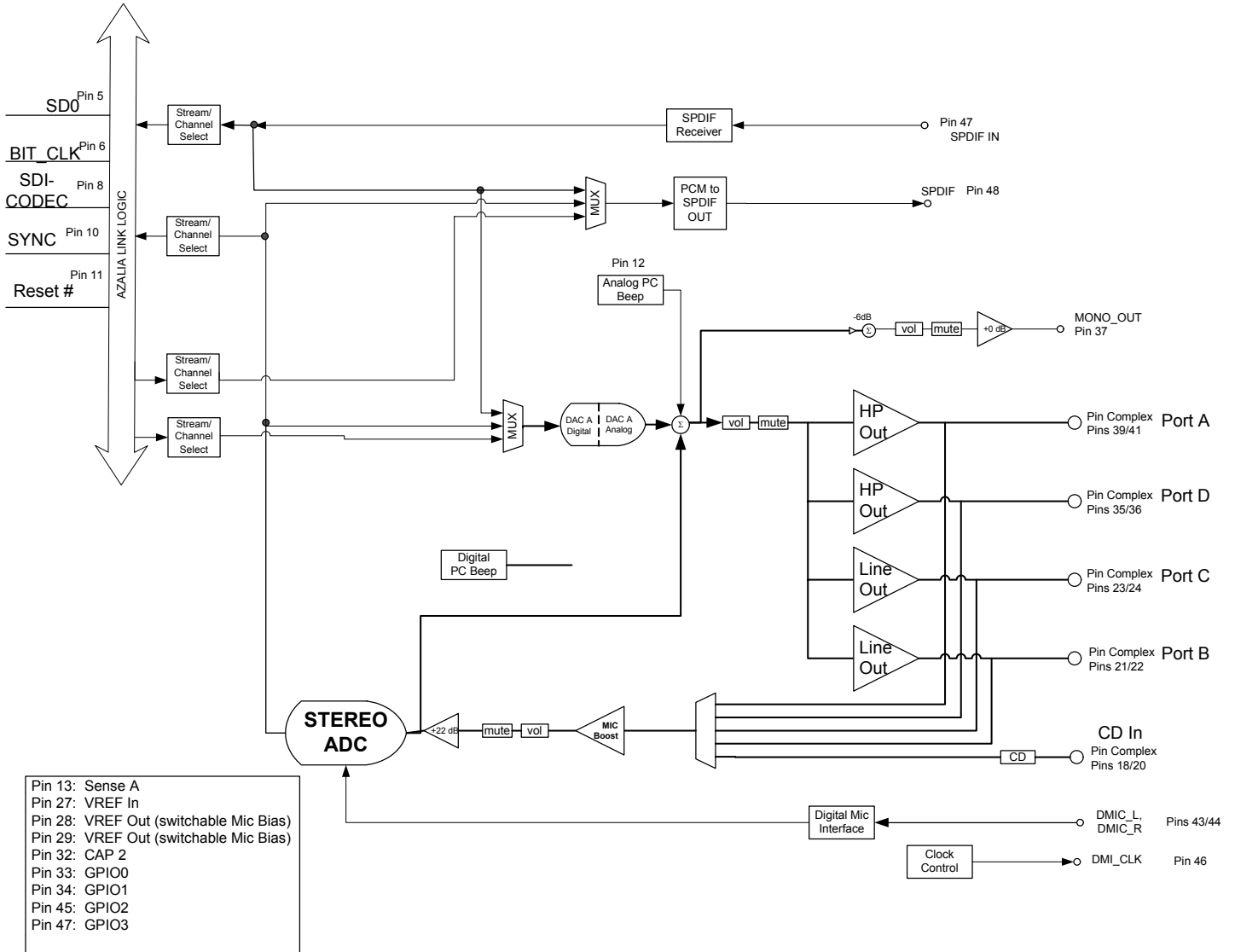
*Note: 1) Headphone capabilities are on Port A (pins 39/41) and Port D (pins 35/36). Do NOT put headphone loads on both sets of pins at the same time.*

*Note: 2) When the 40dB mic boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB MIC boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.*

## 4. FUNCTIONAL BLOCK DIAGRAM

### 4.1. STAC9202

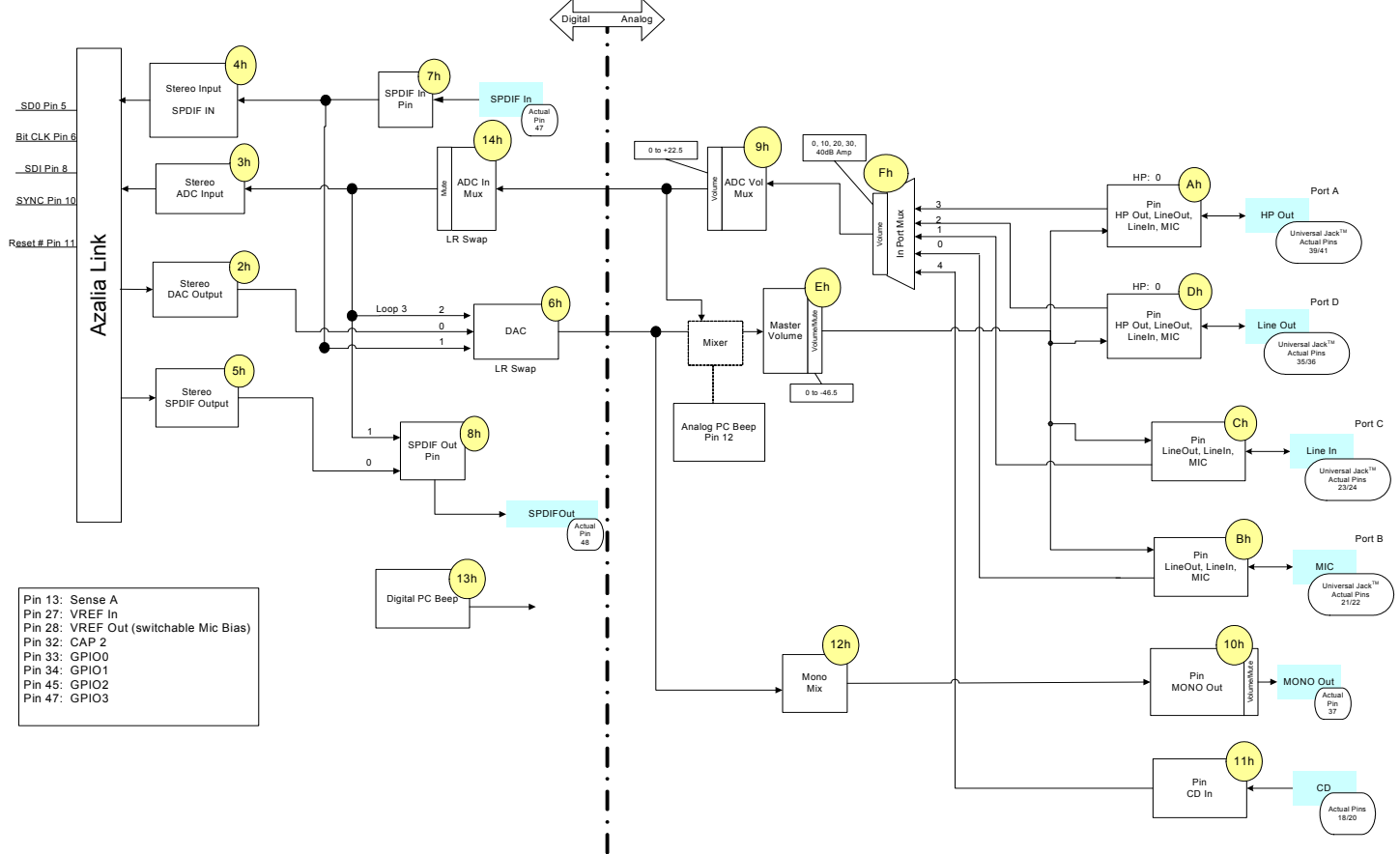
Figure 1. STAC9202 Functional Block Diagram



## 5. WIDGET DIAGRAM

### 5.1. STAC9202 Widget Diagram

Figure 2. STAC9202 Widget Diagram





## 5.2. STAC9202 Widget List

Table 3. High Definition Audio Widget

ID	Widget Name	Description
00h	Root	Root Node
01h	Audio Function Group	Audio Function Group
02h	DAC0	Stereo Output to DAC
03h	ADC0	Stereo Input from ADC
04h	SPDIF_IN	Stereo Input for SPDIF_IN
05h	SPDIF_OUT	Stereo Output for SPDIF_OUT
06h	DAC0Mux	DAC Mux and Boost for outputs for DAC
07h	DigPin1	Pin Widget for SPDIF_IN pin 47
08h	DigPin0	Pin Widget for SPDIF_OUT pin 48
09h	ADC0VolMux	ADC0 Volume
0Eh	MasterVolume	Master Volume Controls
0Fh	InPortMux	Port Mux for ADC0
0Ah	Port A	Port A Pin Widget (Pins 39/41, configurable as HP, Line In, Line Out, Mic)
0Dh	Port D	Port D Pin Widget (Pins 35/36, configurable as HP, Line In, Line Out, Mic)
0Ch	Port C	Port C Pin Widget (Pins 23/24, configurable as Line Out, Mic)
0Bh	Port B	Port B Pin Widget (Pins 21/22, configurable as Line Out, Mic)
10h	MonoOut	Mono Output from DAC
11h	CD	CD Pin Widget pins 18/19/20
12h	MonoOutMix	Mixer for Mono Output
13h	Digital PC Beep	Digital PC Beep
14h	ADC0InMux	Input Mux for ADC converter
15h	DigMicPin	Pin Widget for Digital Microphone (Pins 43/44/46 configurable as a Mic)

### 5.3. Root Node (NID = 0x00)

#### 5.3.1. Root PnpID\_

Table 4. Root PnpID Command Verb Format

	Verb ID	Payload	Response
Get	F00	00	See bitfield table

Table 5. Root PnpID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:16]	Vendor	R	0x8384	Vendor ID = 8384h
[15:0]	Device	R	0x7630	Device ID for: STAC9202 = 7632

#### 5.3.2. Root RevID

Table 6. Root RevID Command Verb Format

	Verb ID	Payload	Response
Get	F00	02	See bitfield table

Table 7. Root RevID Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd	R	0x00	Reserved
[23:20]	Major	R	0x1	Major rev number of compliant HD Audio specification
[19:16]	Minor	R	0x0	Minor rev number of compliant HD Audio specification
[15:8]	Vendor	R	0x01	Vendor rev number for this device ID
[7:0]	Stepping	R	0x01	Vendor stepping number within the given Vendor RevID

### 5.3.3. Root NodeInfo

Table 8. Root NodeInfo Command Verb Format

	Verb ID	Payload	Response
<b>Get</b>	F00	04	See bitfield table

Table 9. Root NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x00	Reserved
[23:16]	StartNID	R	0x01	Starting node number (NID) of first function group
[15:8]	Rsvd1	R	0x00	Reserved
[7:0]	TotalNodes	R	0x01	Total number of nodes

## 5.4. AFG Node (NID = 0x01)

### 5.4.1. AFG Reset

Table 10. AFG Reset Command Verb Format

	Verb ID	Payload	Response
<b>Get</b>	7FF	00	See bitfield table
<b>Set1</b>	7FF	See bits [7:0] of bitfield table	0000_0000h

Table 11. AFG Reset Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:0]	Response	R	0x0	Reserved. Overlaps Execute.
[0]	Execute	W	0x0	Function Reset. Function Group reset is executed when the Set verb 7FF is written with 8-bit payload of 00h. The CODEC should issue a response to acknowledge receipt of the verb, and then reset the affected Function Group and all associated widgets to their power-on reset values. Some controls such as Configuration Default controls should not be reset. Overlaps Response.

#### 5.4.2. AFG NodeInfo

Table 12. AFG NodeInfo Command Verb Format

	Verb ID	Payload	Response
Get	F00	04	See bitfield table

Table 13. AFG NodeInfo Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:24]	Rsvd2	R	0x0	Reserved
[23:16]	StartNID	R	0x02	Starting node number for function group subordinate nodes.
[15:8]	Rsvd1	R	0x0	Reserved
[7:0]	TotalNodes	R	0x14	Total number of nodes. 14h = STAC9202

### 5.4.3. AFG Type

Table 14. AFG Type Command Verb Format

	Verb ID	Payload	Response
Get	F00	05	See bitfield table

Table 15. AFG Type Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:9]	Rsvd	R	0x0	Reserved
[8]	Unsol	R	0x1	This node is capable of generating an unsolicited response, and will respond to the Unsolicited Response verb (Verb ID 708h).
[7:0]	NodeType	R	0x01	Node type = Audio Function Group

### 5.4.4. AFG GrpCap

Table 16. AFG GrpCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	08	See bitfield table

Table 17. AFG GrpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:17]	Rsvd3	R	0x0	Reserved
[16]	BeepGen	R	0x1	Optional Beep Generator is present
[15:12]	Rsvd2	R	0x0	Reserved
[11:8]	InputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the HD Audio link.

Table 17. AFG GrpCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[7:4]	Rsvd1	R	0x0	Reserved
[3:0]	OutputDelay	R	0xD	Typical latency = 13 frames. Number of samples between when the signal is received from the HD Audio link and when it appears as an analog signal at the pin.

#### 5.4.5. AFG FrmtCap

Table 18. AFG FrmtCap Command Verb Format

	Verb ID	Payload	Response
Get	F00	0A	See bitfield table

Table 19. AFG FrmtCap Command Response Format

Bit	Bitfield Name	RW	Reset	Description
[31:21]	Rsvd2	R	0x0	Reserved
[20]	B32	R	0x0	32 bit audio formats are NOT supported
[19]	B24	R	0x1	24 bit audio formats are supported
[18]	B20	R	0x1	20 bit audio formats are supported
[17]	B16	R	0x1	16 bit audio formats are supported
[16]	B8	R	0x0	8 bit audio formats are NOT supported
[15:12]	Rsvd1	R	0x0	Reserved
[11]	R12	R	0x0	384 KHz rate (8/1*48 KHz) NOT supported
[10]	R11	R	0x1	192.0 KHz rate (4/1*48 KHz) supported
[9]	R10	R	0x1	176.4 KHz rate (4/1*44.1 KHz) supported
[8]	R9	R	0x1	96.0 KHz rate (2/1*48 KHz) supported
[7]	R8	R	0x1	88.2 KHz rate (2/1*44.1 KHz) supported