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4-CHANNEL HD AUDIO CODEC WITH QUAD DIGITAL MICROPHONE INTERFACE

STAC9204/9205

Description

The STAC9204/9205 are high fidelity, 4-channel HD Audio CODECs that enable 2.0 Audio with simultaneous Real-Time Communication such as VoIP, conferencing, voice command and control, etc. Up to four digital microphones are supported, enabling high quality voice input for increased usability of voice applications.

Features

- High performance SD technology
  - 103dB DAC SNR
  - 90dB ADC SNR
- Two stereo DACs and two stereo ADCs
  - Supports 2.0 Audio with simultaneous Real-Time Communication (RTC) channel such as VoIP or separate stereo audio stream
  - Provides mono output for laptop sub-woofer
- 24-bit resolution with up to 192 KHz sample rates
- Supports advanced chipsets with flexible 1.5 V to 3.3 V signaling
- Digital microphone interface
  - Direct interface to up to four digital microphones
- Analog stereo microphone
  - Microphone Boost 0, 10, 20, 30, 40dB
  - Five adjustable Vref outputs for microphone bias
- Universal Jacks™ functionality for jack retasking
- S/PDIF In and Out
- Two-pin volume up/down control
- Digital PC Beep to all outputs
- +3.3 V, +4 V, +4.5 V and +5 V analog power supply options
- Optimized and flexible power management
- 48-pin LQFP and 48-pad QFN environmental package

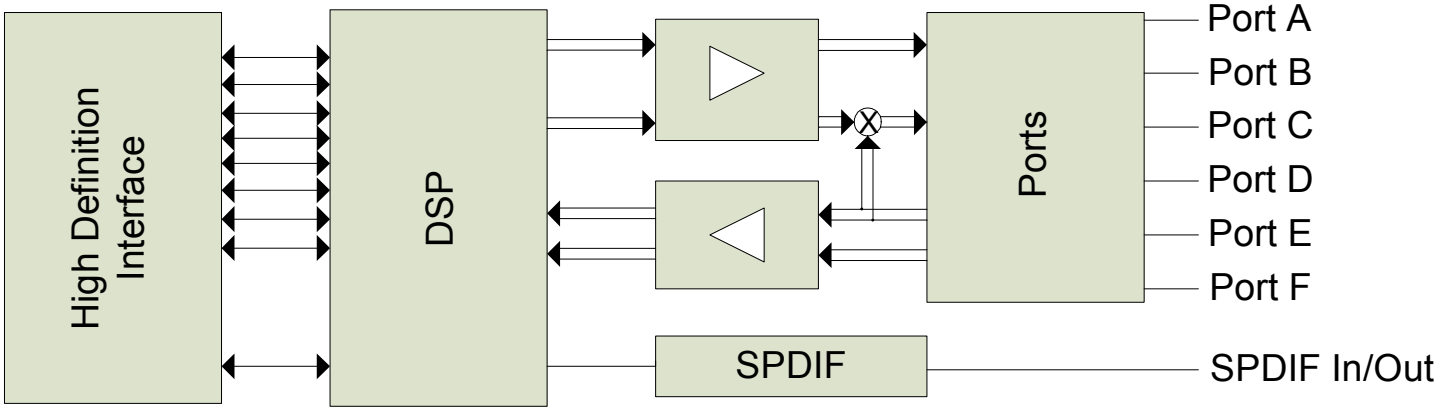
Software Support

- SKPI (Kernel Processing Interface)
  - Enables plug-ins that can operate globally on all audio streams of the system
- 12 band parametric equalizer SKPI plug-in
  - Constant, system-level effects tuned to optimize a particular platform can be combined with user-mode “presets” tailored for specific acoustical environments and applications
  - System-level effects automatically disabled when external audio connections made
- Dynamics Processing SKPI plug-in
  - Enables improved voice articulation
  - Compressor/limiter allows higher average noise level without resonances

Third Party Partners

- Dolby PC Entertainment Experience Logo Program
  - Dolby Home Theater™ (HT)
  - Dolby Sound Room™ (SR)
- Dolby Technologies
  - Dolby Headphone™, Dolby Virtual Speaker™
  - Dolby ProLogic II™, Dolby ProLogic IIx™
  - Dolby Digital Live™ (DDL)
- Intel Audio Studio™ from Sonic Focus
- Maxx Player™ from Waves
- Microphone Beam Forming, Acoustic Echo Cancellation, and Noise Suppression from Knowles™

Block Diagram



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1. DESCRIPTION

1.1. Overview

The STAC9204/9205 are high fidelity, 4-channel HD Audio CODECs that enable 2.0 Audio with simultaneous real-time communication such as VoIP, conferencing, voice command and control, etc. Up to four digital microphones are supported enabling high quality voice input for increased usability of voice applications.

The STAC9204/9205 incorporate IDT's proprietary SD technology to achieve a DAC SNR in excess of 100dB. The higher performance and quality of IDT's audio solutions brings consumer electronics level performance to the notebook, desktop and media center PC.

The STAC9204/9205 provide stereo, 24-bit, full duplex resolution, supporting sample rates up to 192 KHz by the DAC and ADC. The STAC9204/9205 SPDIF In/Out supports sample rates of 96 KHz, 48 KHz and 44.1 KHz plus SPDIF OUT supports 88.2 KHz and 192 KHz. Additional sample rates are supported by the driver software.

The STAC9204/9205 support all desired four channel configurations, including switchable Headphone (HP) Out and Universal Jacks™ functionality for jack detection and re-tasking. The SPDIF interface provides connectivity to consumer electronic equipment like Dolby Digital decoders, powered speakers and mini-disk drives, or to a home entertainment system. All analog I/O pairs support LINE_IN, LINE_OUT and MIC. (Port D only supports fixed-function microphone.)

MIC inputs can be programmed with 0/10/20/30/40dB boost. For more advanced configurations, the STAC9204/9205 have five General Purpose I/O (GPIO) pins. The STAC9204/9205 also provide single ended CD input for compatibility with DRM solutions and to support legacy OS issues.

The STAC9204/9205 integrate two headphone amplifiers which are available on Ports A and D. The headphone amplifiers are dedicated to these two outputs for increased flexibility, enhanced user experience, and reduced implementation costs.

The Universal Jack capabilities allow the CODECs to detect when audio devices are connected, and allow the CODECs to be reconfigured to support these devices regardless of which port they are connected to. SPDIF input sensing is also supported. The fully parametric IDT SoftEQ can be initiated upon headphone jack insertion and removal for protection of notebook speakers.

The STAC9204/9205 operate with a 3.3 V digital supply and either 3.3 V, 4 V, 4.5 V or 5 V analog supply. They also support 1.5 V and 3.3 V HDA signaling; the correct voltage is selected dynamically based on the value of the appropriate pin.

The STAC9204/9205 are available in a 48-pin LQFP or a 48-pad QFN Environmental (ROHS) package.

1.2. Block Diagram

Figure 1. STAC9204/9205 / STAC9204D/9205D Block Diagram

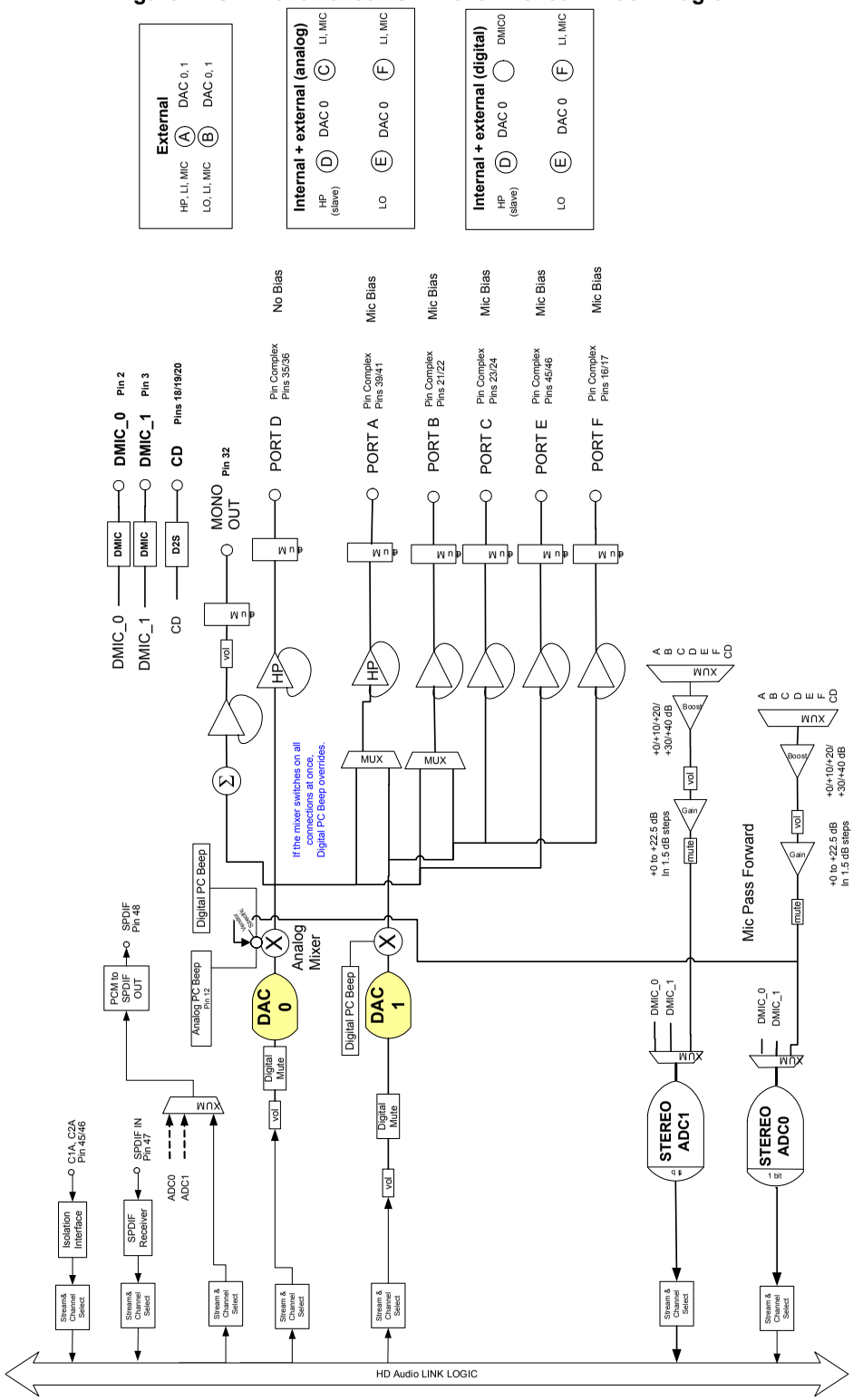
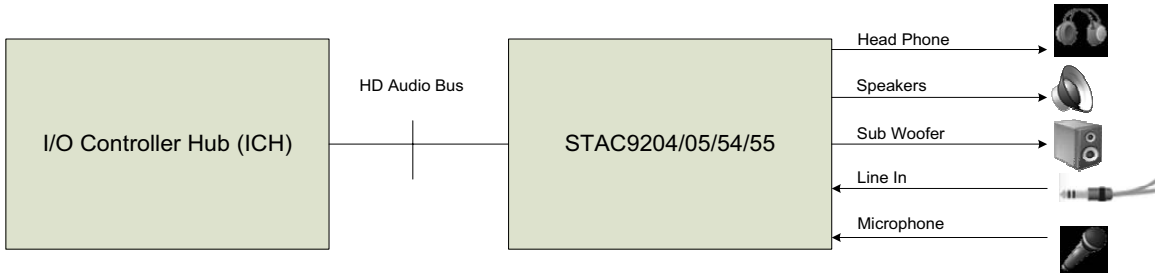


Figure 2. System Diagram



1.3. Detailed Description

1.3.1. Low-voltage High Definition Audio Link Signaling

The STAC9204/9205 are compatible with either 1.5 V or 3.3 V High Definition Audio Link signaling; the voltage selection is performed dynamically based on the input voltage of DVDD_IO. Note that DVDD_IO is not a logic configuration pin but provides the digital power supply to be used for the High Definition Audio Link signals.

When in 1.5 V mode, the STAC9204/9205 can correctly decode BITCLK, SYNC, RESET# and SDO because they operate at 1.5 V. Additionally, it will drive SDI_CODEC at 1.5 V. None of the GPIOs are affected, as they always function at their nominal voltage (DVDD or AVDD).

1.3.2. Digital Microphone Support

The digital microphone interface permits connection of digital microphones to the STAC9205 via the DMIC0, DMIC1, and DMIC_CLK three-pin interface. The DMIC0 and DMIC1 pins carry either 1 or 2 channels of digital microphone data to the STAC9205. In the event that a single microphone is used, the data is routed to both ADC channels.

The DMIC_CLK output is programmable from 1.176 MHz to 4.704 MHz in 1.176 MHz increments and is synchronous to the 24 MHz internal clock. The default frequency is 2.352 MHz.

The STAC9205 supports the digital microphone configurations listed in Table 1.

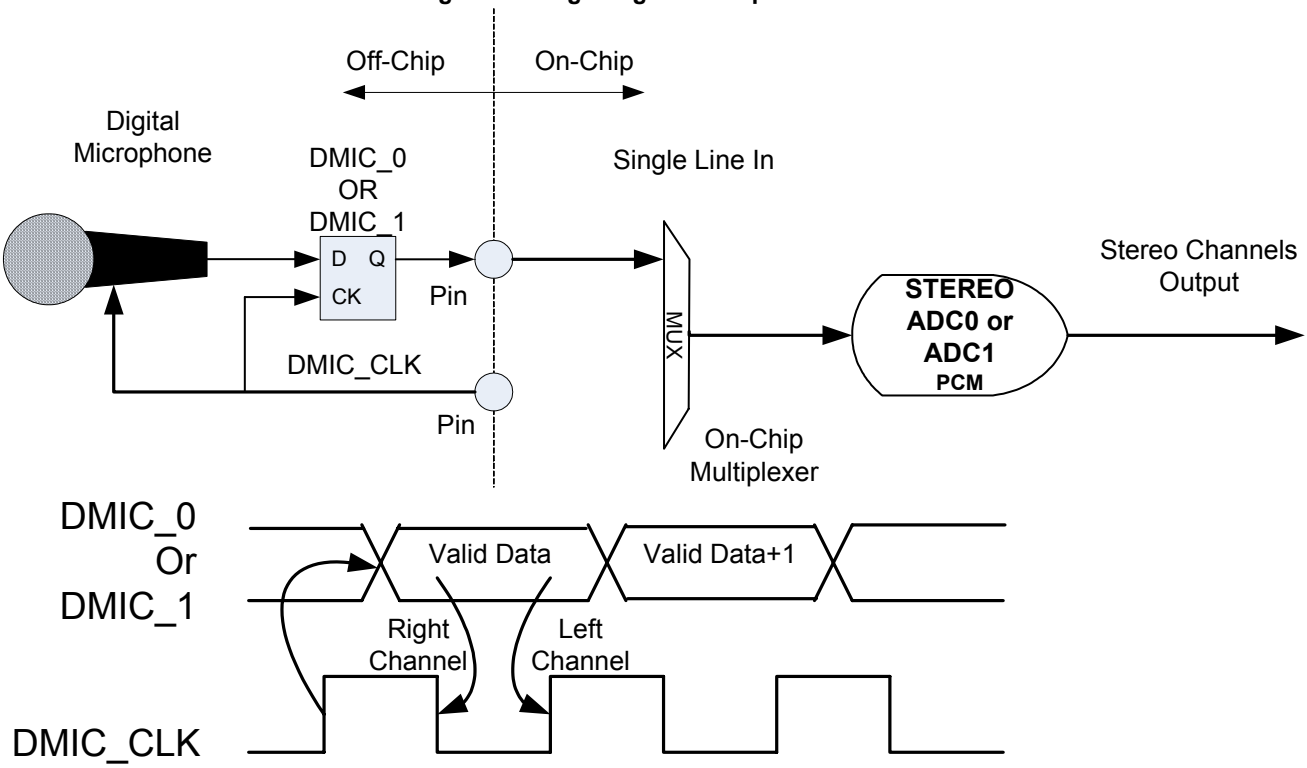
Table 1. STAC9205 Valid Digital Microphone Configurations

Digital Mics	Data Sample	ADC Conn.	Notes
0	N/A	N/A	No Digital Microphones
1	Single Edge (see Figure 3)	0 or 1	Available on either DMIC_0 or DMIC_1 Both ADC Channels process data, may be in-phase or out-of-phase by 1/2 DMIC_CLK period depending upon external configuration and timing
2	Double Edge on either DMIC_0 or 1 (see Figure 4) *OR* Single Edge on DMIC_0 and 1	0 or 1	Available on either DMIC_0 or DMIC_1 External logic required to support sampling on a single Digital Microphone pin channel on rising edge and second Digital Microphone right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. If both DMIC_0 and DMIC_1 are used to support 2 digital microphones, 2 separate ADC units will be used, however, this configuration is not recommended since it consumes two stereo ADC resources.
3	Double Edge on one DMIC pin and Single Edge on the second DMIC pin.	0 or 1	Requires both DMIC_0 or DMIC_1 External logic required to support sampling on a single Digital Microphone pin channel on rising edge and second Digital Microphone right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration
4	Double Edge (see Figure 5)	0 or 1	Connected to DMIC_0 and DMIC_1 External logic required to support sampling on a single Digital Microphone pin channel on rising edge and second Digital Microphone right channel on falling edge of DMIC_CLK for those digital microphones that don't support alternative clock edge capability. Two ADC units are required to support this configuration

Table 2. DMIC_CLK, DMIC_0 and DMIC_1 Operation During Power States

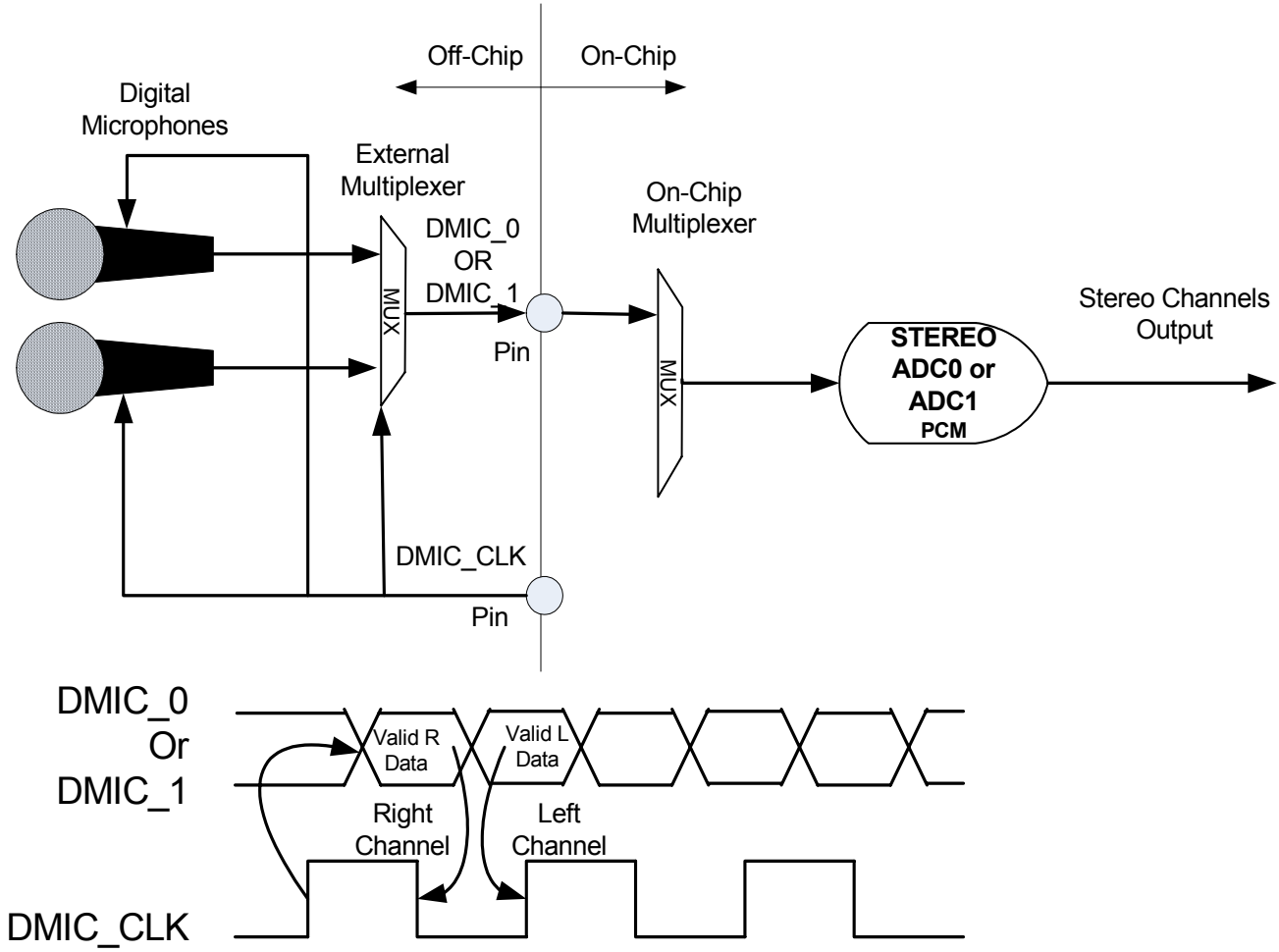
Power State	DMIC Widget Enabled?	DMIC_CLK Output	DMIC_0,1	Notes
D0	Yes	Clock Capable	Input Capable	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 input widget is enabled. Otherwise, the DMIC_CLK remains low.
D1	Yes	Clock Disabled	Input Disabled	DMIC_CLK Output is Enabled when either DMIC_0 or DMIC_1 input widget is enabled. Otherwise, the DMIC_CLK remains low.
D2	Yes	Clock Disabled	Input Disabled	DMIC_CLK remains low
D3	Yes	Clock Disabled	Input Disabled	DMIC_CLK remains low
D0-D3	No	Clock Disabled	Input Disabled	DMIC_CLK is HIGH-Z with weak pull-down

Figure 3. Single Digital Microphone



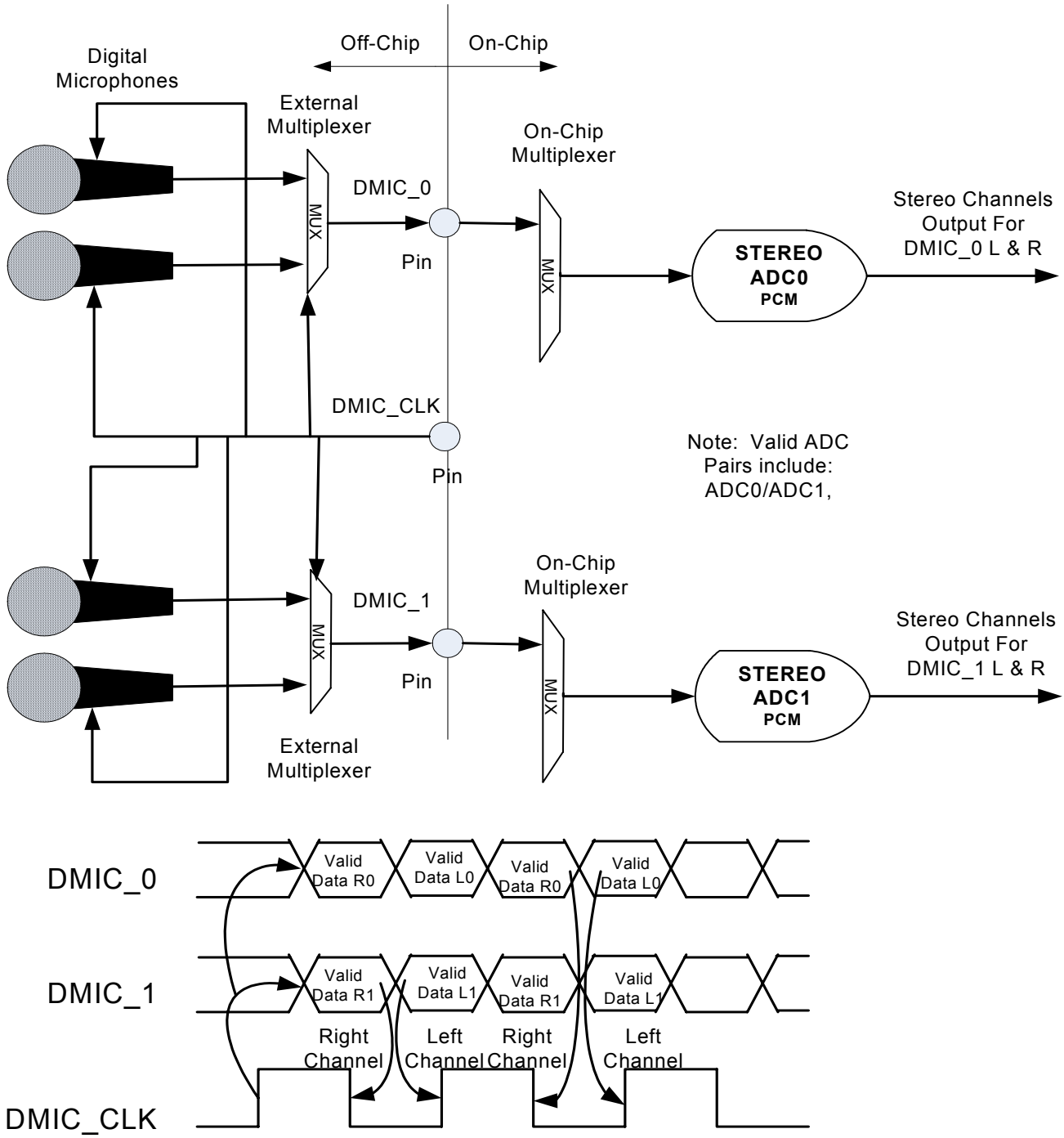
Note: Data is ported to both left and right channels.

Figure 4. Stereo Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore the external mux may not be required.

Figure 5. Quad Digital Microphone Configuration



Note: Some Digital Microphone Implementations support data on either edge, therefore the external mux may not be required

1.3.3. Volume/Digital Microphone/GPIO Selection

For the STAC9205, three functions are available on pins 2 and 3. To determine which function is actually enabled on these pins, the order of precedence is followed:

1. If the GPIOs are enabled through the Audio Function Group, they override both Volume Control and Digital Microphones.
2. If the GPIOs are not enabled through the Audio Function Group, then, at reset, the Volume control is enabled with a weak pull-up.
3. If BIOS or other software application enables either Digital Microphone input through the Configuration Default Register, the Volume is disconnected and the pull-ups are disconnected, with the weak pull-downs enabled.

For STAC9204, Digital Microphones are not available, but the other two functions operate with the same order of precedence.

1.3.4. VRefOut/GPIO Selection

Two functions are available on pins 30 and 31. To determine which function is enabled on the two pins, the order of precedence followed is:

1. If the GPIOs are enabled, they override VRefOut-E or VRefOut-F.
2. If the GPIOs are not activated through the Audio Function Group, then, at reset, the VRefOut pins are enabled.

If using the GPIOs as inputs, incorporate 10 KW external pull-ups or the GPI will not function correctly.

1.3.5. SPDIF Input

SPDIF IN can operate at 44.1 KHz, 48 KHz or 96 KHz, and implements internal Jack Sensing.

A sophisticated digital PLL allows automatic rate detection and accurate data recovery. The ability to directly accept consumer SPDIF voltage levels eliminates the need for costly external receiver ICs. Advanced features such as record-slot-select and SPDIF_IN routing to the DAC allow for simultaneous record and play.

1.3.6. SPDIF Output

SPDIF Output supports 44.1 KHz, 48 KHz, 88.2 KHz, 96 KHz and 192 KHz sample rates, as defined in the Intel High Definition Audio Specification, with resolutions up to 24 bits. This insures compatibility with all consumer audio gear and allows for convenient integration into home theater systems and media center PCs.

1.3.7. Mono Output

MONO Output is supported on pin 32 and has an independent mute and volume control. The MONO Output derives input from the output of the summing node after DAC0. The following analog signals feed the summing amplifier that feeds the MONO Output summing amplifier:

- DAC0 Output: When enabled, both DAC0 Outputs are summed together.
- Analog PC Beep: Sourced from pin 12.
- ADC Input: Stereo analog feed into the stereo ADC input.
- The combination of the stereo channels from DAC0 are combined into a single analog signal with a -6dB degradation in signal strength.

Note: MONO Output only works with the IDT Driver.

1.3.8. Universal Jacks™

The Universal Jacks™ technology allows for the greatest flexibility in board design and implementation.

For the STAC9204/9205 the Universal Jacks™ capabilities are as follows[1]:

- Ports A and D[2] support[3]:
  - Headphone Out
  - Line Out
  - Line In
  - Microphone, with 0/10/20/30/40 dB Microphone boost[4]
- Ports B, C, E, and F support[3]:
  - Line Out
  - Line In
  - Microphone, with 0/10/20/30/40 dB Microphone boost[4]
- Mono Output cannot be reconfigured

Note: 1) On the STAC9204/9205, only one function can be selected on each pin pair at a time. For example, a pin pair cannot be configured as an input and output at the same time. Configuration can be changed at any time.

Note: 2) Port D does not provide a microphone bias pin. Therefore only an internal, fixed-function microphone can be supported.

Note: 3) Headphone capabilities are provided on Ports A and D, however, audio performance degrades when 2 headphones are enabled.

Note: 4) When the 40dB microphone boost feature is enabled, additional gain increases greater than 6dB may result in significant audio quality degradation of the microphone audio input. In particular, when the 40dB microphone boost is active, the SNR, THD+N and DC offset will significantly degrade regardless of the input signal level.

1.3.8.1. Jack Detect

SENSE_A pin is used to detect the presence of plugs in ports A, B, C, and D. SENSE_B pin is used to detect the presence of plugs in ports E and F. Refer to the STAC9204/9205 reference design for port detect circuitry.

For different analog supply voltages, Table 3 summarizes what ports can be detected and the resistor tolerance needed.

Table 3. Jack Detect

AVdd Nominal Voltage (+/- 5%)	Resistor Tolerance Sense A (If port D is used)	Resistor Tolerance Sense A (If port D is not used)	Resistor Tolerance Sense B (For ports E and F)
5 V	1%	1%	1%
4.5 V	1%	1%	1%
4 V	0.50%	1%	1%
3.3 V	0.10%	1%	1%

Includes pull-up resistors on Sense A/B and series resistors between jack switch and Sense A/B. See the reference design for more information on Jack Detect implementation.

1.3.8.2. Impedance Sense

Impedance Sensing is accomplished by on-chip circuitry that tests the impedance at the pin of the chip and compares it to internal reference impedance. Table 4 describes the bin information and the codes that are returned when the Pin Widget Impedance field in the Port Pin Sense widget is read. Please note that even under the best conditions, there is no method to guarantee 100% impedance sensing due to variations in external circuitry and impedance overlap of devices that can be plugged into a jack. The impedance sense table reflects both standard Line Out and Headphone output drivers.

Table 4. Impedance Sense

Bins	Return Hex Code	Measured Impedance Level	General Device Detected
000b	0064h	Impedance < 300 Ω	Passive Speakers, Headset Speakers
001b	012Ch	Impedance = 300 Ω +/- 25%	Some Headset Speakers
010b	028Ah	300 Ω > Impedance < 1275 Ω	Some Microphones
011b	03E8h	Impedance = 1275 Ω +/- 25%	Microphones
100b	07D0h	1275 Ω > Impedance < 2000 Ω	Microphones
101b	0BB8h	Impedance = 2000 Ω +/- 25%	Amplified Speakers
110b	2710h	> 2000 Ω	Amplified Speakers, Line In
111b	2710h	> 2000 Ω	Amplified Speakers, Line In

1.3.9. Power Management

Table 5 describes the active functionality in each power state.

Table 5. Power Management

Function	D0-D1	D2	D3-default	D3-alternate
DAC	On	Off	Off	Off
ADC	On	Off	Off	Off
Ports	On	On	Off	Off
Headphone (HP) Amps	On	On	Off[1]	Off
VrefOut	On	On	Off	Off
Port Sense	On	On	On[2]	Programmable
AZ-Link	On	On	On[3]	Programmable[4]
VAG	On	On	On[5]	Programmable
Differential Amplifiers	On	On	Off	Off

1. VAG is kept active when amplifiers are turned off.
2. If BITCLK is not active, a wake event must be generated. Otherwise an unsolicited response is sent.
3. Not active if BITCLK is not running.
4. This mode can only be exited with a Bus Reset.
5. VAG is always ramped up and down gradually, except in the case of a sudden power removal.

The D3-default state is available for HD Audio compliance. The programmable values exposed via vendor-specific settings are under the IDT Device Driver control for further power reduction.

The default power state for the Audio Function Group after reset is D3-default.

1.3.10. Analog PC-Beep

PC Beep may need to be active on power up, in which case the BIOS is responsible for enabling it by setting AnalogBeepEn in the AFG AnaCtrl widget. The PC_BEEP input is routed directly to the MONO_OUT, LINE_OUT and HP_OUT pins of the CODEC. Because the PC_BEEP input drive is often a full scale digital signal, some resistive attenuation of the PC_BEEP input is recommended to keep the beep tone within reasonable volume levels. The user should mute this input before using any other mixer input because the PC Beep input can contribute noise to the lineout during normal operation.

Analog PC-Beep is not supported during Link Reset.

1.3.11. Headphone Drivers

Performance degradation will occur when using two headphones simultaneously. See the electrical specifications for details.

1.3.12. Device IDs

Table 6. Device IDs

Part Number	DAC SNR	DAC	ADC	Digital Mics	Dolby	VID	DID
STAC9205X	103dB	4	4	Yes	No	8384h	76A0h
STAC9205D	103dB	4	4	Yes	Yes-HT/SR	8384h	76A1h
STAC9204X	103dB	4	4	No	No	8384h	76A2h
STAC9204D	103dB	4	4	No	Yes-HT/SR	8384h	76A3h

Note: HT/SR refers to Dolby Home Theater (HT) and Sound Room (SR), logos of the Dolby PC Entertainment Experience Logo program.

2. CHARACTERISTICS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9204/9205. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0 ^{o}C to +70 ^{o}C
Storage temperature		-55 ^{o}C to +125 ^{o}C
Soldering temperature		Soldering temperature information for all available packages begins on page 189.

2.1.2. Recommended Operating Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
(Note: With Supply Override Enable Bit set to force 5 V operation.)	Analog - 4 V	3.8	4	4.2	V
	Analog - 4.5 V	4.275	4.5	4.725	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C
	T_{case} (48-QFN)			+95	°C

ESD: The STAC9204/9205 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9204/9205 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.2. STAC9204/9205 5.0V, 4.5V, 4.0V, and 3.3V Analog Performance Characteristics

(Tambient = 25 ºC, AVdd = Supply ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 kHz input sine wave; Sample Frequency = 48 kHz; 0 dB = 1 VRMS, 10KW//50pF load, Testbench Characterization BW: 20 Hz – 20 kHz, 0 dB settings on all gain stages)

Table 7. Performance Characteristics

Parameter	Conditions	AVdd	Min	Typ	Max	Unit
Digital to Analog Converters						
Resolution		All		24		Bits
SNR - DAC to All Line-Out Ports (Note 4)	PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		103 101 100 98		dB
THD+N - DAC to All Line-Out Ports	-3dB Signal, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		87 85 84 82		dB
SNR - DAC to All Headphone Ports (Note 4)	10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		103 101 100 98		dB
THD+N - DAC to All Headphone Ports (Note 3)	-3dB Signal, 10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		85 83 82 80		dB
SNR - DAC to All Headphone Ports with 2 Headphone Outputs Operating (Note 4)	10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		100 98 97 95		dB
THD+N - DAC to All Headphone Ports with 2 Headphone Outputs Operating (Note 3)	-3dB Signal, 10KΩ load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		82 80 79 77		dB
SNR - DAC to All Headphone Ports (Note 4)	32Ω load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		103 101 100 98		dB
THD+N - DAC to All Headphone Ports (Note 3)	-3dB Signal, 32Ω load, PCM data, (Note 9)	5V 4.5V 4.0V 3.3V		80 80 78 76		dB
Any Analog Input to DAC Crosstalk	10KHz Signal Frequency	All	-	-80	-	dB
Any Analog Input to DAC Crosstalk	1KHz Signal Frequency	All	-	-85	-	dB
Gain Error	(Note 9)	All			0.5	dB
Interchannel Gain Mismatch	(Note 9)	All			0.5	dB