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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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AC'97 2.3 CODECS WITH STEREO MICROPHONE & UNIVERSAL JACK

STAC9752A/9753A

FEATURES

- **High Performance ΣΔ Technology**
- **AC'97 Rev 2.3 Complaint**
- **20-bit Full Duplex Stereo ADC & DACs**
- **Independent Sample Rates for ADC & DACs**
- **5-Wire AC-Link Protocol Compliance**
- **20-Bit SPDIF Output**
- **Universal Jacks™**
- **Full Stereo Microphone Pre-Amp**
- **Internal Jack Sensing on Headphone & Line_Out**
- **Internal Microphone Input Sensing**
- **Digital PC Beep Option**
- **Extended AC'97 2.3 Paging Registers**
- **General Purpose I/Os and Crystal Elimination Circuit**
- **Headphone Drive Capability (50 mW per channel)**
- **Switchable Headphone Out (pins 39/41 or 35/36)**
- **0dB, 10dB, 20dB and 30dB Microphone Boost Capability**
- **+3.3 V (STAC9753A) and +5 V (STAC9752A) Analog Power Supply Options**
- **Pin Compatible with STAC9750/52/66**

KEY SPECIFICATIONS

- **Analog LINE_OUT SNR: 94dB**
- **Digital DAC SNR: 92dB**
- **Digital ADC SNR: 85dB**
- **Full-scale Total Harmonic Distortion: 0.002%**
- **Crosstalk Between Input Channels: -70dB**
- **Spurious Tone Rejection: 100dB**
- **Stereo Microphone Input**

RELATED MATERIALS

- **Data Sheet**
- **Reference Designs**

DESCRIPTION

IDT's STAC9752A/9753A are general purpose 20-bit, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio CODEC 97 Component Specification Rev. 2.3). The STAC9752A/9753A incorporates IDT's proprietary ΣΔ technology.

The AC'97 CODEC is designed to achieve a DAC SNR in excess of 94dB. The DACs, ADCs, and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel.

The STAC9752A/9753A includes digital input/output capability for support of modern PC systems, with an output that supports the SPDIF format. The STAC9752A/9753A is a standard 2-channel stereo CODEC. With IDT's headphone drive capability, headphones can be driven with without an external amplifier.

The STAC9752A/9753A may be used as a secondary CODEC, with the STAC9700/21/56/08/84/50/52 as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.3 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications.

The STAC9752A/9753A communicates via the five-wire AC-Link to any digital component of AC'97, providing flexibility in the audio system design.

Packaged in an AC'97 compliant 48-pin TQFP, the STAC9752A/9753A can be placed on a motherboard, daughter boards, PCI, AMR, CNR, MDC or ACR cards.

The STAC9752A/9753A provides variable sample rate Digital-to-Analog (DA) and Analog-to-Digital (AD) conversion, mixing, and analog processing.

Supported audio sample rates include 48KHz, 44.1KHz, 32KHz, 22.05KHz, 16KHz, 11.025KHz, and 8 KHz; additional rates are supported in the STAC9752A/9753A soft audio drivers. All ADCs and DACs operate at 20-bit resolu-

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1. PRODUCT BRIEF

1.1. Features

- High performance ΣΔ technology
- AC'97 Rev 2.3 Complaint, 20-bit, full duplex stereo ADCs & DACs
- Independent sample rates for ADCs & DACs
- 5-Wire AC-Link protocol compliance
- 20-Bit SPDIF Output
- Universal Jacks™
- Full Stereo Microphone Pre-Amp
- Internal Jack Sensing on Headphone & Line_Out
- Internal Microphone Input Sensing
- Digital PC Beep Option
- Extended AC'97 2.3 Paging Registers
- Digital-ready status
- General purpose I/Os
- Crystal Elimination Circuit
- Headphone drive capability (50 mW per channel)
- Switchable Headphone Out (pins 39/41 or 35/36)
- 0, 10db, 20db, and 30 dB microphone boost capability
- +3.3 V (STAC9753A) and +5 V (STAC9752A) analog power supply options
- Pin compatible with STAC9700/21/56
- 100% compatible with STAC9750/52/66
- IDT Surround (SS3D) Stereo Enhancement
- Energy saving dynamic power modes
- Multi-CODEC option (Intel AC'97 rev 2.3)
- 94dB SNR LINE-LINE

1.2. Description

IDT's STAC9752A/9753A are general purpose 20-bit, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio Codec 97 Component Specification Rev. 2.3). The STAC9752A/9753A incorporates IDT's proprietary ΣΔ technology to achieve a DAC SNR in excess of 92dB. The DACs, ADCs and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel.

The STAC9752A/9753A include digital output capability for support of modern PC systems with an output that supports the SPDIF format.

The STAC9752A/9753A are standard 2-channel stereo CODEC. With IDT's headphone drive capability, headphones can be driven without an external amplifier.

The STAC9700/21/44/56/08/84/50/66 may be used as a secondary or tertiary CODEC, with the STAC9752A/9753A as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.3 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications.

The STAC9752A/9753A communicates via the five wire AC-Link to any digital component of AC'97, providing flexibility in the audio system design.

Packaged in an AC'97 compliant 48-pin LQFP or in the 32-pad/pin QFN, the STAC9752A/9753A can be placed on motherboards, daughter boards, PCI, AMR, CNR, MDC or ACR cards.

The STAC9752A/9753A block diagram is illustrated in Figure 1.

The STAC9752A/9753A provides variable sample rate Digital-to-Analog (DA) and Analog-to-Digital (AD) conversion, mixing, and analog processing. Supported audio sample rates include 48KHz, 44.1KHz, 32KHz, 22.05KHz, 16KHz, 11.025KHz, and 8KHz; additional rates are supported in the STAC9752A/9753A soft audio drivers All ADC's and DAC's operate at 20-bit resolution.

Two 20-Bit DACs convert the digital stereo PCM_OUT content to audio. The MIXER block combines the PCM_OUT with any analog sources to drive the LINE_OUT and HP_OUT outputs. The MONO_OUT delivers either mic only, or a mono mix of sources from the MIXER. The stereo, variable-sample-rate, 20-bit ADCs provide record capability for any mix of mono or stereo sources, and deliver a digital stereo PCM-in signal back to the AC-Link. The microphone input in mono mode and the mono mix input can be recorded simultaneously, thus allowing for an all digital output in support of the digital-ready initiative. For a digital-ready record path, the microphone is connected to the left channel ADC while the mono output of the stereo mixer is connected to right channel ADC.

The STAC9752A/9753A includes full Stereo Microphone Pre-Amp support and can be used with the 10, 20 and 30dB Microphone Boost options. This integration allows for additional cost savings and options.

The STAC9752A/9753A also includes IDT's Universal Jacks™ functionality for jack interchangeability. The STAC9752A/9753A includes internal jack sensing using proprietary current- and impedance-sensing techniques. The impedance load on any of the inputs or outputs, including the Headphone and Line Outputs, can be detected. This enables jack sensing on the Headphone and Line_Out. The STAC9752A/9753A jack sense can detect the presence of devices on the Headphone and Line Outputs and on both Mic inputs.

The STAC9752A/9753A implementation of jack sense uses the Extended Paging Registers defined by the AC'97 2.3 Specification. This allows for additional registry space to hold the identification information about the CODEC, the jack sensing details and results, and the external surroundings of the CODEC. The information within the Extended Paging Registers will allow for the automatic configuration of the audio subsystem without end-user intervention. For example, the BIOS can populate the Extended Paging Registers with valuable information for both the audio driver and the operating system such as gain and attenuation stages, input population and input phase. With this input information, the IDT driver will automatically provide to the Volume Control Panel only the vol-

ume sliders that are implemented in the system, thus improving the end-user's experience with the PC.

The information in the Extended Paging Registers will also allow for automatic configuration of microphone inputs, the ability to switch between SPDIF and analog outputs, the routing of the master volume slider to the proper physical output, and SoftEQ configurations. The fully parametric IDT SoftEQ can be initiated upon jack insertion and sensed impedance levels.

The STAC9752A/9753A also offers two styles of PC BEEP, Analog and Digital. The digital PC BEEP is a new feature added to the AC'97 Specification Rev 2.3.

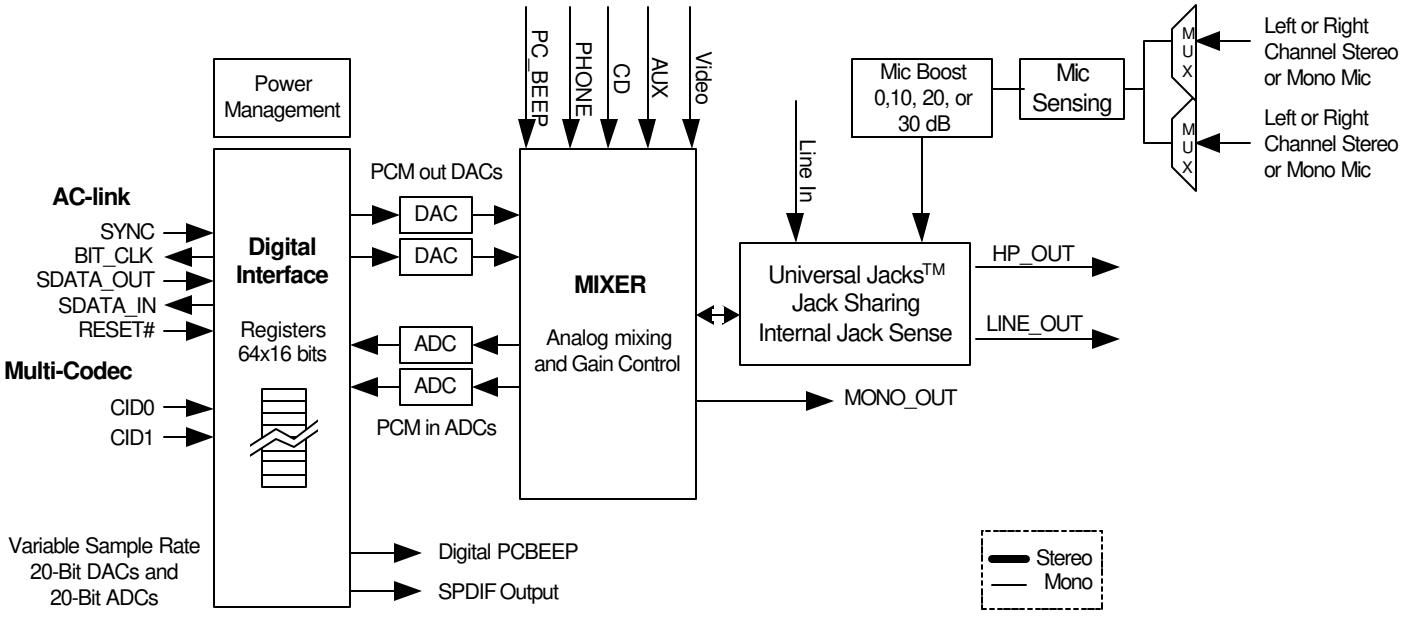
The STAC9752A/9753A is designed primarily to support stereo (2-speaker) audio. True AC-3 playback can be achieved for 6-speaker applications by taking advantage of the multi-CODEC option available in the AC'97 architecture and supported by the STAC9752A/9753A. Additionally, the STAC9752A/9753A provides for a stereo enhancement feature, IDT Surround 3D (SS3D). SS3D provides the listener with several options for improved speaker separation beyond the normal 2- or 4-speaker arrangements.

The STAC9752A/9753A can be SoundBlaster® and Windows Sound System® compatible when used with IDT's WDM driver for Windows 98/2K/ME/XP or with Intel/Microsoft driver included with Windows 2K/ME/XP.

SoundBlaster is a registered trademark of Creative Labs.
Windows is a registered trademark of Microsoft Corporation.

1.3. STAC9752A/9753A Block Diagram

Figure 1. STAC9752A/9753A Block Diagram



1.4. Key Specifications

- Analog LINE_OUT SNR: 94 dB
- Digital DAC SNR: 92 dB
- Digital ADC SNR: 85 dB
- Full-scale Total Harmonic Distortion: 0.002%
- Crosstalk between Input Channels: -70 dB
- Spurious Tone Rejection: 100 dB
- Stereo Microphone Input

1.5. Related Materials

- Product Brief
- Reference Designs for MB, AMR, CNR, and ACR applications
- Audio Precision Performance Plots

1.6. Additional Support

Additional product and company information can be obtained by going to the IDT web site at: www.IDT.com

2. CHARACTERISTICS AND SPECIFICATIONS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9752A/9753A. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		±5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0^oC to $+70^oC$
Storage temperature		-55 ^oC to +125 ^oC
Soldering temperature		260 ^oC for 10 seconds * Soldering temperature information for all available packages begins on page 101.

2.1.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 5 V	4.75	5	5.25	V
	Analog - 3.3 V	3.135	3.3	3.465	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C

ESD: The STAC9752A/9753A is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9752A/9753A implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.1.3. Power Consumption

Parameter	Min	Typ	Max	Unit
Digital Supply Current				
+ 3.3 V Digital	-	35	-	mA
Analog Supply Current				
+ 5 V Analog	-	80	-	mA
+ 3.3 V Analog	-	70	-	mA
Power Down Status				
PR0 Supply Current	-	TBD	-	mA
PR1 Supply Current	-	TBD	-	mA
PR2 Supply Current	-	TBD	-	mA
PR3 Supply Current	-	TBD	-	mA
PR4 Supply Current	-	TBD	-	mA
PR5 Supply Current	-	TBD	-	mA
PR6 Supply Current	-	TBD	-	mA

2.1.4. AC-Link Static Digital Specifications

($T_{ambient}$ = 25 ºC, DVdd = 3.3 V ± 5%, AVss = DVss = 0 V; 50 pF external load)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage Range	Vin	-0.30	-	DVdd + 0.30	V
Low level input range	Vil	-	-	0.35 x DVdd	V
High level input voltage	Vih	0.65 x DVdd	-	-	V
High level output voltage	Voh	0.90 x DVdd	-	-	V
Low level output voltage	Vol	-	-	0.1 x DVdd	V
Input Leakage Current (AC-Link inputs)	-	-10	-	10	µA
Output Leakage Current (Hi-Z AC-Link outputs)	-	-10	-	10	µA
Output buffer drive current	-	-	4	-	mA

2.1.5. STAC9752A Analog Performance Characteristics

($T_{ambient}$ = 25ºC, AVdd = 5.0V±5%, DVdd = 3.3V±5%, AVss = DVss = 0V; 1KHzinputsinewave; SampleFrequency = 48KHz; 0dB = 1Vrms, 10KΩ / 50pFload, Testbench Characterization BW:20Hz–20KHz, 0dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	1.0	-	Vrms
PCM (DAC) to LINE_OUT		1.0		Vrms
MONO_OUT	-	1.0	-	Vrms
HEADPHONE_OUT (32 Ω load) (peak)	-	50	-	mW
Analog S/N: (Note 2)				
CD to LINE_OUT	-	94	-	dB
Other to LINE_OUT	-	94	-	dB
D/A to LINE_OUT	-	92	-	dB
LINE_IN to A/D with High pass filter enabled	-	85	-	dB
Analog Frequency Response (Note 3)	20	-	20,000	Hz
Total Harmonic Distortion: (Note 4)				
CD to LINE_OUT	-	95	-	dB
Other to LINE_OUT	-	95	-	dB
D/A to LINE_OUT (full scale)	-	84	-	dB
LINE_IN to A/D with High pass filter enabled	84	-	-	dB
HEADPHONE_OUT	74	80	-	dB
A/D & D/A Digital Filter Pass Band (Note 5)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 6)	100	-	-	dB
DAC Out-of-Band Rejection (Note 7)	55	-	-	dB
Group Delay (48KHz sample rate)	-		1	ms
Any Analog Input to LINE_OUT Crosstalk (10KHz Signal Frequency)	70	-	-	dB
Any Analog Input to LINE_OUT Crosstalk (1KHz Signal Frequency)	-	100	-	dB
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance (Note 8)	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 x AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB

Note:
1. With +30 dB Boost on, 1.0 Vrms with Boost off
2. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3. ± 1dB limits for Line Output & 0dB gain
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a 20 KHz BW, 48 KHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.

7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.
8. For all inputs except PC BEEP.

2.1.6. STAC9753A Analog Performance Characteristics

($T_{ambient}$ = 25ºC, AVdd = 5.0V±5%, DVdd = 3.3V±5%, AVss = DVss = 0V; 1KHzinputsinewave; SampleFrequency = 48KHz; 0dB = 1Vrms, 10KΩ / 50pFload, Testbench Characterization BW:20Hz–20KHz, 0dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	0.5	-	Vrms
PCM (DAC) to LINE_OUT		0.5		Vrms
MONO_OUT	-	0.5	-	Vrms
HEADPHONE_OUT (32 Ω load) (peak)	-	12.5	-	mW
Analog S/N: (Note 2)				
CD to LINE_OUT	-	93	-	dB
Other to LINE_OUT	-	93	-	dB
D/A to LINE_OUT	-	91	-	dB
LINE_IN to A/D with High pass filter enabled	-	85	-	dB
Analog Frequency Response (Note 3)	20	-	20,000	Hz
Total Harmonic Distortion: (Note 4)				
CD to LINE_OUT	-	93	-	dB
Other to LINE_OUT	-	93	-	dB
D/A to LINE_OUT (full scale)	-	84	-	dB
LINE_IN to A/D with High pass filter enabled	-	84	-	dB
HEADPHONE_OUT	74	80	-	dB
A/D & D/A Digital Filter Pass Band (Note 5)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 6)	100	-	-	dB
DAC Out-of-Band Rejection (Note 7)	55	-	-	dB
Group Delay (48KHz sample rate)	-	-	1	ms
Any Analog Input to LINE_OUT Crosstalk (10KHz Signal Frequency)	70	-	-	dB
Any Analog Input to LINE_OUT Crosstalk (1KHz Signal Frequency)	-	100	-	dB
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance (Note 8)	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 x AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC

Note:
1. With +30 dB Boost on, 1.0Vrms with Boost off
2. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).0 dB gain, 20 KHz BW, 48 KHz Sample Frequency± 1 dB limits
3. ± 1dB limits for Line Output & 0 dB gain

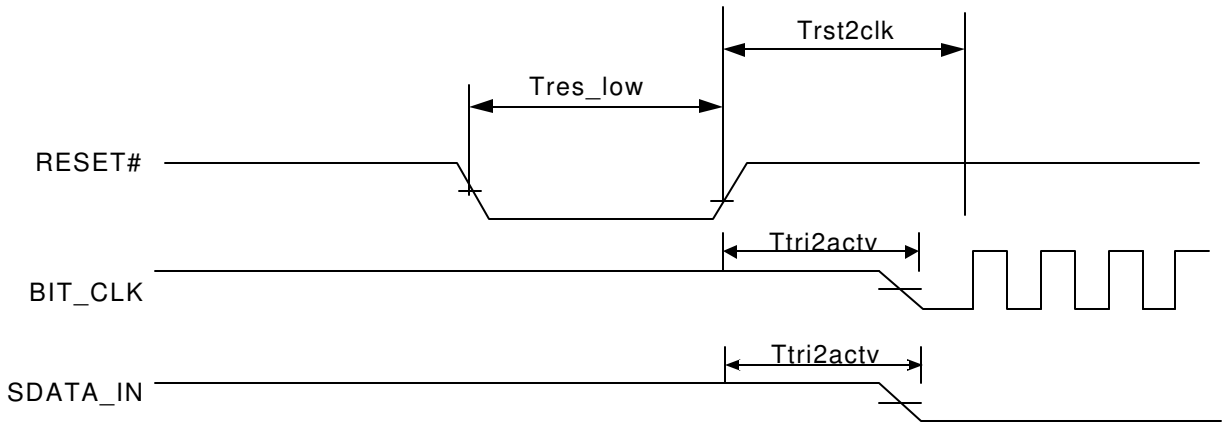
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a, 20 KHz BW, 48 KHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.
8. For all inputs except PC BEEP.

2.2. AC Timing Characteristics

($T_{ambient}$ = 25 °C, AVdd = 3.3V or 5V ± 5%, DVdd = 3.3V ± 5%, AVss = DVss = 0V; 75pF external load for BIT_CLK and 60pF external load for SDATA_IN)

2.2.1. Cold Reset

Figure 2. Cold Reset Timing

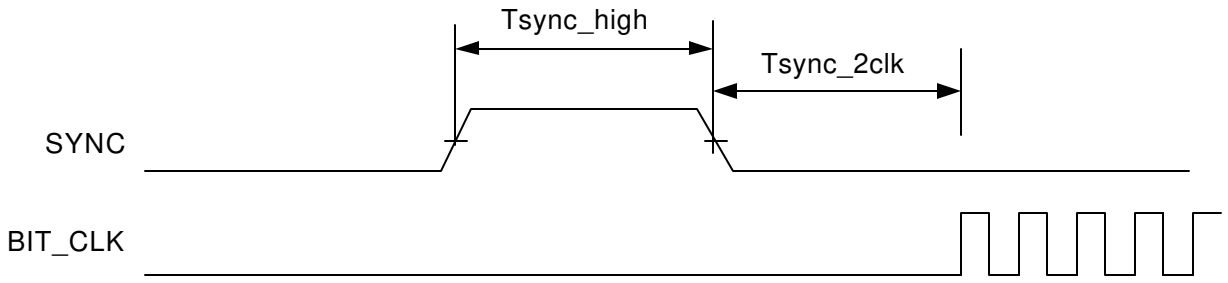


Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Tres_low	1.0	-	-	µs
RESET# inactive to SDATA_IN or BIT_CLK active delay	Tri2actv	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	Trst2clk	.01628	-	400	µs
BIT_CLK active to RESET# asserted (Not shown in diagram)	Tclk2rst	0.416	-	-	µs

Note: BIT_CLK and SDATA_IN are in a high impedance state during reset.

2.2.2. Warm Reset

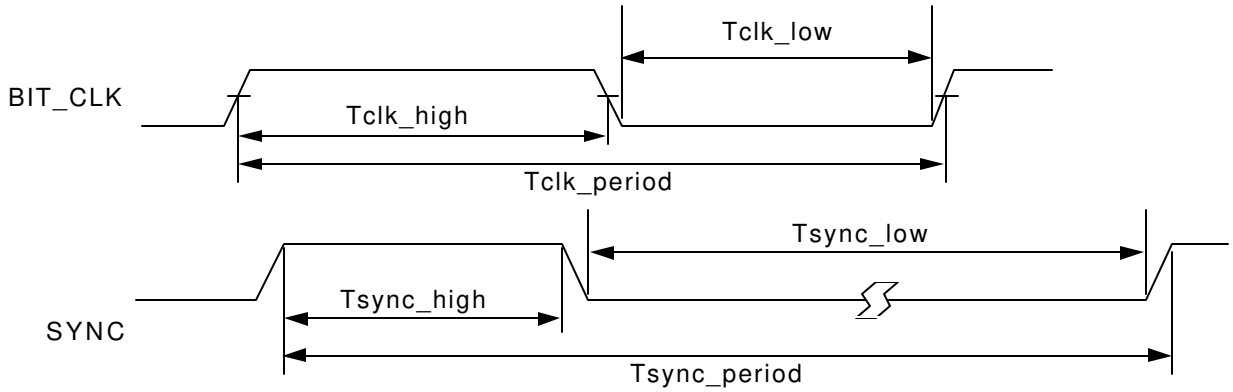
Figure 3. Warm Reset Timing



Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tsync_high	1.0	1.3	-	µs
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

2.2.3. Clocks

Figure 4. Clocks Timing



Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	750	-	ps
BLT_CLK high pulse width (Note 1)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (Note 1)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	Tsync_period	-	20.8	-	µs
SYNC high pulse width	Tsync_high	-	1.3	-	µs
SYNC low pulse width	Tsync_low	-	19.5	-	µs

Note: 1. Worst case duty cycle restricted to 45/55.

2.2.4. STAC9752A/9753A Crystal Elimination Circuit and Clock Frequencies

The STAC9752A/9753A supports several clock frequency inputs as described in the following table. In general, when a 24.576MHz crystal is not used, the XTALOUT pin should be tied to ground. This short to ground configures the part into an alternate clock mode and enables an on board PLL.

CODEC Modes:
P = The STAC9752A/9753A as a Primary CODEC
S = The STAC9752A/9753A as a Secondary CODEC.

Table 1. Clock mode configuration

XTL_OUT Pin Config	CID1 Pin Config	CID0 pin config	Clock Source Input	CODEC Mode	CODEC ID
XTAL	float	float	24.576MHz xtal	P	0
XTAL or open	float	pulldown	12.288MHz bit clk	S	1
XTAL or open	pulldown	float	12.288MHz bit clk	S	2
XTAL or open	pulldown	pulldown	12.288MHz bit clk	S	3
short to ground	float	float	14.31818MHz source	P	0
short to ground	float	pulldown	27MHz source	P	0

Table 1. Clock mode configuration

XTL_OUT Pin Config	CID1 Pin Config	CID0 pin config	Clock Source Input	CODEC Mode	CODEC ID
short to ground	pulldown	float	48MHz source	P	0
short to ground	pulldown	pulldown	24.576MHz source	P	0

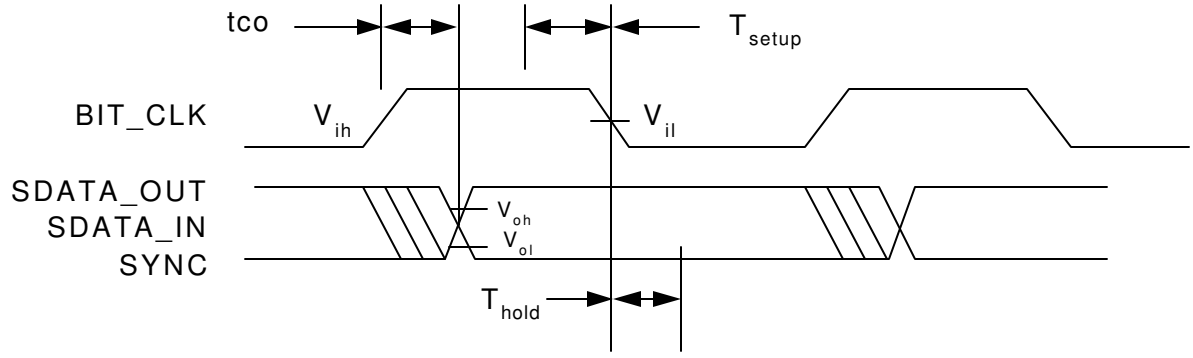
Table 2. Common Clocks and Sources

Clock Source	Clock Frequency
XTAL	24.576MHz
BIT_CLK	12.288MHz
VGA	14.31818MHz
Digital Video	27MHz
USB	48MHz

2.2.5. Data Setup and Hold

(50pF external load)

Figure 5. Data Setup and Hold Timing



Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	10	-	-	ns
Hold from falling edge of BIT_CLK	Thold	10	-	-	ns
Output Valid Data from rising edge of BIT_CLK	tco	-	-	15	ns

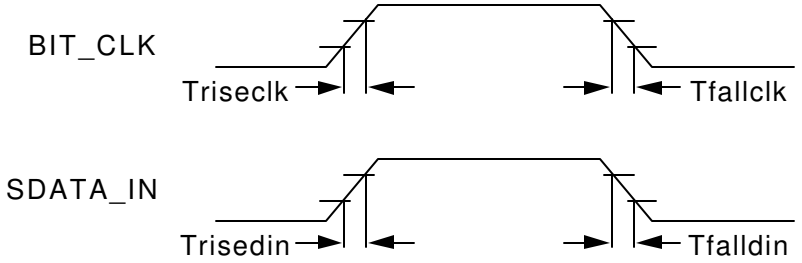
Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

2.2.6. Signal Rise and Fall Times

(BIT_CLK: 75pF external load; from 10% to 90% of Vdd)

(SDATA_IN: 60pF external load; from 10% to 90% of Vdd)

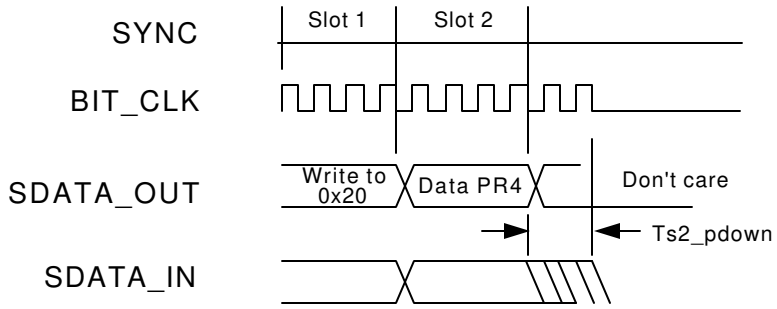
Figure 6. Signal Rise and Fall Times Timing



Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	Triseclk	-	-	6	ns
BIT_CLK fall time	Tfallclk	-	-	6	ns
SDATA_IN rise time	Trisedin	-	-	6	ns
SDATA_IN fall time	Tfalldin	-	-	6	ns

2.2.7. AC-Link Low Power Mode Timing

Figure 7. AC-Link Low Power Mode Timing

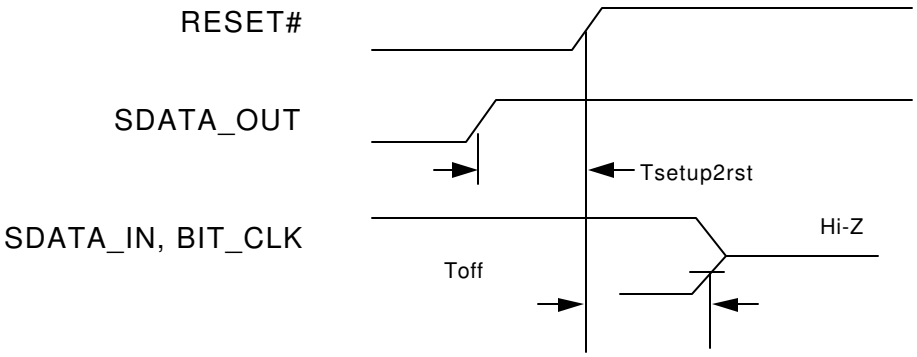


Note: BIT_CLK not to scale

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	µs

2.2.8. ATE Test Mode

Figure 8. ATE Test Mode Timing



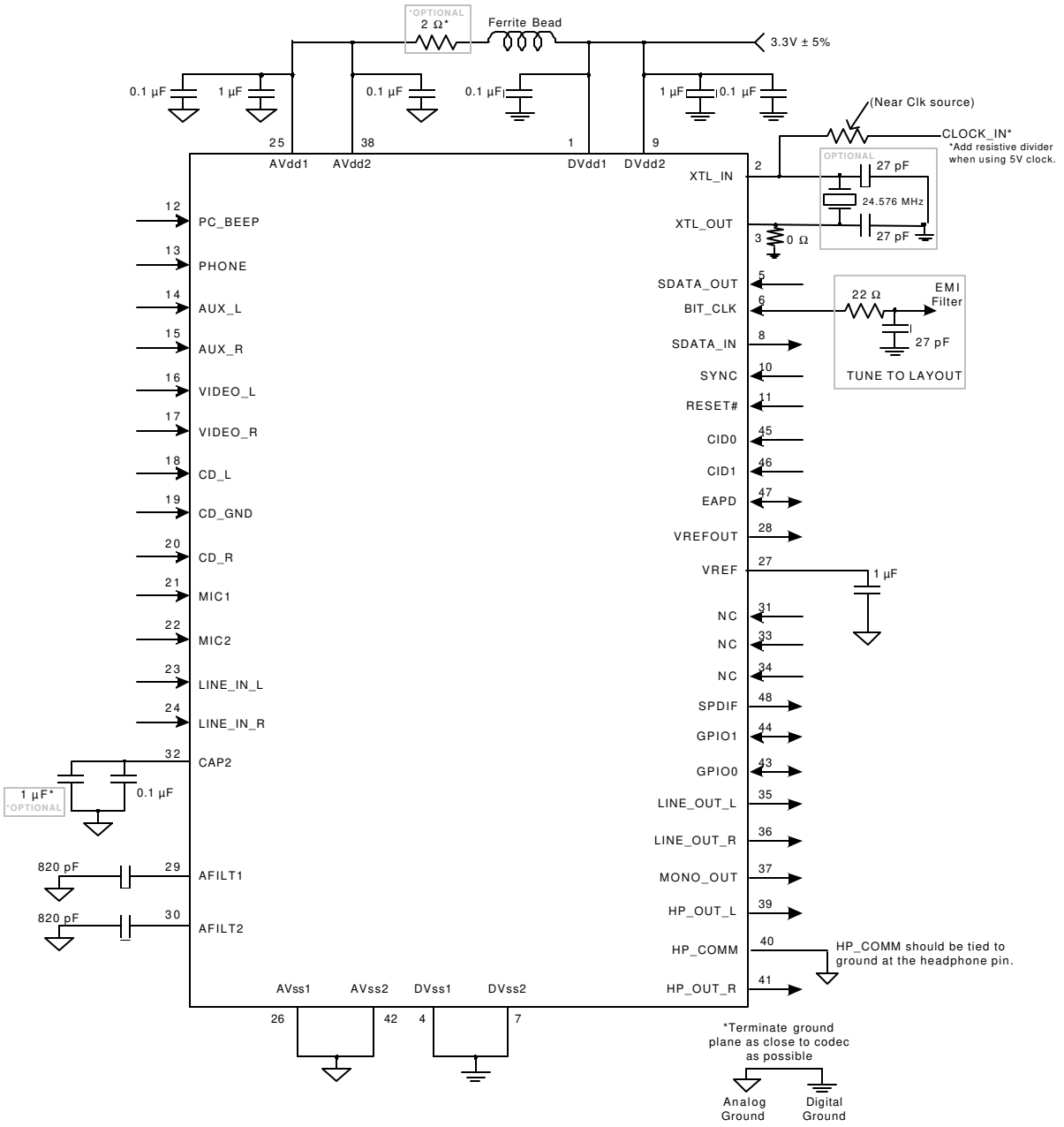
Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Note:
1. All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes the STAC9752A/9753A AC-Link outputs to go high impedance, which is suitable for ATE in-circuit testing.
2. Once the test mode has been entered, the STAC9752A/9753A must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.
3. # denotes active low.

3. TYPICAL CONNECTION AND POWER DIAGRAMS

3.1. STAC9752A/9753A Typical Connection Diagram for 48-pin LQFP

Figure 9. STAC9752A/9753A Typical Connection Diagram 48-pin LQFP

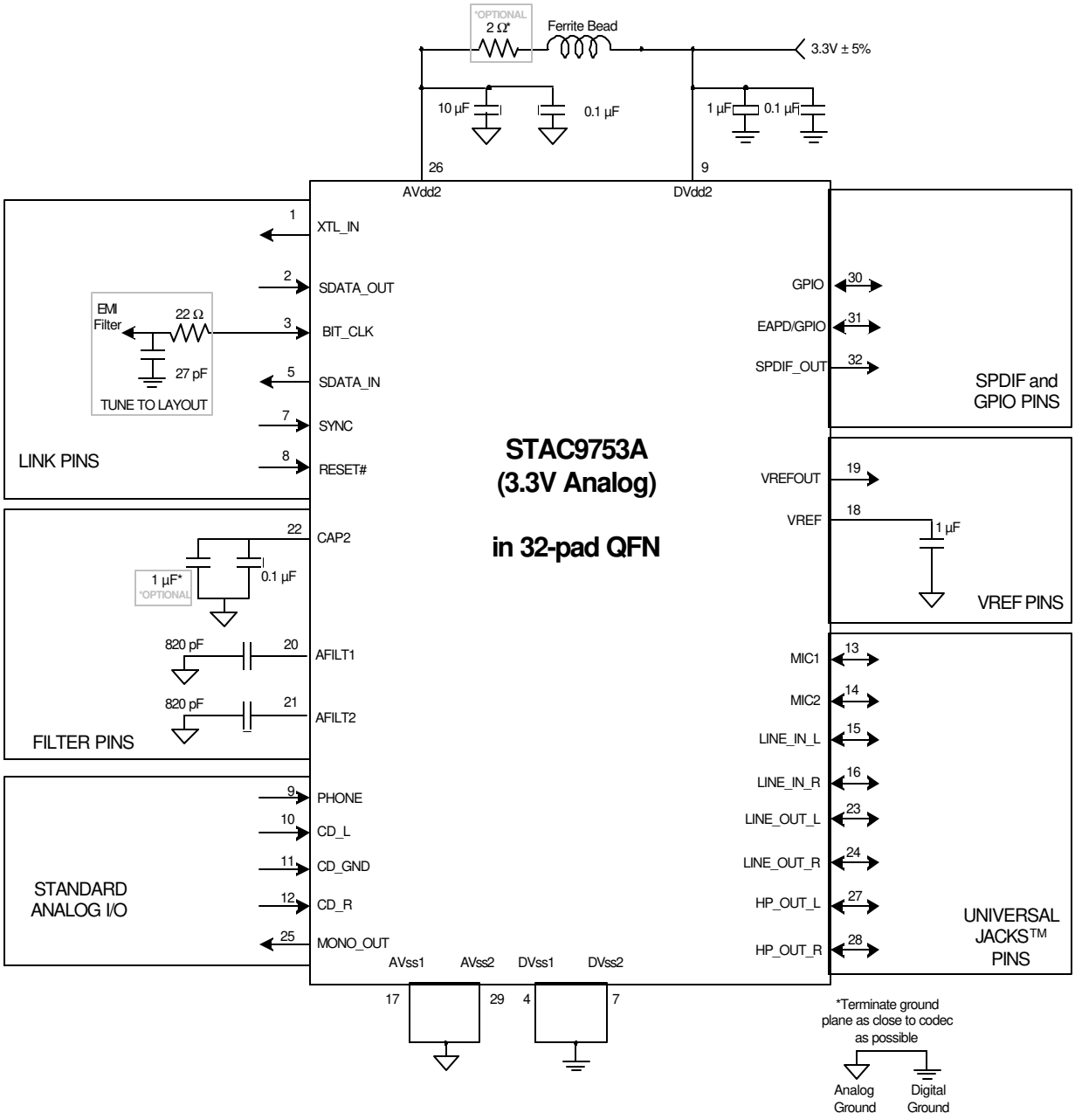


Note: Pin 48: To Disable SPDIF, use an 1KΩ - 10 KΩ external pullup resistor.

Note: The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC'97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause significant distortion. If there is no analog CD input, then this pin can be No-Connect.

3.2. STAC9752A/9753A Typical Connection Diagram for 32-pad QFN

Figure 10. STAC9752A/9753A Typical Connection Diagram 32-pad QFN



Note: Pin 48: To Disable SPDIF, use an 1KΩ - 10 KΩ external pullup resistor.

Note: The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC'97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause bad distortion. If there is no analog CD input, then this pin can be No-Connect.

3.3. Split Independent Power Supply Operation

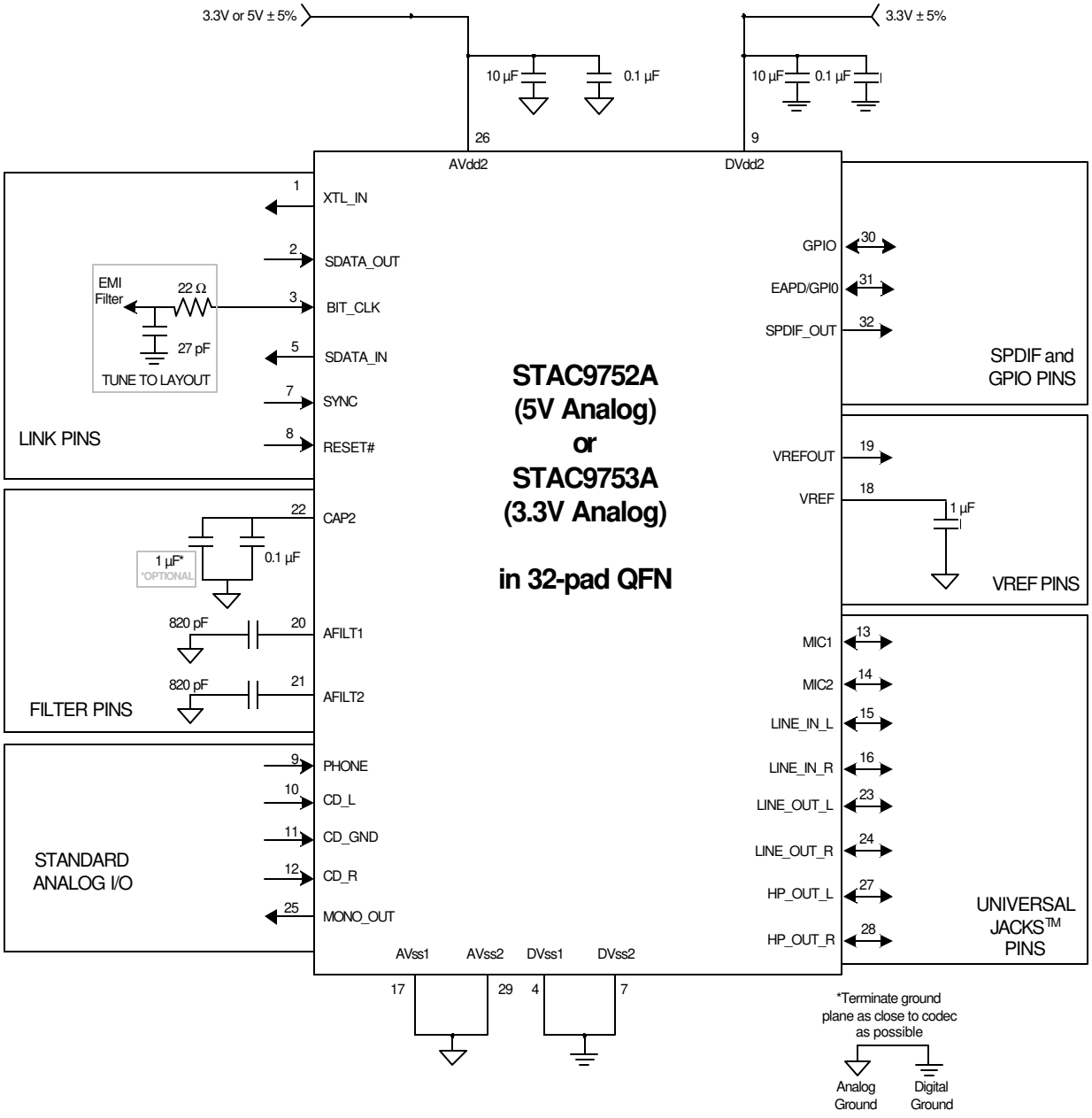
In PC applications, one power supply input to the STAC9752A/9753A may be derived from a supply regulator and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's CODECs would be subject to on-chip SCR type latch-up.

IDT's STAC9752A/9753A specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the CODEC. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.

However, the STAC9752A/9753A is not designed to operate for extended periods with only the analog supply active.

3.4. Split Independent Power Supply Operation for the 32-pad QFP Package

Figure 11. Split Connection Diagram 32-pad QFN



4. CONTROLLER, CODEC, AND AC-LINK

This section describes the physical and high-level functional aspects of the AC'97 Controller to CODEC interface, referred to as the AC-Link.

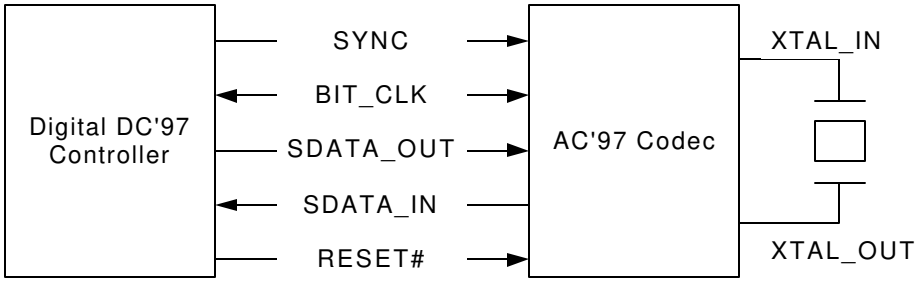
4.1. AC-Link Physical interface

The STAC9752A/9753A communicates with its companion Digital Controller via the AC-Link digital serial interface. AC-Link has been defined to support connections between a single Controller and up to four CODECs. All digital audio, modem and handset data streams, as well as all control (command/status) information are communicated over this serial interconnect, which consists of a clock (BIT_CLK), frame synchronization (SYNC), serial data in (SDATA_IN), serial data out (SDATA_OUT), and a reset (RESET#).

4.2. Controller to Single CODEC

The simplest and most common AC'97 system configuration is a point-to-point AC-Link connection between Controller and the STAC9752A/9753A, as illustrated in Figure 12.

Figure 12. AC-Link to its Companion Controller



A primary CODEC may act as either a source or a consumer of the BIT_CLK, depending on the configuration.

While RESET# is asserted, if a clock is present at the BIT_CLK pin for at least five cycles before RESET# is de-asserted, then the CODEC is a consumer of BIT_CLK, and must not drive BIT_CLK when RESET# is de-asserted. The clock is being provided by other than the primary CODEC, for instance by the controller or an independent clock chip. In this case the primary CODEC must act as a consumer of the BIT_CLK signal as if it were a secondary CODEC.

This clock source detection must be done each time the RESET# line is asserted. In the case of a warm reset, where the clock is halted but RESET# is not asserted, the CODEC must remember the clock source, and not begin generating the clock on the assertion of SYNC if the CODEC had previously determined that it was a consumer of BIT_CLK.

The STAC9752A/9753A uses the XTAL_OUT pin (Pin 3) and the CID0 and CID1 pins (Pins 45 & 46) to determine its alternate clock frequencies. See section2.2.4: page 17 for additional information on Crystal Elimination and for supported clock frequencies.