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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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HIGH-PERFORMANCE 6-CHANNEL AC'97 2.3 CODEC WITH UNIVERSAL JACKS™

STAC9758/9759

OVERVIEW

High performance, 6-channel, AC'97 2.3 CODECs with high Signal-to-Noise ratio and low distortion.

FEATURES

- **High performance ΣΔ technology**
- **6-Channel AC'97 2.3 CODECs**
- **20-bit full duplex stereo ADCs**
- **20-bit full duplex DACs**
- **Headphone drive capability**
- **SPDIF_IN Support**
- **SPDIF_OUT Support, including 96 kHz**
- **ADAT® Optical "Litepipe" Interface Support**
- ***Universal Jacks*™ Functionality for jack interchangeability**
- ***Internal* Jack Sensing**
- **Crystal Elimination Circuit**
- **Front/Rear Stereo Microphone**
- **96 kHz DAC Playback support**
- **Up to 5 General Purpose I/Os**
- **Digital and Analog PC BEEP**
- **AC'97 2.3 Paging Registers and Analog Plug and Play Capability**
- **Energy saving dynamic power modes**
- **>90 dB SNR and >-90dBV THD+N**
- **Adjustable VREF_OUT Control**
- **Pin compatible with 2-Channel CODECs**
- **Independent sample rates for ADC & DACs**
- **+3.3 V & +5 V analog power supply options**

DESCRIPTION

IDT's STAC9758/9759 are general purpose 20-bit, full duplex, 6-Channel audio CODECs conforming to the analog component specification of AC '97 (Audio Codec 97 Component Specification Rev. 2.3). The STAC9758/9759 incorporates IDT's proprietary ΣΔ technology to achieve a DAC SNR in excess of 90dB. With IDT's headphone drive capability, headphones can be driven without an external amplifier. The STAC9758/9759 communicates via the five AC-Link to any digital component of AC '97, providing flexibility in the audio system design. Packaged in an AC '97 compliant 48-pin TQFP, the STAC9758/9759 can be placed on the motherboard, daughter boards, PCI, AMR, CNR, MDC or ACR cards.

Supported ADC and DAC audio sample rates include 96kHz, 48kHz, 44.1kHz, 32kHz, 22.05kHz, 16kHz, 11.025kHz, and 8 kHz; additional rates are supported in the STAC9758/9759 soft audio drivers. All ADCs and DACs operate at 20-bit resolution. SPDIF_OUT supported sample rates include 96kHz, 48kHz, 44.1kHz and 32kHz. SPDIF_IN supports 48kHz and 44.1kHz.

The STAC9758/9759 includes ***internal*** jack sensing using proprietary IDT current and impedance-sensing techniques. The impedance load on any of the inputs or outputs can be detected. The STAC9758/9759 also supports ***Universal Jacks*™** functionality for jack interchangeability.

The GPIOs on the STAC9758/9759 remain available for advanced configurations. The STAC9758/9759 can support up to 5 GPIOs.

The STAC9758/9759 is designed primarily to support 6-channel audio. Additionally, the STAC9758/9759 provides for a stereo enhancement feature, IDT Surround 3D (SS3D).

The STAC9758/9759 also supports the ADAT® Optical "Litepipe" Interface, which provides an 8 channel output for professional and consumer audio applications.

The STAC9758/9759 can be SoundBlaster® and Windows Sound System® compatible when used with IDT's WDM driver for Windows 98/2K/ME/XP or with Intel/Microsoft driver included with Windows 2K/ME/XP.

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1. DESCRIPTION

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The STAC9758/9759 includes ***internal*** jack sensing using proprietary IDT current and impedance-sensing techniques. The impedance load on any of the inputs or outputs can be detected. The STAC9758/9759 also supports ***Universal Jacks™*** functionality for jack interchangeability.

The GPIOs on the STAC9758/9759 remain available for advanced configurations. The STAC9758/9759 can support up to 5 GPIOs.

The STAC9758/9759 implementation of ***internal*** jack sense uses the Extended Paging Registers defined by the AC '97 2.3 Specification. This allows for additional registry space to hold the identification information about the CODEC, the jack sensing details and results, and the external surroundings of the CODEC. The information within the Extended Paging Registers will allow for the automatic configuration of the audio subsystem without end-user intervention. For example, the BIOS can populate the Extended Paging Registers with valuable information for both the audio driver and the operating system such as gain and attenuation stages, input population and input phase and jack location. With this input information, the IDT driver will automatically provide to the Volume Control Panel only the volume sliders that are implemented in the system, thus improving the end-user's experience with the PC.

The information in the Extended Paging Registers will also allow for automatic configuration of microphone inputs, the ability to switch between SPDIF and analog outputs, the routing of the master volume slider to the proper physical output, and SoftEQ configurations. The fully parametric IDT SoftEQ can be initiated upon jack insertion and removal.

The STAC9758/9759 is designed primarily to support 6-channel audio. Additionally, the STAC9758/9759 provides for a stereo enhancement feature, IDT Surround 3D (SS3D).

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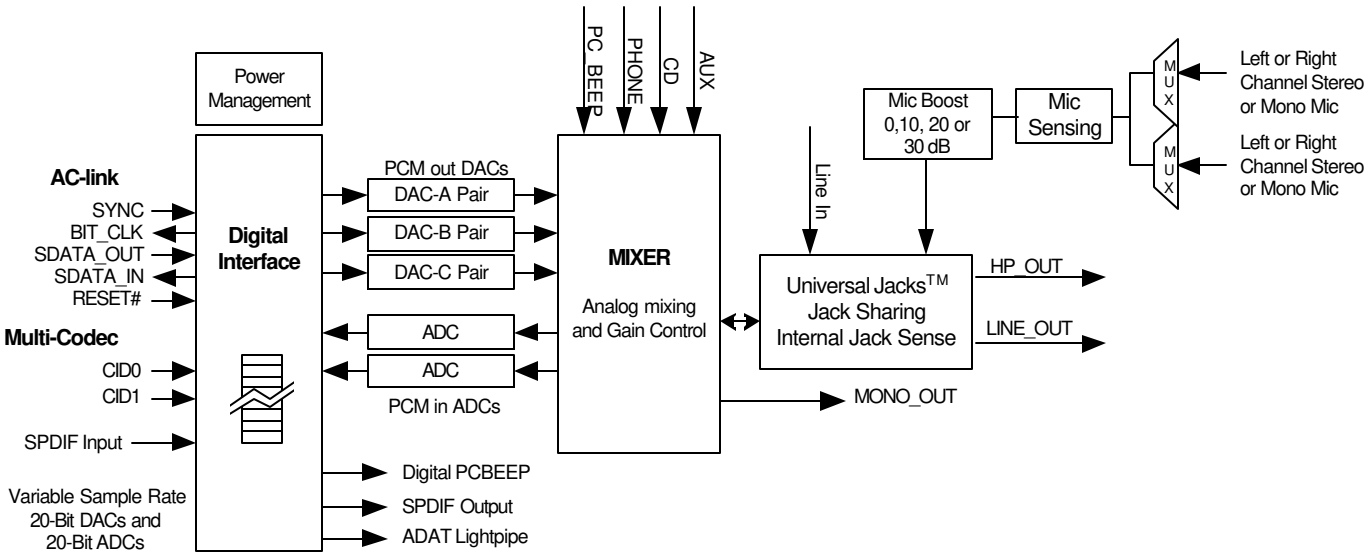
SoundBlaster is a registered trademark of Creative Labs.
Windows is a registered trademark of Microsoft Corporation.
ADAT Optical is a registered trademark of Alesis Corporation.

1.1. Features

- Six Channel, AC'97 Revision 2.3 Compliant
- 20-bit ADCs
- 20-bit DACs
- 96KHz Sample Rate support
- SPDIF OUTPUT at 32 KHz, 44.1KHz, and 48KHz
- Double Rate SPDIF Output at 96 KHz
- ADAT Optical Lightpipe Output
  - 8 channel, 20 bit output at 48KHz and 44.1KHz
- SPDIF INPUT at 48KHz and 44.1KHz with Internal Jack Sensing
- HEADPHONE AMPLIFIER with 50mW per channel
- Programmable +3dB voltage gain
- **Universal Jacks™** and 3-jack/6-channel jack-sharing
  - The STAC9758/9759 supports 5 stereo analog I/O ports.
  - These ports correspond to the following AC'97 referenced pins: Mic1/2 (21/22), Line_In (23/24), Line_Out (35/36), Surround (39/41), Center/LFE (43/44).
  - These 5 ports may be used in the common "jack sharing" implementation or in a completely reconfigurable (Universal Jacks™) configuration.
  - Pins 35 and 36 = Headphone (default)
  - Pins 23 and 24 = Line_In (default) or Surround out.
  - Pin 21 and 22 = Microphone (default, mono) or CTR/LFE out.
  - Rear jacks are dynamically reconfigurable to input or output.
  - Internal jack sense is used to detect attached devices and inform the driver to reconfigure the jack as appropriate.
  - All "Universal Jacks™" pins (as well as pins 16/17) may also be inputs.
- Mixer Inputs
  - Analog PC Beep, Digital PC Beep, Phone, Aux In, Line In (has pre-select mux for jack sharing/Universal Jacks™), Mic In (mono and stereo modes - includes pre-select mux), DAC-A, DAC-B
  - Split-mute option on all stereo inputs allows left and right inputs to be muted independently.
- Analog Output Sources
  - DAC-A, DAC-B, DAC-C, Stereo Mix, Mono
- Analog I/O
  - Pins 21/22, 23/24, 35/36, 39/41, 43/44
  - All Analog I/O pins have analog jack sense
  - Pins 35/36 and 39/41 are capable of driving headphones
  - All outputs are high impedance when powered down
- Split-mute (bit D7) option on all outputs allows left and right outputs to be muted independently
- Internal Microphone Sensing
- Mono and Dual Stereo Microphone Support
- Adjustable VRefOut Control
- Extended AC'97 2.3 Paging Registers

- Up to 5 GPIO depending upon configuration
- Power Management
- IDT SS3D
- Primary and Secondary Mode Operation
- High performance Sigma-Delta technology
- Digital and Analog PC Beep Option
- Digital-ready status
- Crystal Elimination Circuit
- 0, 10db, 20db, and 30 dB microphone boost capability
- +3.3 V (STAC9759) and +5 V (STAC9758) analog power supply options

1.2. Block Diagram



2. CHARACTERISTICS/SPECIFICATIONS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9758/9759. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0°C to +70°C
Storage temperature		-55 °C to +125 °C
Soldering temperature		260 °C for 10 seconds * Soldering temperature information for all available packages begins on page 114.

2.1.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 5 V	4.75	5	5.25	V
	Analog - 3.3 V	3.135	3.3	3.465	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C

ESD: The **STAC9758/9759** is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the **STAC9758/9759** implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.1.3. Power Consumption

Parameter		Min	Typ	Max	Unit
Digital Supply Current					
+ 3.3 V Digital		-	44	-	mA
Analog Supply Current (at Reset state)					
+ 5 V Analog		-	58	-	mA
+ 3.3 V Analog		-	52	-	mA
Power Down Status (individually asserted)	(All PR measurements taken while unmuted.)				
All paths unmuted	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	96 88 49	-	mA
PR0	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	90 82 39	-	mA
PR1	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	71 66 34	-	mA
PR2	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	51 45 22	-	mA
PR3	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	28 26 22	-	mA
PR4	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	104 89 1.3	-	mA
PR5	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	89 83 22	-	mA
PR6	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	84 79 49	-	mA
PR0 & PR1	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	65 61 22	-	mA
PR0, PR1, PR2, PR6	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	12 11 22	-	mA
PR0, PR1, PR2, PR3, PR6	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	0.8 0.6 22	-	mA
PR0, PR1, PR2, PR3, PR4, PR6	+5V Analog Supply Current +3.3V Analog Supply Current +3.3V Digital Supply Current	-	0.8 0.6 1.3	-	mA
For additional power configuration, each DAC pairs can be powered down individually.					

2.1.4. AC-Link Static Digital Specifications

($T_{ambient}$ = 25 ºC, DVdd = 3.3V ± 5%, AVss=DVss = 0V)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage Range	Vin	-0.30	-	DVdd + 0.30	V
Low level input range	Vil	-	-	0.35 x DVdd	V
High level input voltage	Vih	0.65 x DVdd	-	-	V
High level output voltage	Voh	0.90 x DVdd	-	-	V
Low level output voltage	Vol	-	-	0.1 x DVdd	V
Input Leakage Current (AC-Link inputs)	-	-10	-	10	µA
Output Leakage Current (High-impedance AC-Link outputs)	-	-10	-	10	µA
BIT_CLK (primary mode) Output Leakage Current	-	-10	-	100*	µA
BIT_CLK (secondary mode) Output Leakage Current	-	-10	-	10	µA
Output buffer drive current	-	-	8		mA
BIT_CLK/SPDIF Output Drive Current	-	-	24		mA

*Note: * Due to an internal pull-down resistor, the BIT_CLK pin will exhibit less than 100 µA of leakage current when the CODEC is configured as primary. This pin meets the +/- 10 µA leakage specification when configured as secondary.*

2.1.5. STAC9758 5V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0V ± 5%, DVdd = 3.3V ± 5%, AVss = DVss = 0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 Vrms, 10KΩ/50pF load, Testbench Characterization BW: 20Hz – 20KHz, 0dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.00	-	Vrms
Microphone Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	1.00	-	Vrms
PCM (DAC) to LINE_OUT	-	1.00	-	Vrms
MONO_OUT	-	1.00	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	50	-	mW
Dynamic Range: -60dB signal level (Note 2)				
CD to LINE_OUT	-	98	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	100	-	dB
PCM (DAC) to LINE_OUT	-	85	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	88	-	dB
LINE_IN to A/D (1 VRMS input referenced)	-	90	-	dB
LINE_IN to HEADPHONE_OUT	-	94	-	dB

Parameter	Min	Typ	Max	Unit
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
CD to LINE_OUT	-	-90	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	-90	-	dB
PCM (DAC) to LINE_OUT (full scale)	-	-86	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	-89	-	dB
LINE_IN to A/D (-3dBV input Level)	-	-81	-	dB
HEADPHONE_OUT (32 Ω load)	-	-80	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-85	-	dB
SNR (idle channel) (Note 5)				
DAC to LINE_OUT	-	85	-	dB
DAC in BYPASS Mode	-	87	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	100	-	dB
LINE_IN to A/D with High Pass Filter enabled	-	92	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency)	-	-70	-	dB
Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency)	-	-90	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.45X AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	10	20	mV
Deviation from Linear Phase	-	-	1	degrees

Parameter	Min	Typ	Max	Unit
LINE_OUT/MONO_OUT Load Resistance	10	-	-	KΩ
LINE_OUT/MONO_OUT Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	-	100	pF
Mute Attenuation	-	96	-	dB
PLL lock time	-	100	200	µsec
PLL 24.576MHz clock jitter	-	-	750	psec
PLL frequency multiplication tolerance	-	-	12.5	ppm
PLL bit clock jitter	-	-	750	psec

Note:
1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. 48 KHz Sample Frequency
5. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.1.6. STAC9759 3.3V Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = DVdd = 3.3V ± 5%, AVss=DVss=0V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 Vrms, 10KΩ/50pF load, Testbench Characterization BW: 20Hz – 20KHz, 0dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.00	-	Vrms
Microphone Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	0.5	-	Vrms
PCM (DAC) to LINE_OUT	-	0.5	-	Vrms
MONO_OUT	-	0.5	-	Vrms
HEADPHONE_OUT (32 Ω load) per channel (peak)	-	12.5	-	mW
Dynamic Range: -60dB signal level (Note 2)				
CD to LINE_OUT	-	85	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	85	-	dB
PCM (DAC) to LINE_OUT	-	82	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	83	-	dB
LINE_IN to A/D	-	85	-	dB

Parameter	Min	Typ	Max	Unit
LINE_IN to HEADPHONE_OUT	-	85	-	dB
Analog Frequency Response (Note 3)	10	-	30,000	Hz
Total Harmonic Distortion + Noise (-3dB): (Note 4)				
CD to LINE_OUT	-	-90	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	-92	-	dB
PCM (DAC) to LINE_OUT (full scale)	-	-81	-	dB
PCM (DAC) in BYPASS Mode to LINE_OUT	-	-84	-	dB
LINE_IN to A/D(-3dBV input Level)	-	-81	-	dB
HEADPHONE_OUT (32 Ω load)	-	-80	-	dB
HEADPHONE_OUT (10 KΩ load)	-	-90	-	dB
SNR (idle channel) (Note 5)				
DAC to LINE_OUT	-	83	-	dB
DAC in BYPASS Mode	-	86	-	dB
LINE / AUX / VIDEO to LINE_OUT	-	100	-	dB
LINE_IN to A/D with High Pass Filter enabled	-	88	-	dB
A/D & D/A Digital Filter Pass Band (Note 6)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 7)	-100	-	-	dB
DAC Out-of-Band Rejection (Note 8)	-55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Power Supply Rejection Ratio (1 KHz)	-	-70	-	dB
Power Supply Rejection Ratio (20 KHz)	-	-40	-	dB
Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency)	-	-70	-	dB
Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency)	-	-90	-	dB
Spurious Tone Rejection	-	-100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
VREF	-	0.41X AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC
DAC Offset Voltage	-	10	20	mV

Parameter	Min	Typ	Max	Unit
Deviation from Linear Phase	-	-	1	deg.
LINE_OUT/MONO_OUT Load Resistance	10	-	-	KΩ
LINE_OUT/MONO_OUT Load Capacitance	-	-	50	pF
HEADPHONE_OUT Load Resistance	-	32	-	Ω
HEADPHONE_OUT Load Capacitance	-	-	100	pF
Mute Attenuation	-	96	-	dB
PLL lock time	-	100	200	µsec
PLL 24.576MHz clock jitter	-	-	750	psec
PLL frequency multiplication tolerance	-	-	12.5	ppm

Note:
1. With +30 dB Boost on, 1.00 Vrms with Boost off.
2. Ratio of Full Scale signal to noise output with -60dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth.
3. ± 1dB limits for Line Output & 0 dB gain, at -20dBV
4. Ratio of Full Scale signal to THD+N output with -3dB signal, measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. 48 KHz Sample Frequency
5. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
6. Peak-to-Peak Ripple over Passband meets ± 0.25dB limits, 48 KHz Sample Frequency.
7. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
8. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.

2.2. AC Timing Characteristics

($T_{ambient}$ = 25 °C, AVdd = 3.3V or 5V ± 5%, DVdd = 3.3V ± 5%, AVss=DVss=0V; 50pF external load)

2.2.1. Cold Reset

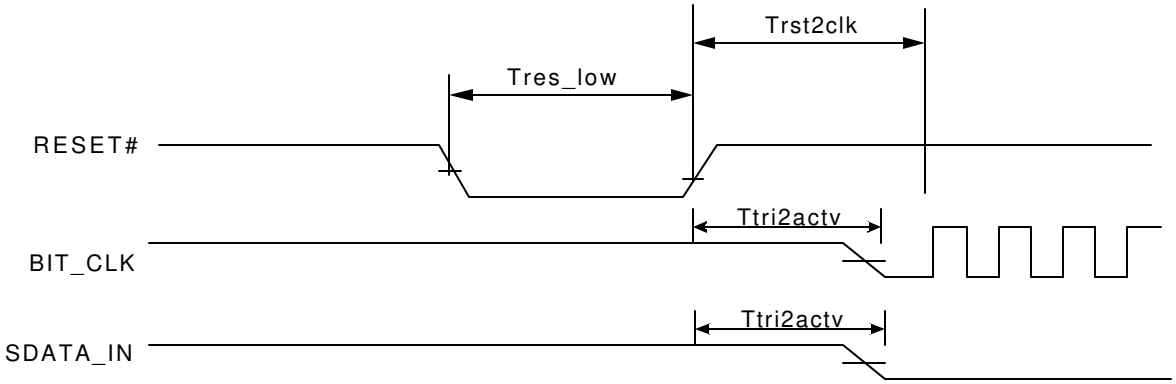


Figure 1. Cold Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Tres_low	1.0	-	-	µs
RESET# inactive to SDATA_IN or BIT_CLK active delay	Tri2actv	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	Trst2clk	0.1628	-	400	µs
BIT_CLK active to RESET# asserted	Tclk2rst	0.416	-	-	µs

Note: BIT_CLK and SDATA_IN are in a high impedance state during reset.

2.2.2. Warm Reset

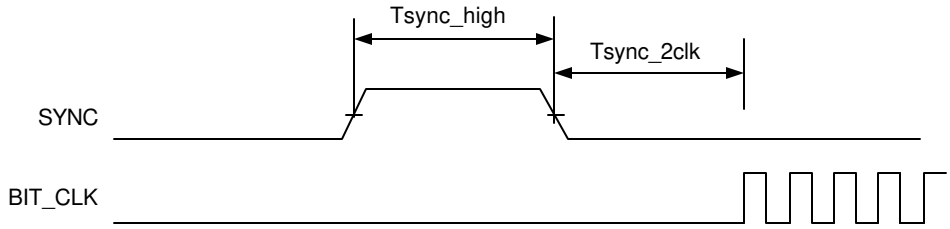


Figure 2. Warm Reset Timing

Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tsync_high	1.0	1.3	-	µs
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

2.2.3. Clocks

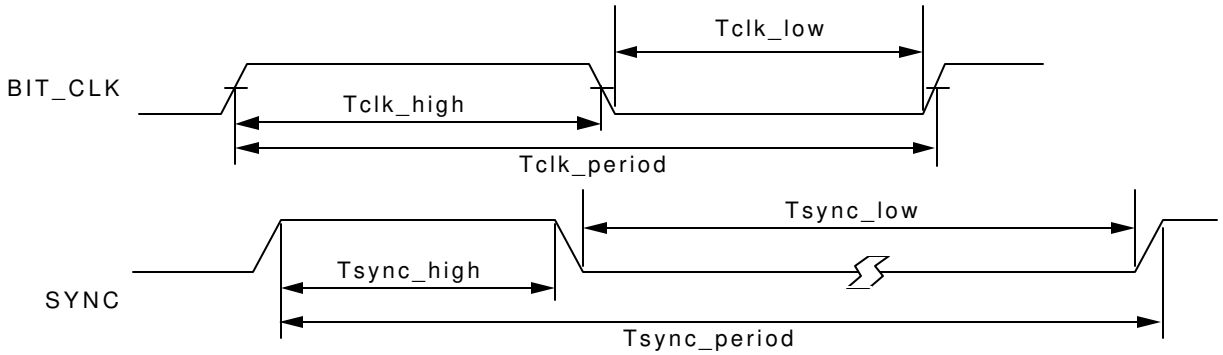


Figure 3. Clocks Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	750	-	ps
BLT_CLK high pulse width (Note Note:)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (Note Note:)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	Tsync_period	-	20.8	-	µs
SYNC high pulse width	Tsync_high	-	1.3	-	µs
SYNC low_pulse width	Tsync_low	-	19.5	-	µs

Note: 1) Worst case duty cycle restricted to 45/55.

2.2.4. STAC9758/9759 Crystal Elimination Circuit and Clock Frequencies

The STAC9758/9759 supports several clock frequency inputs as described in the following table. In general, when a 24.576MHz crystal is not used, the XTL_OUT pin should be tied to ground. This short to ground configures the part into an alternate clock mode and enables an on board PLL.

CODEC Modes:

P = The STAC9758/9759 as a Primary CODEC

S = The STAC9758/9759 as a Secondary CODEC

Table 1. Clock Mode Configuration

XTL_OUT pin config	CID1 pin config	clock source input	CODEC mode	CODEC ID
XTAL	float	24.576 MHz crystal	P	0
short to ground	float	14.31818 MHz source	P	0
short to ground	pulldown	48 MHz source	P	0
XTAL or open	pulldown	12.288 MHz BIT_CLK	S	2

Whenever pin 3 is pulled down, the CODEC will be in primary mode with the CODEC ID 00 regardless of the state of CID1 pin. The only secondary mode operation available is with external device sourcing BIT_CLK and CODEC ID = 2.

Table 2. Common Clocks and Sources

Clock Source	Clock Frequency
XTAL	24.576 MHz
BIT_CLK	12.288 MHz
VGA	14.31818 MHz
USB	48 MHz

Note: 1) Pin #2 (XTL_IN) may be left unconnected if CODEC is in secondary mode.

2.2.5. Data Setup and Hold

(50 pF external load)

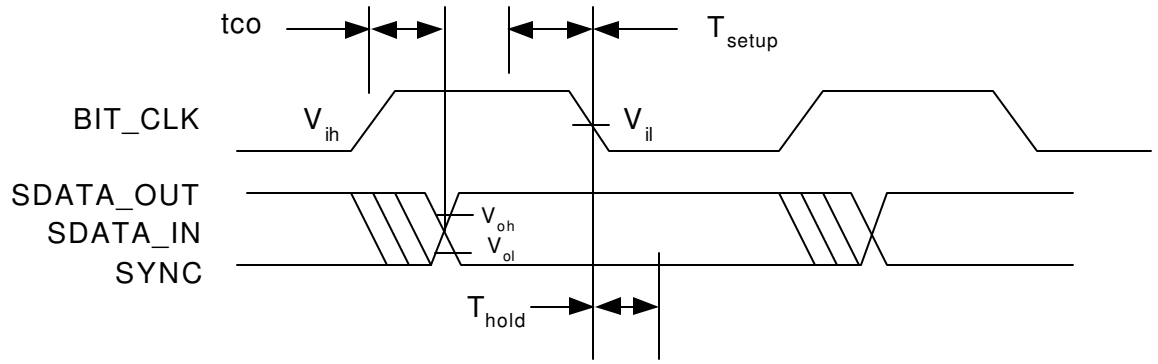


Figure 4. Data Setup and Hold Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	10	-	-	ns
Hold from falling edge of BIT_CLK	Thold	10	-	-	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

2.2.6. Signal Rise and Fall Times

(BIT_CLK: 75 pF external load; from 10% to 90% of Vdd)

(SDATA_IN: 60 pF external load; from 10% to 90% of Vdd))

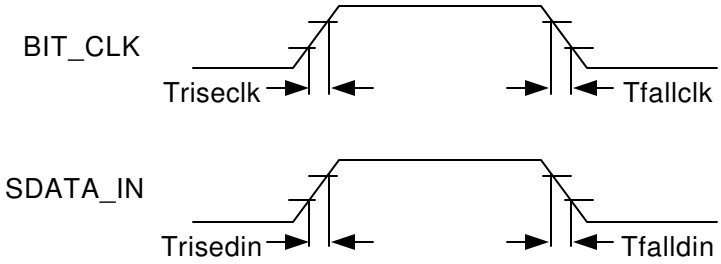


Figure 5. Signal Rise and Fall Times Timing

Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	Triseclk	-	-	6	ns
BIT_CLK fall time	Tfallclk	-	-	6	ns
SDATA_IN rise time	Trisedin	-	-	6	ns
SDATA_IN fall time	Tfalldin	-	-	6	ns

2.2.7. AC-Link Low Power Mode Timing

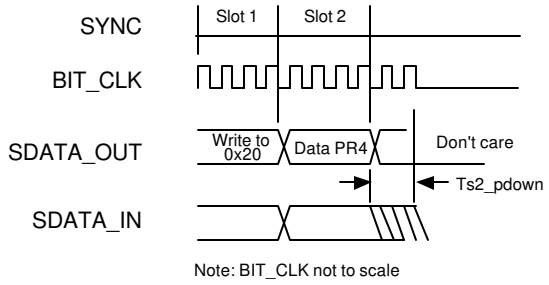


Figure 6. AC-Link Low Power Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	µs

2.2.8. ATE Test Mode

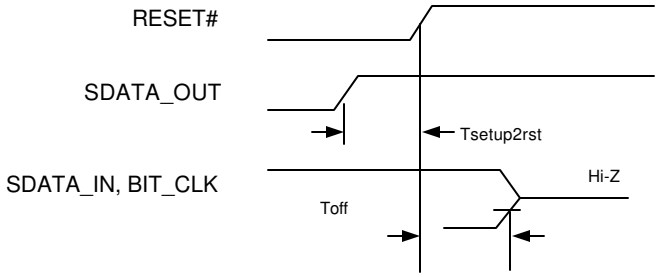


Figure 7. ATE Test Mode Timing

Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

Note: All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes the STAC9758/9759 AC-Link outputs to go high impedance, which is suitable for ATE in-circuit testing.

Once the test mode has been entered, the STAC9758/9759 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.

Note: # denotes an active low signal.

3. TYPICAL CONNECTION DIAGRAM

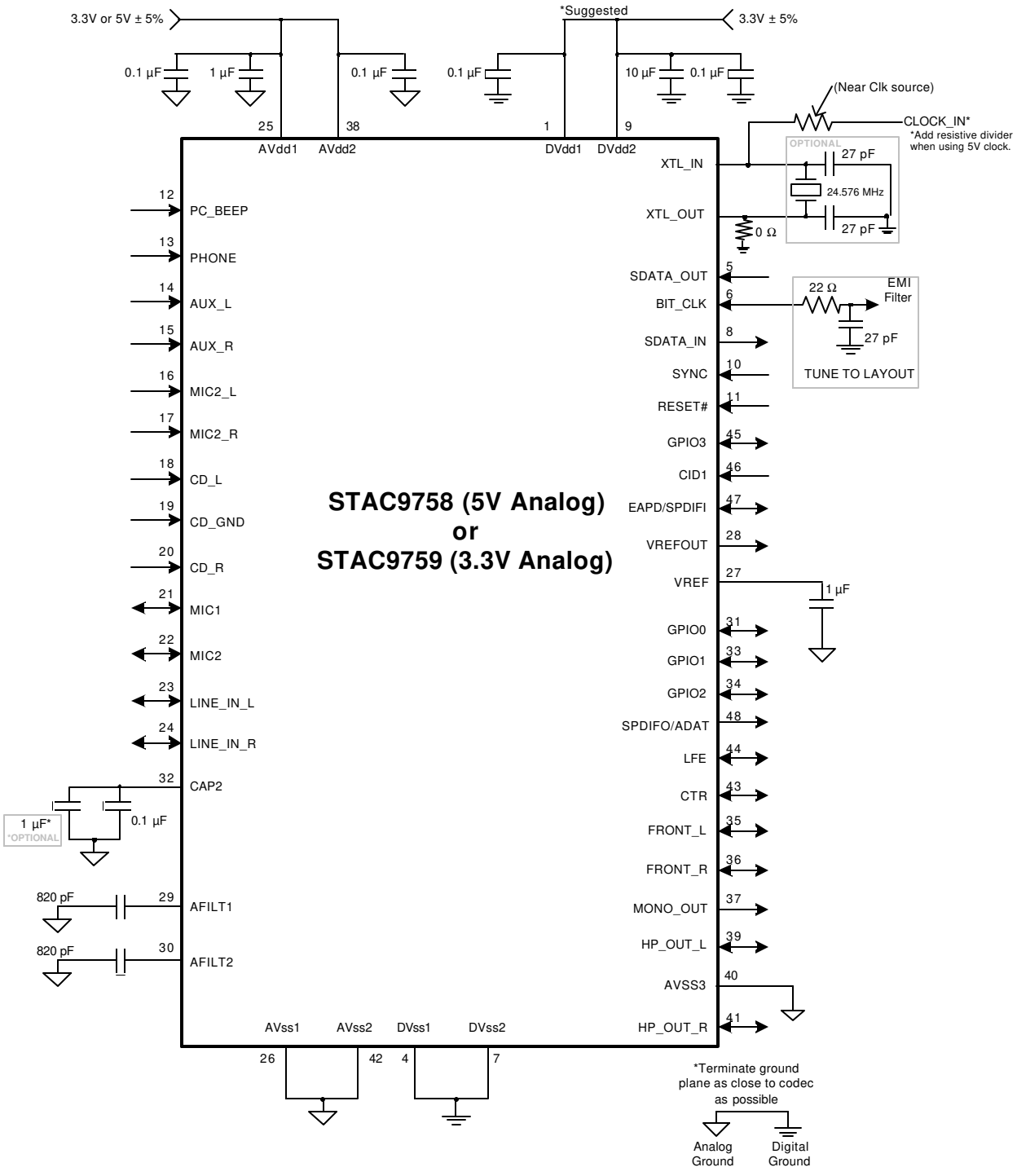


Figure 8. Typical Connection Diagram

See the Reference Design for additional connection information.

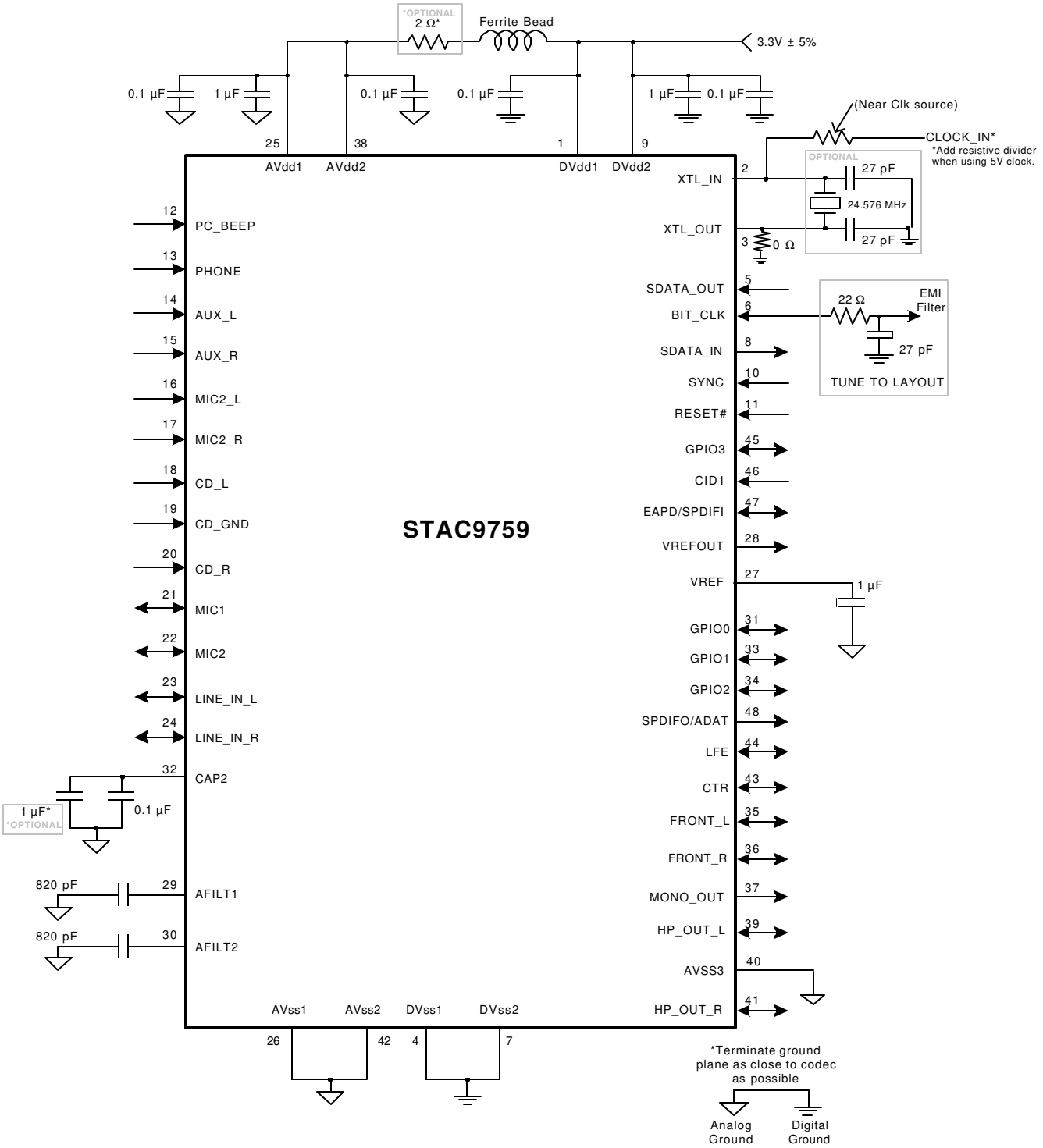
NOTE: If pin 48 is held high at powerup, register 28h (Extended Audio ID), bit [2] will be held to zero, to indicate the SPDIF is not available. Tie pin 48 to ground with a 10 KΩ resistor to ensure SPDIF is enabled.

3.1. Split Independent Power Supply Operation

In PC applications, one power supply input to the STAC9758/9759 may be derived from a supply regulator and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's CODECs would be subject to on-chip SCR type latch-up.

IDT's STAC9758/9759 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the CODEC. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up. See the Reference Design for additional connection information.

Figure 9. Split Independent Power Supply Operation



NOTE: If pin 48 is held high at powerup, register 28h (Extended Audio ID), bit [2] will be held to zero, to indicate the SPDIF is not available. Tie pin 48 to ground with a 10 KΩ resistor to ensure SPDIF is enabled.

4. CONTROLLER, CODEC AND AC-LINK

This section describes the physical and high-level functional aspects of the AC'97 Controller to CODEC interface, referred to as AC-Link.

4.1. AC-Link Physical interface

The STAC9758/9759 communicates with its companion Digital Controller via the AC-Link digital serial interface. AC-Link has been defined to support connections between a single Controller and up to four CODECs. All digital audio, modem, and handset data streams, as well as all control (command/status) information are communicated over this serial interconnect, which consists of a clock (BIT_CLK), frame synchronization (SYNC), serial data in (SDATA_IN), serial data out (SDATA_OUT), and a reset (RESET#).

4.2. Controller to Single CODEC

The simplest and most common AC'97 system configuration is a point-to-point AC-Link connection between Controller and the STAC9758/9759, as illustrated in Figure 10.

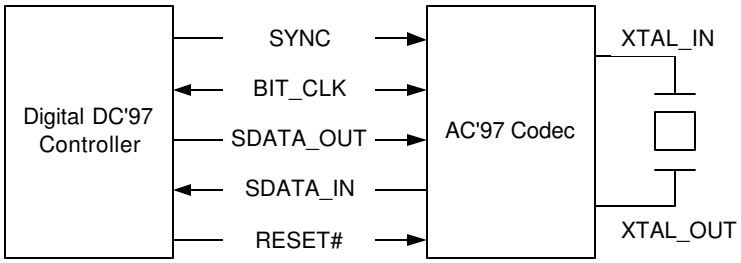


Figure 10. AC-Link to its Companion Controller

A primary CODEC may act as either a source or a consumer of the bit clock, depending on the configuration.

While RESET# is asserted, if a clock is present at the BIT_CLK pin for at least five cycles before RESET# is de-asserted, then the CODEC is a consumer of BIT_CLK, and must not drive BIT_CLK when RESET# is de-asserted. The clock is being provided by other than the primary CODEC, for instance by the controller or an independent clock chip. In this case the primary CODEC must act as a consumer of the BIT_CLK signal as if it were a secondary CODEC.

This clock source detection must be done each time the RESET# line is asserted. In the case of a warm reset, where the clock is halted but RESET# is not asserted, the CODEC must remember the clock source, and not begin generating the clock on the assertion of SYNC if the CODEC had previously determined that it was a consumer of BIT_CLK.