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TWO-CHANNEL, 20-BIT, AC'97 2.3 CODECS WITH STEREO MICROPHONE AND MIC/JACK SENSING

STAC9766/9767

FEATURES

- **This datasheet is for Rev. CC1 Parts and Beyond**
- **High Performance ΣΔ Technology**
- **AC'97 Rev 2.3 Complaint**
- **20-bit Full Duplex Stereo ADC & DACs**
- **Independent Sample Rates for ADC & DACs**
- **5-Wire AC-Link Protocol Compliance**
- **20-bit SPDIF Output**
- **Full Stereo Microphone Pre-Amp**
- **Internal Jack Sensing on Headphone & Line_Out**
- **Internal Microphone Input Sensing**
- **Digital PC Beep Option**
- **Extended AC'97 2.3 Paging Registers**
- **Digital-ready Status**
- **General Purpose I/O**
- **Crystal Elimination Circuit**
- **Headphone Drive Capability (50 mW)**
- **0dB, 10dB, 20dB and 30dB Microphone Boost Capability**
- **+3.3 V (STAC9767) and +5 V (STAC9766) Analog Power Supply Options**
- **Pin Compatible with STAC9700/21/56**
- **100% Compatible with STAC9750/52**
- **IDT Surround (SS3D) Stereo Enhancement**
- **Energy Saving Dynamic Power Modes**
- **Multi-CODEC Option (Intel AC'97 rev 2.3)**
- **Six Analog Line-level Inputs**
- **103dB SNR LINE-LINE**

KEY SPECIFICATIONS

- **Analog LINE_OUT SNR: 103 dB**
- **Digital DAC SNR: 95 dB**
- **Digital ADC SNR: 85 dB**
- **Full-scale Total Harmonic Distortion: 0.002%**
- **Crosstalk Between Input Channels: -70 dB**
- **Spurious Tone Rejection: 100 dB**

RELATED MATERIALS

- **Data Sheet**
- **Reference Designs**

DESCRIPTION

IDT's STAC9766/9767 (Revision CC1 and beyond) are general purpose 20-bit, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio CODEC 97 Component Specification Rev. 2.3).

The STAC9766/9767 incorporates IDT's proprietary ΣΔ technology The AC'97 CODEC is designed to achieve a DAC SNR in excess of 103dB.

The DACs, ADCs and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. The STAC9766/9767 includes digital input/output capability for support of modern PC systems with an output that supports the SPDIF format.

The STAC9766/9767 is a standard 2-channel stereo CODEC. With IDT's headphone drive capability, headphones can be driven with without an external amplifier.

The STAC9766/9767 may be used as a secondary CODEC, with the STAC9700/21/56/08/84/50/52 as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.3 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications.

The STAC9766/9767 communicates via the five-wire AC-Link to any digital component of AC'97, providing flexibility in the audio system design.

Packaged in an AC'97 compliant 48-pin TQFP, the STAC9766/9767 can be placed on a motherboard, daughter boards, PCI, AMR, CNR, MDC or ACR cards.

The STAC9766/9767 provides variable sample rate Digital-to-Analog (DA) and Analog-to-Digital (AD) conversion, mixing and analog processing.

Supported audio sample rates include 48KHz, 44.1KHz, 32KHz, 22.05KHz, 16KHz, 11.025KHz, and 8 KHz; additional rates are supported in the STAC9766/9767 soft audio drivers. All ADCs and DACs operate at 20-bit resolution.

The STAC9766/9767 includes *full Stereo Microphone*

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1. PRODUCT BRIEF

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- AC'97 Rev 2.3 Complaint
- 20-bit Full Duplex Stereo ADCs, DACs
- Independent Sample Rates for ADCs & DACs
- 5-Wire AC-Link Protocol Compliance
- 20-bit SPDIF Output
- Full Stereo Microphone Pre-Amp
- Internal Jack Sensing on Headphone and Line_Out
- Internal Microphone Input Sensing
- Digital PC Beep Option
- Extended AC'97 2.3 Paging Registers
- Adjustable VREF Amplifier
- Digital-ready Status
- General Purpose I/Os
- Crystal Elimination Circuit
- Headphone Drive Capability (50 mW)
- 0dB, 10dB, 20dB, and 30dB Stereo or Mono Microphone Boost Capability
- +3.3V (STAC9767) and +5V (STAC9766) Analog Power Supply Options
- Pin Compatible with the STAC9700, STAC9721, STAC9756
- 100% Pin Compatible with STAC9750 and STAC9752
- IDT Surround (SS3D) Stereo Enhancement
- Energy Saving Dynamic Power Modes
- Multi-CODEC option (Intel AC'97 rev 2.3)
- Six Analog Line-level Inputs
- 103dB SNR LINE-LINE

1.2. Description

IDT's STAC9766/9767 (Revision CC1 and beyond) are general purpose 20-bit, full duplex, audio CODECs conforming to the analog component specification of AC'97 (Audio CODEC 97 Component Specification Rev. 2.3). The STAC9766/9767 incorporates IDT's proprietary ΣΔ technology to achieve a DAC SNR in excess of 103dB. The DACs, ADCs and mixer are integrated with analog I/Os, which include four analog line-level stereo inputs, two analog line-level mono inputs, two stereo outputs, and one mono output channel. The STAC9766/9767 includes digital output capability for support of modern PC systems with an output that supports the SPDIF format. The STAC9766/9767 is a standard 2-channel stereo CODEC. With IDT's headphone drive capability, headphones can be driven without an external amplifier. The STAC9766/9767 may be used as a secondary CODEC, with the STAC9700/21/44/56/08/84/50/66 as the primary, in a multiple CODEC configuration conforming to the AC'97 Rev. 2.3 specification. This configuration can provide the true six-channel, AC-3 playback required for DVD applications. The STAC9766/9767 communicates via the five-wire

AC-Link to any digital component of AC'97 providing flexibility in the audio system design. Packaged in an AC'97 compliant 48-pin TQFP, the STAC9766/9767 can be placed on a motherboard, daughter boards, PCI, AMR, CNR, MDC or ACR cards.

The STAC9766/9767 block diagram is illustrated in Figure 1. It provides variable sample rate Digital-to-Analog (DA) and Analog-to-Digital (AD) conversion, mixing, and analog processing. Supported audio sample rates include 48KHz, 44.1KHz, 32 KHz, 22.05KHz, 16KHz, 11.025KHz, and 8KHz; additional rates are supported in the STAC9766/9767 soft audio drivers. All ADCs and DACs operate at 20-bit resolution.

Two 20-bit DACs convert the digital stereo PCM-out content to audio. The MIXER block combines the PCM_OUT with any analog sources to drive the LINE_OUT and HP_OUT outputs. The MONO_OUT delivers either microphone only, or a mono mix of sources from the MIXER. The stereo variable sample rate 20-bit ADCs provide record capability for any mix of mono or stereo sources, and deliver a digital stereo PCM-in signal back to the AC-Link. The microphone input and mono mix input can be recorded simultaneously, thus allowing for an all digital output in support of the digital ready initiative. For a digital ready record path, the microphone is connected to the left channel ADC while the mono output of the stereo mixer is connected to right channel ADC.

The STAC9766/9767 includes full Stereo Microphone Pre-Amp support and can be used with the 10dB, 20dB and 30dB Microphone Boost options. This integration allows for additional cost savings and options.

The STAC9766/9767 includes jack sensing on the Headphone and Line_Out. The STAC9766/9767 jack sense can detect the presence of devices on the Headphone and Line Outputs and on both Mic inputs. With proprietary IDT current- and impedance-sensing techniques, the impedance load on the Headphone and Line Outputs can also be detected. The GPIOs on the STAC9766/9767 remain available for advanced configurations.

The STAC9766/9767 implementation of jack sense uses the Extended Paging Registers defined by the AC'97 2.3 Specification. This allows for additional registry space to hold the identification information about the CODEC, the jack sensing details and results, and the external surroundings of the CODEC. The information within the Extended Paging Registers will allow for the automatic configuration of the audio subsystem without end-user intervention. For example, the BIOS can populate the Extended Paging Registers with valuable information for both the audio driver and the operating system such as gain and attenuation stages, input population and input phase. With this input information, the IDT driver will automatically provide to the Volume Control Panel only the volume sliders that are implemented in the system, thus improving the end-user's experience with the PC.

The information in the Extended Paging Registers will also allow for automatic configuration of microphone inputs, the ability to switch between SPDIF and analog outputs, the routing of the master volume slider to the proper physical output, and SoftEQ configurations. The fully parametric IDT SoftEQ can be initiated upon jack insertion and sensed impedance levels.

The STAC9766/9767 also offers two styles of PC BEEP, Analog and Digital. The digital PC BEEP is a new feature added to the AC'97 Specification Rev 2.3.

The STAC9766/9767 is designed primarily to support stereo (2-speaker) audio. True AC-3 playback can be achieved for 6-speaker applications by taking advantage of the multi-CODEC option available in the STAC9766/9767 to support multiple CODECs in an AC'97 architecture. Additionally, the

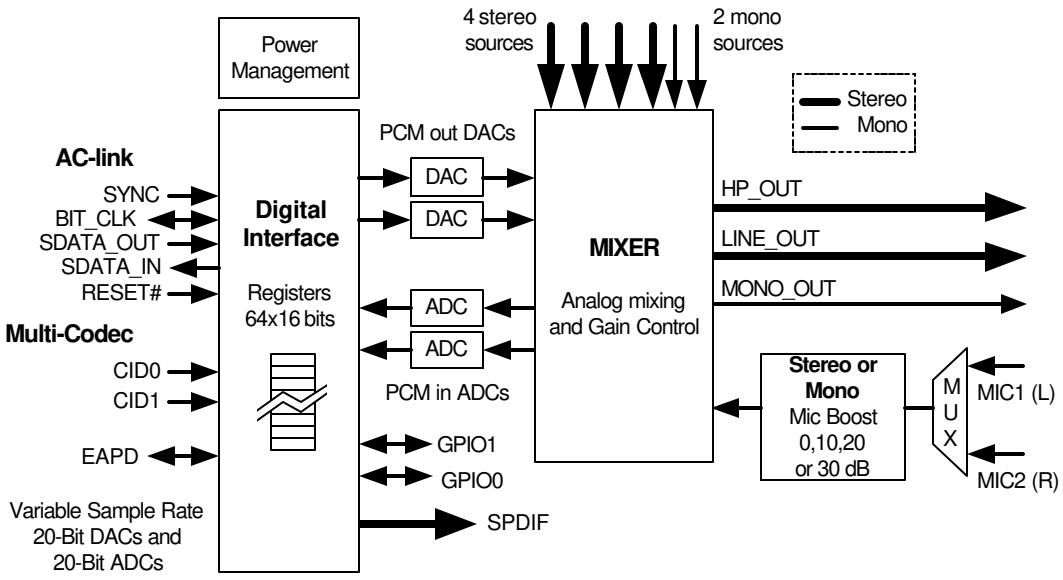
STAC9766/9767 provides for a stereo enhancement feature, IDT Surround 3D (SS3D). SS3D provides the listener with several options for improved speaker separation beyond the normal 2- or 4-speaker arrangements.

The STAC9766/9767 can be SoundBlaster® and Windows Sound System® compatible when used with IDT's WDM driver for Windows 98/2K/ME/XP or with Intel/Microsoft driver included with Windows 2K/ME/XP.

SoundBlaster is a registered trademark of Creative Labs.
Windows is a registered trademark of Microsoft Corporation.

1.3. STAC9766/9767 Block Diagram

Figure 1. Block Diagram



1.4. Key Specifications

- Analog LINE_OUT SNR: 103 dB
- Digital DAC SNR: 95 dB
- Digital ADC SNR: 85 dB
- Full-scale Total Harmonic Distortion: 0.002%
- Crosstalk between Input Channels: -70 dB
- Spurious Tone Rejection: 100 dB

1.5. Related Materials

- Product Brief
- Reference Designs for MB, AMR, CNR, and ACR applications
- Audio Precision Performance Plots

1.6. Additional Support

Additional product and company information can be obtained by going to the IDT web site at: www.IDT.com

2. CHARACTERISTICS AND SPECIFICATIONS

2.1. Electrical Specifications

2.1.1. Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the STAC9766/9767. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Pin	Maximum Rating
Analog maximum supply voltage	AVdd	6 Volts
Digital maximum supply voltage	DVdd	5.5 Volts
VREFOUT output current		5 mA
Voltage on any pin relative to ground		Vss - 0.3 V to Vdd + 0.3 V
Operating temperature		0°C to +70°C
Storage temperature		-55 °C to +125 °C
Soldering temperature		260 °C for 10 seconds * Soldering temperature information for all available packages begins on page 92.

2.1.2. Recommended Operation Conditions

Parameter		Min.	Typ.	Max.	Units
Power Supply Voltage	Digital - 3.3 V	3.135	3.3	3.465	V
	Analog - 3.3 V	3.135	3.3	3.465	V
	Analog - 5 V	4.75	5	5.25	V
Ambient Operating Temperature		0		+70	°C
Case Temperature	T_{case} (48-LQFP)			+90	°C

ESD: The STAC9766/9767 is an ESD (electrostatic discharge) sensitive device. The human body and test equipment can accumulate and discharge electrostatic charges up to 4000 Volts without detection. Even though the STAC9766/9767 implements internal ESD protection circuitry, proper ESD precautions should be followed to avoid damaging the functionality or performance.

2.1.3. Power Consumption

Parameter	Min	Typ	Max	Unit
Digital Supply Current				
+ 3.3V Digital	-	35	-	mA
Analog Supply Current				
+ 5V Analog	-	80	-	mA
+ 3.3V Analog	-	70	-	mA
Power Down Status				
PR0 Supply Current	-	TBD	-	mA
PR1 Supply Current	-	TBD	-	mA
PR2 Supply Current	-	TBD	-	mA
PR3 Supply Current	-	TBD	-	mA
PR4 Supply Current	-	TBD	-	mA
PR5 Supply Current	-	TBD	-	mA
PR6 Supply Current	-	TBD	-	mA

2.1.4. AC-Link Static Digital Specifications

($T_{ambient}$ = 25 ºC, DVdd = 3.3 V ± 5%, AVss = DVss = 0 V; 50 pF external load)

Parameter	Symbol	Min	Typ	Max	Unit
Input Voltage Range	Vin	-0.30	-	DVdd + 0.30	V
Low level input range	Vil	-	-	0.35 x DVdd	V
High level input voltage	Vih	0.65 x DVdd	-	-	V
High level output voltage	Voh	0.90 x DVdd	-	-	V
Low level output voltage	Vol	-	-	0.1 x DVdd	V
Input Leakage Current (AC-Link inputs)	-	-10	-	10	µA
Output Leakage Current (AC-Link outputs - Hi-Z)	-	-10	-	10	µA
Output buffer drive current	-	-	4	-	mA

2.1.5. STAC9766 Analog Performance Characteristics

($T_{ambient}$ = 25 ºC, AVdd = 5.0 V ± 5%, DVdd = 3.3 V ± 5%, AVss = DVss = 0 V; 1 KHz input sine wave; Sample Frequency = 48 KHz; 0dB = 1 Vrms, 10 KΩ / 50 pF load, Testbench Characterization BW: 20 Hz – 20 KHz, 0dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	1.0	-	Vrms
PCM (DAC) to LINE_OUT		1.0		Vrms
MONO_OUT	-	1.0	-	Vrms
HEADPHONE_OUT (32 Ω load) (peak)	-	50	-	mW
Analog S/N: *(Note 2)*				
CD to LINE_OUT	-	103	-	dB
Other to LINE_OUT	-	103	-	dB

Parameter	Min	Typ	Max	Unit
D/A to LINE_OUT	-	95	-	dB
LINE_IN to A/D with High pass filter enabled	-	85	-	dB
Analog Frequency Response (Note 3)	20	-	20,000	Hz
Total Harmonic Distortion: *(Note 4)*				
CD to LINE_OUT	-	95	-	dB
Other to LINE_OUT	-	95	-	dB
D/A to LINE_OUT (full scale)	-	84	-	dB
LINE_IN to A/D with High pass filter enabled	84	-	-	dB
HEADPHONE_OUT	74	80	-	dB
A/D & D/A Digital Filter Pass Band (Note 5)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 6)	100	-	-	dB
DAC Out-of-Band Rejection (Note 7)	55	-	-	dB
Group Delay (48 KHz sample rate)	-		1	ms
Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency)	70	-	-	dB
Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency)	-	100	-	dB
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance (Note 8)	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 x AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB

Note:
1. With +30 dB Boost on, 1.0 Vrms with Boost off
2. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3. ± 1dB limits for Line Output & 0dB gain
4. 20 KHz BW, 48 KHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.
8. For all inputs except PC BEEP.

2.1.6. STAC9767 Analog Performance Characteristics

($T_{ambient}$ =25ºC, AVdd=3.3V±5%, DVdd=3.3V±5%, AVss=DVss=0V; 1KHzinputsine wave; Sample Frequency=48KHz; 0dB=1Vrms, 10KΩ / 50 pFload, TestbenchCharacterization BW: 20Hz–20KHz, 0dB settings on all gain stages)

Parameter	Min	Typ	Max	Unit
Full Scale Input Voltage:				
All Analog Inputs except Mic	-	1.0	-	Vrms
Mic Inputs (Note 1)	-	0.03	-	Vrms
Full Scale Output:				
Line Output	-	0.5	-	Vrms

Parameter	Min	Typ	Max	Unit
PCM (DAC) to LINE_OUT		0.5		Vrms
MONO_OUT	-	0.5	-	Vrms
HEADPHONE_OUT (32 Ω load) (peak)	-	12.5	-	mW
Analog S/N: *(Note 2)*				
CD to LINE_OUT	-	97	-	dB
Other to LINE_OUT	-	97	-	dB
D/A to LINE_OUT	-	95	-	dB
LINE_IN to A/D with High pass filter enabled	-	85	-	dB
Analog Frequency Response (Note 3)	20	-	20,000	Hz
Total Harmonic Distortion: *(Note 4)*				
CD to LINE_OUT	-	95	-	dB
Other to LINE_OUT	-	95	-	dB
D/A to LINE_OUT (full scale)	-	84	-	dB
LINE_IN to A/D with High pass filter enabled	-	84	-	dB
HEADPHONE_OUT	74	80	-	dB
A/D & D/A Digital Filter Pass Band (Note 5)	20	-	19,200	Hz
A/D & D/A Digital Filter Transition Band	19,200	-	28,800	Hz
A/D & D/A Digital Filter Stop Band	28,800	-	-	Hz
A/D & D/A Digital Filter Stop Band Rejection (Note 6)	100	-	-	dB
DAC Out-of-Band Rejection (Note 7)	55	-	-	dB
Group Delay (48 KHz sample rate)	-	-	1	ms
Any Analog Input to LINE_OUT Crosstalk (10 KHz Signal Frequency)	70	-	-	dB
Any Analog Input to LINE_OUT Crosstalk (1 KHz Signal Frequency)	-	100	-	dB
Spurious Tone Rejection	-	100	-	dB
Attenuation, Gain Step Size	-	1.5	-	dB
Input Impedance (Note 8)	-	50	-	KΩ
Input Capacitance	-	15	-	pF
VREFout	-	0.5 X AVdd	-	V
Interchannel Gain Mismatch ADC	-	-	0.5	dB
Interchannel Gain Mismatch DAC	-	-	0.5	dB
Gain Drift	-	100	-	ppm/ºC

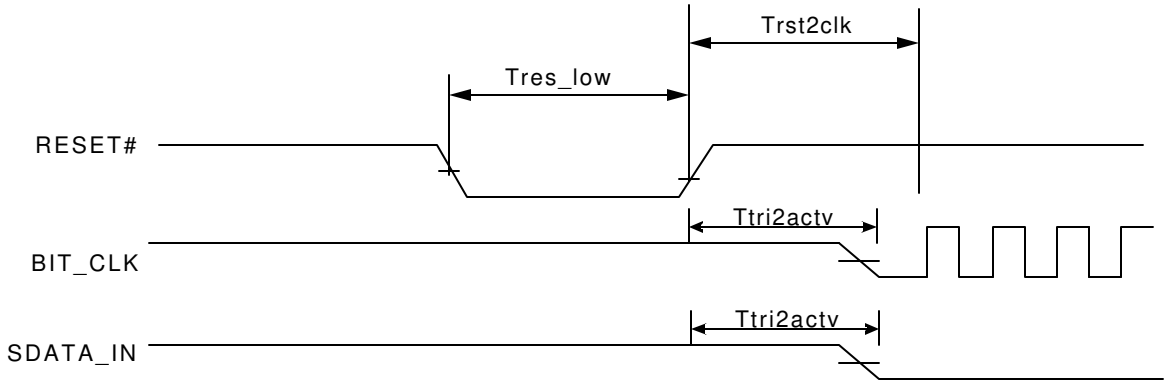
Note:
1. With +30 dB Boost on, 1.0Vrms with Boost off
2. Ratio of Full Scale signal to idle channel noise output is measured "A weighted" over a 20 Hz to a 20 KHz bandwidth. (AES17-1991 Idle Channel Noise or EIAJ CP-307 Signal-to-noise Ratio).
3. ± 1dB limits for Line Output & 0 dB gain
4. 20 KHz BW, 48 KHz Sample Frequency
5. ± 0.25dB limits
6. Stop Band rejection determines filter requirements. Out-of-Band rejection determines audible noise.
7. The integrated Out-of-Band noise generated by the DAC process, during normal PCM audio playback, over a bandwidth 28.8 to 100 KHz, with respect to a 1 Vrms DAC output.
8. For all inputs except PC BEEP.

2.2. AC Timing Characteristics

($T_{ambient}$ = 25 °C, AVdd = 3.3 V or 5 V ± 5%, DVdd = 3.3V ± 5%, AVss = DVss = 0 V; 75 pF external load for BIT_CLK and 60pF external load for SDATA_IN)

2.2.1. Cold Reset

Figure 2. Cold Reset Timing

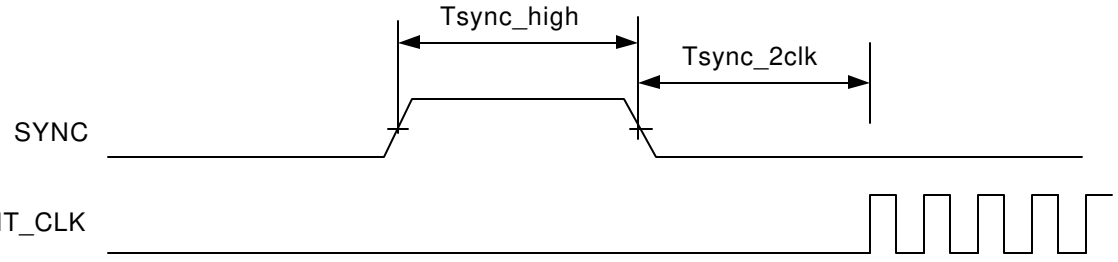


Parameter	Symbol	Min	Typ	Max	Units
RESET# active low pulse width	Tres_low	1.0	-	-	µs
RESET# inactive to SDATA_IN or BIT_CLK active delay	Tri2actv	-	-	25	ns
RESET# inactive to BIT_CLK startup delay	Trst2clk	0.01628	-	400	µs
BIT_CLK active to RESET# asserted (Not shown in diagram)	Tclk2rst	0.416	-	-	µs

Note: BIT_CLK and SDATA_IN are in a high impedance state during reset.

2.2.2. Warm Reset

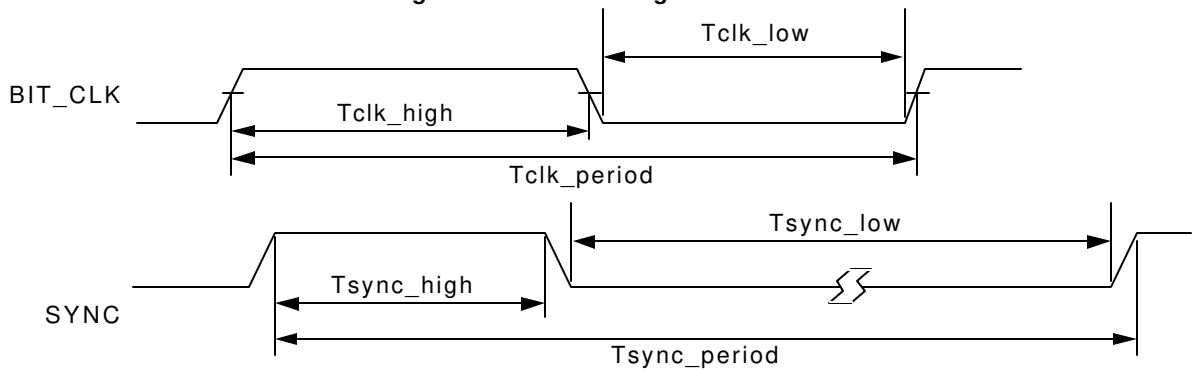
Figure 3. Warm Reset Timing



Parameter	Symbol	Min	Typ	Max	Units
SYNC active high pulse width	Tsync_high	1.0	1.3	-	µs
SYNC inactive to BIT_CLK startup delay	Tsync2clk	162.8	-	-	ns

2.2.3. Clocks

Figure 4. Clocks Timing



Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK frequency		-	12.288	-	MHz
BIT_CLK period	Tclk_period	-	81.4	-	ns
BIT_CLK output jitter		-	750	-	ps
BLT_CLK high pulse width (Note 1)	Tclk_high	36	40.7	45	ns
BIT_CLK low pulse width (Note 1)	Tclk_low	36	40.7	45	ns
SYNC frequency		-	48.0	-	KHz
SYNC period	Tsync_period	-	20.8	-	µs
SYNC high pulse width	Tsync_high	-	1.3	-	µs
SYNC low pulse width	Tsync_low	-	19.5	-	µs

Note: 1. Worst case duty cycle restricted to 45/55.

2.2.4. STAC9766/9767 Crystal Elimination Circuit and Clock Frequencies

The STAC9766/9767 supports several clock frequency inputs as described in the following table. In general, when a 24.576 MHz xtal is not used, the XTALOUT pin should be tied to ground. This short to ground configures the part into an alternate clock mode and enables an on board PLL.

CODEC Modes:

P = The STAC9766/9767 as a Primary CODEC
S = The STAC9766/9767 as a Secondary CODEC.

Table 1. Clock Mode Configuration

XTL_OUT Pin Config	CID1 Pin Config	CID0 Pin Config	Clock Source Input	CODEC Mode	CODEC D
XTAL	float	float	24.576MHz crystal	P	0
XTAL or open	float	pulldown	12.288 MHz BIT_CLK	S	1
XTAL or open	pulldown	float	12.288 MHz BIT_CLK	S	2
XTAL or open	pulldown	pulldown	12.288 MHz BIT_CLK	S	3
short to ground	float	float	14.31818 MHz source	P	0
short to ground	float	pulldown	27 MHz source	P	0
short to ground	pulldown	float	48 MHz source	P	0
short to ground	pulldown	pulldown	24.576 MHz source	P	0

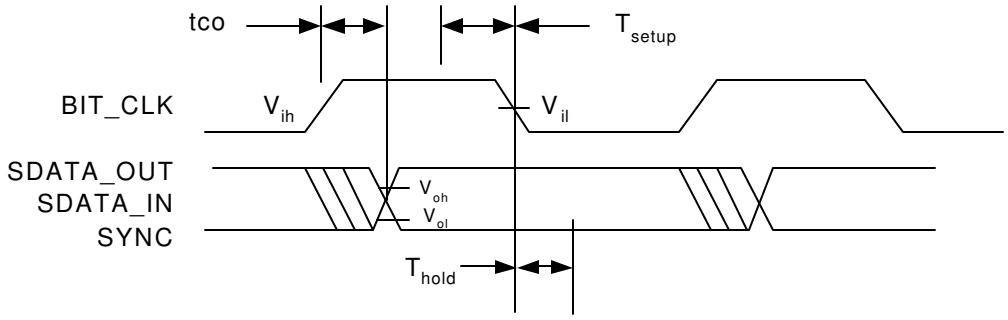
Table 2. Common Clocks and Sources

Clock Source	Clock Frequency
XTAL	24.576MHz
BIT_CLK	12.288MHz
VGA	14.31818MHz
Digital Video	27MHz
USB	48MHz

2.2.5. Data Setup and Hold

(50pF external load)

Figure 5. Data Setup and Hold Timing



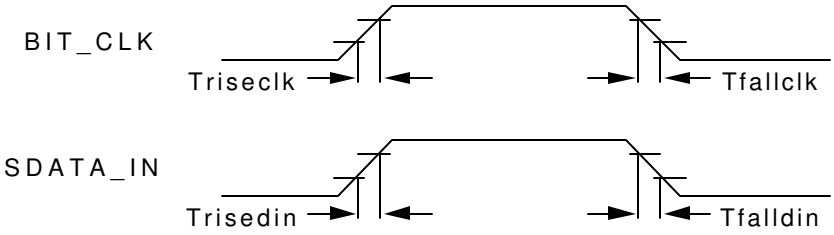
Parameter	Symbol	Min	Typ	Max	Units
Setup to falling edge of BIT_CLK	Tsetup	10	-	-	ns
Hold from falling edge of BIT_CLK	Thold	10	-	-	ns
Output Valid Data from rising edge of BIT_CLK	tco	-	-	15	ns

Note: Setup and hold time parameters for SDATA_IN are with respect to the AC'97 controller.

2.2.6. Signal Rise and Fall Times

(BIT_CLK: 75pF external load; from 10% to 90% of Vdd)
(SDATA_IN: 60pF external load; from 10% to 90% of Vdd)

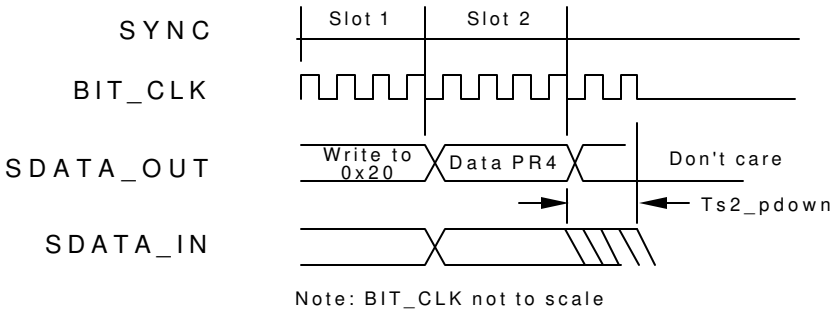
Figure 6. Signal Rise and Fall Times Timing



Parameter	Symbol	Min	Typ	Max	Units
BIT_CLK rise time	Triseclk	-	-	6	ns
BIT_CLK fall time	Tfallclk	-	-	6	ns
SDATA_IN rise time	Trisedin	-	-	6	ns
SDATA_IN fall time	Tfalldin	-	-	6	ns

2.2.7. AC-Link Low Power Mode Timing

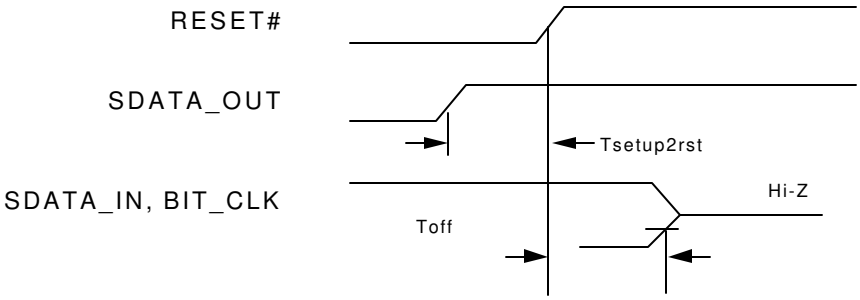
Figure 7. AC-Link Low Power Mode Timing



Parameter	Symbol	Min	Typ	Max	Units
End of Slot 2 to BIT_CLK, SDATA_IN low	Ts2_pdown	-	-	1.0	µs

2.2.8. ATE Test Mode

Figure 8. ATE Test Mode Timing



Parameter	Symbol	Min	Typ	Max	Units
Setup to trailing edge of RESET# (also applies to SYNC)	Tsetup2rst	15.0	-	-	ns
Rising edge of RESET# to Hi-Z delay	Toff	-	-	25.0	ns

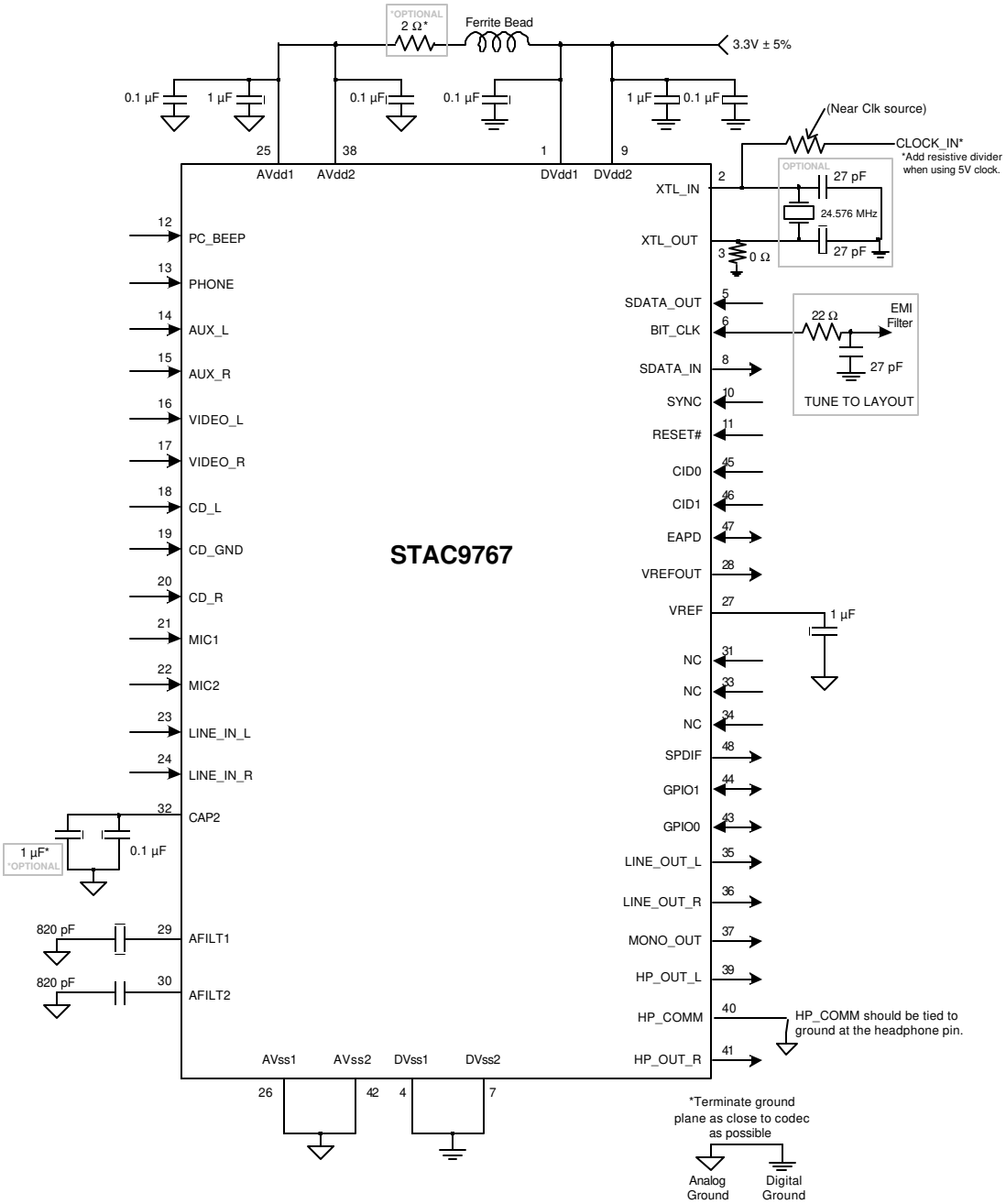
Note: 1) All AC-Link signals are normally low through the trailing edge of RESET#. Bringing SDATA_OUT high for the trailing edge of RESET# causes the STAC9766/9767 AC-Link outputs to go high-impedance, which is suitable for ATE in-circuit testing.

Note: 2) Once the test mode has been entered, the STAC9766/9767 must be issued another RESET# with all AC-Link signals low to return to the normal operating mode.

Note: 3) # denotes active low.

3. TYPICAL CONNECTION DIAGRAM

Figure 9. Typical Connection Diagram



Pin 48: To Enable SPDIF, use a 1KΩ - 10 KΩ external pulldown. To Disable SPDIF, use a 1KΩ - 10 KΩ external pullup. Do NOT leave Pin 48 floating.

The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause significant distortion. If there is no analog CD input, then this pin can be No-Connect.

3.1. Split Independent Power Supply Operation

In PC applications, one power supply input to the STAC9766/9767 may be derived from a supply regulator and the other directly from the PCI power supply bus. When power is applied to the PC, the regulated supply input to the IC will be applied some time delay after the PCI power supply. Without proper on-chip partitioning of the analog and digital circuitry, some manufacturer's CODECs would be subject to on-chip SCR type latch-up.

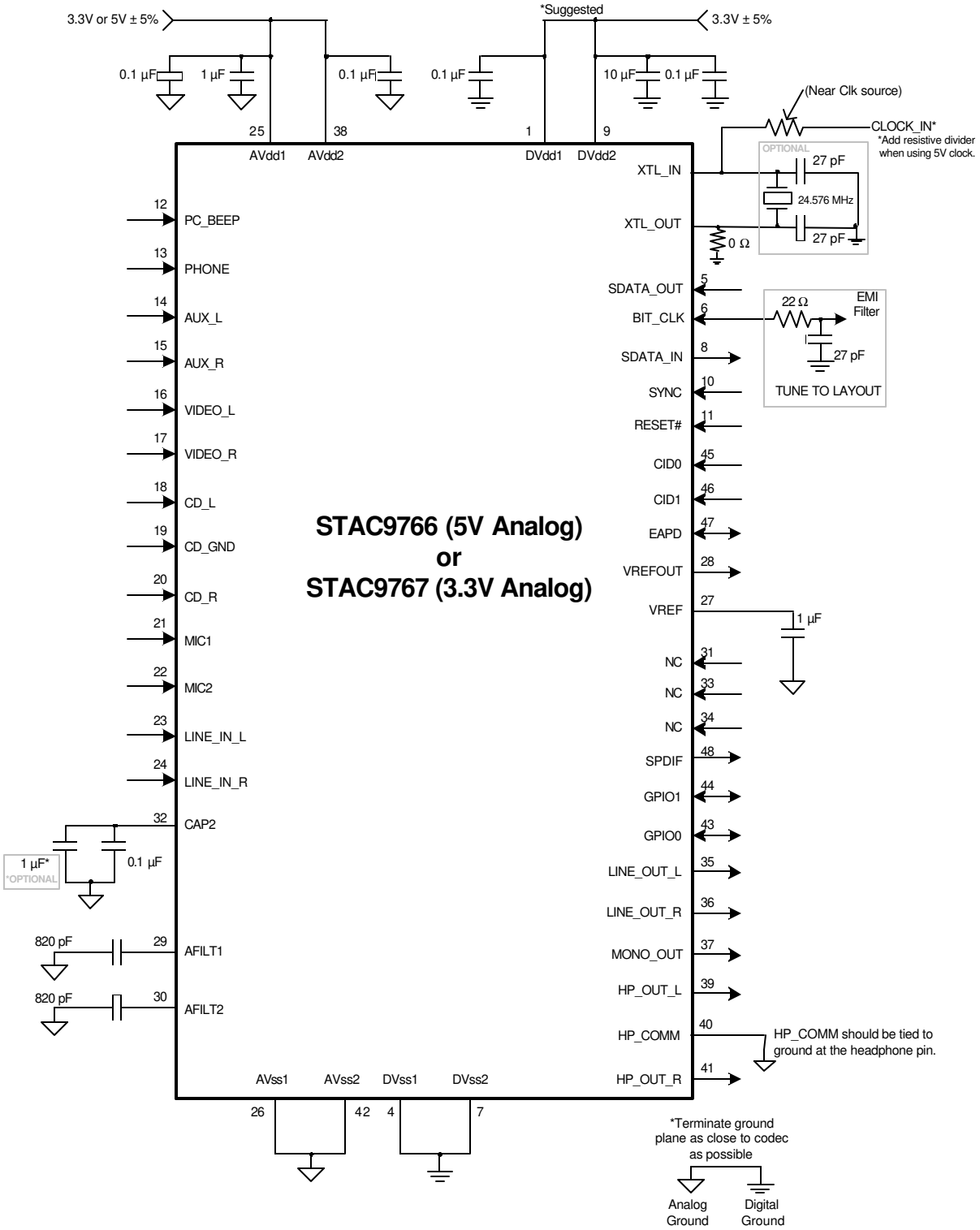
IDT's STAC9766/9767 specifically allows power-up sequencing delays between the analog (AVddx) and digital (VDddx) supply pins. These two power supplies can power-up independently and at different rates with no adverse effects to the CODEC. The IC is designed with independent analog and digital circuitry that prevents on-chip SCR type latch-up.

However, the STAC9766/9767 is not designed to operate for extended periods with only the analog supply active.

Note: Pin 48: To Enable SPDIF, use a 1 KΩ - 1 0 KΩ external pulldown. To Disable SPDIF, use a 1 KΩ - 1 0 KΩ external pullup. Do NOT leave Pin 48 floating.

Note: The CD_GND signal is an AC signal return for the two CD input channels. It is normally biased at about 2.5V. The name of the pin in the AC97 specification is CD_GND, and this has confused many designers. It should not have any DC path to GND. Connecting the CD_GND signal directly to ground will change the internal bias of the entire CODEC, and cause significant distortion. If there is no analog CD input, then this pin can be No-Connect.

Figure 10. Split Independent Power Supply Operation



4. CONTROLLER, CODEC AND AC-LINK

This section describes the physical and high-level functional aspects of the AC'97-Controller to CODEC interface, referred to as AC-link.

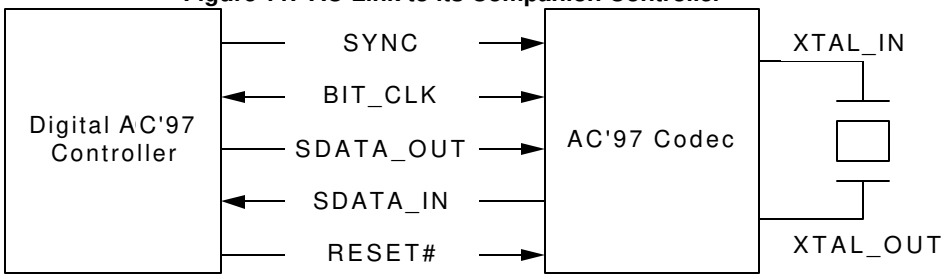
4.1. AC-link Physical interface

The STAC9766/9767 communicates with its companion Digital Controller via the AC-link digital serial interface. AC-link has been defined to support connections between a single Controller and up to four CODECs. All digital audio, modem, and handset data streams, as well as all control (command/status) information are communicated over this serial interconnect, which consists of a clock (BIT_CLK), frame synchronization (SYNC), serial data in (SDATA_IN), serial data out (SDATA_OUT), and a reset (RESET#).

4.2. Controller to Single CODEC

The simplest and most common AC'97 system configuration is a point-to-point AC-link connection between Controller and the STAC9766/9767, as illustrated in Figure 11.

Figure 11. AC-Link to its Companion Controller

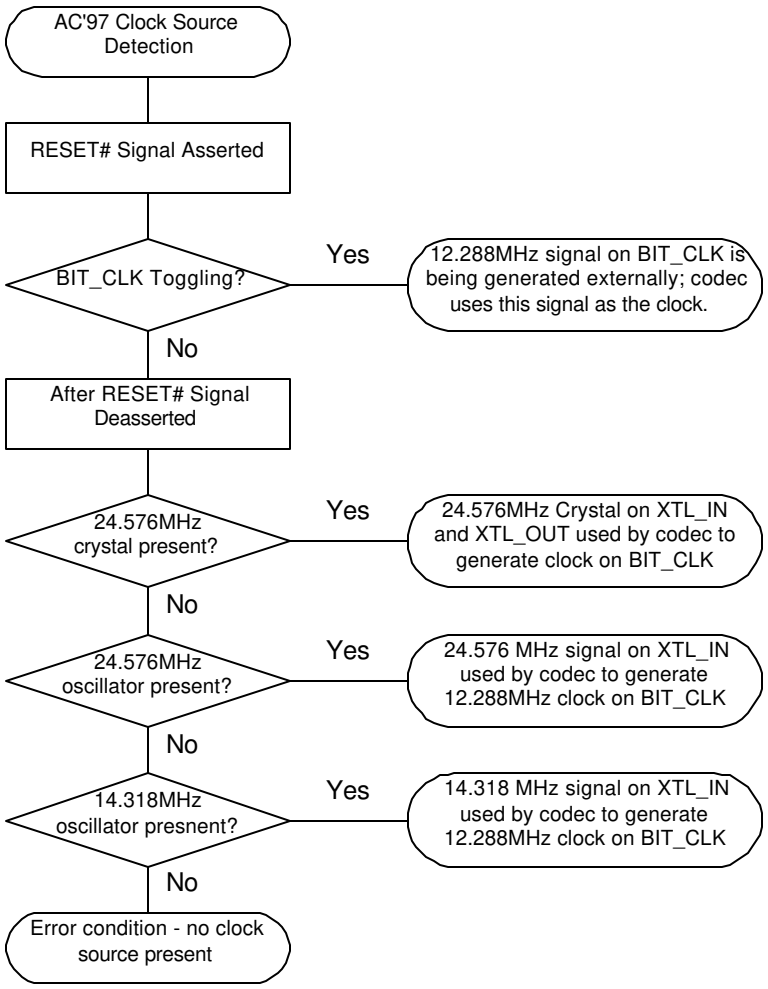


A primary CODEC may act as either a source or a consumer of BIT_CLK, depending on the configuration.

While RESET# is asserted, if a clock is present at the BIT_CLK pin for at least five cycles before RESET# is de-asserted, then the CODEC is a consumer of BIT_CLK, and must not drive BIT_CLK when RESET# is de-asserted. The clock is being provided by other than the primary CODEC, for instance by the controller or an independent clock chip. In this case the primary CODEC must act as a consumer of the BIT_CLK signal as if it were a secondary CODEC.

This clock source detection must be done each time the RESET# line is asserted. In the case of a warm reset, where the clock is halted but RESET# is not asserted, the CODEC must remember the clock source, and not begin generating the clock on the assertion of SYNC if the CODEC had previously determined that it was a consumer of BIT_CLK.

Figure 12. CODEC Clock Source Detection



The STAC9766/9767 uses the XTAL_OUT pin (pin 3) and the CID0 and CID1 pins (pins 45 & 46) to determine its alternate clock frequencies. See section 2.2.4: page14 for additional information on Crystal Elimination and for supported clock frequencies.

If, when the RESET# signal has been de-asserted, the CODEC has not detected a signal on BIT_CLK, as defined in the previous paragraph, then the AC'97 CODEC derives its clock internally from an externally attached 24.576 MHz crystal or oscillator (or optionally from an external 14.318 MHz oscillator), and drives a buffered 12.288 MHz clock to its digital companion Controller over AC-link under the signal name "BIT_CLK". Clock jitter at the DACs and ADCs is a fundamental impediment to high quality output, and the internally generated clock will provide AC'97 with a clean clock that is independent of the physical proximity of AC'97's companion Digital Controller (hence-forth referred to as "the Controller").

If BIT_CLK begins toggling while the RESET# signal is still asserted, the clock is being provided by other than the primary CODEC, for instance by the controller or by a discrete clock source. In this case, the primary CODEC must act as a consumer of the BIT_CLK signal as if it were a secondary CODEC.

The beginning of all audio sample packets, or Audio Frames, transferred over AC-link is synchronized to the rising edge of the SYNC signal. SYNC is driven by the Controller. The Controller generates SYNC by dividing BIT_CLK by 256 and applying some conditioning to tailor its duty cycle. This yields a 48 KHz SYNC signal whose period defines an audio frame. Data is transitioned on AC-link on every rising edge of BIT_CLK, and subsequently sampled by the receiving device on the receiving side of AC-link on each immediately following falling edge of BIT_CLK.

4.3. Controller to Multiple CODECs

Several vendor specific methods of supporting multiple CODEC configurations on AC-link have been implemented or proposed, including CODECs with selective AC-link pass-through and controllers with duplicate AC-links.

Potential implementations include:

- 6-channel audio using 3 x 2-channel CODECs.
- Separate CODECs for independent audio and modem AFE.
- Docking stations, where one CODEC is in the laptop and another is in the dock.

This specification defines support for up to four CODECs on the AC-link. By definition there can be one Primary CODEC (ID 00) and up to three Secondary CODECs (IDs 01,10, and 11). The CODEC ID functions as a chip select. Secondary devices therefore have completely orthogonal register sets; each is individually accessible and they do not share registers.

Multiple CODEC AC-link implementations must run off a common BIT_CLK. They can potentially save Controller pins by sharing SYNC, SDATA_OUT, and RESET# from the AC'97 Digital Controller. Each device requires its own SDATA_IN pin back to the Controller. This prevents contention of multiple devices on one serial input line.

Support for multiple CODEC operation necessitates a specially designed Controller. An AC'97 Digital Controller that supports multiple CODEC configurations implements multiple SDATA_IN inputs, supporting one Primary CODEC and up to three Secondary CODECs.

4.3.1. Primary CODEC Addressing

Primary AC'97 CODECs respond to register read and write commands directed to CODEC ID 00. Primary devices must be configurable (by hardwiring, strap pin(s), or other methods) as CODEC ID 00, and reflect this in the two-bit CODEC ID field(s) of the Extended Audio and/or Extended Modem ID Register(s).

The Primary CODEC may either drive the BIT_CLK signal or consume a BIT_CLK signal provided by the digital controller or other clock generator.

4.3.2. Secondary CODEC Addressing

Secondary AC'97 CODECs respond to register read and write commands directed to CODEC IDs 01, 10, or 11. Secondary devices must be configurable (via hardwiring, strap pin(s), or other methods) as CODEC IDs 01, 10, or 11 in the two-bit field(s) of the Extended Audio and/or Extended Modem ID Register(s).

CODECs configured as Secondary must power up with the BIT_CLK pin configured as an input. Using the provided BIT_CLK signal is necessary to ensure that everything on the AC-link is synchronous. BIT_CLK is the clock source (multiplied by 2 so that the internal rate is 24.576 MHz).

4.3.3. CODEC ID Strapping

Audio CODECs in the 48-pin package use pins 45 and 46 (defined as ID0# and ID1#) as strapping (i.e. configuration) pins to configure the CODEC ID. The ID0# and ID1# strapping bits adopt inverted polarity and default to 00 = Primary (via a weak internal pullup) when left floating. This eliminates the need for external resistors for CODECs configured as Primary, and maintains backward compatibility with existing layouts that treat pins 45 and 46 as "no connect" or cap to ground. Pulldowns are typically 1 KΩ - 10 KΩ and connected to Digital (not Analog) Ground.

Table 3. Recommended CODEC ID Strapping

CID1 (pin 46)	CID0 (pin 45)	Configuration
NC (weak internal pullup)	NC (weak internal pullup)	Primary ID 00
NC (weak internal pullup)	pulldown	Secondary ID 01
pulldown	NC (weak internal pullup)	Secondary ID 10
pulldown	pulldown	Secondary ID 11

4.4. Clocking for Multiple CODEC Implementations

To keep the system synchronous, all Primary and Secondary CODEC clocking must be derived from the same clock source, so they are operating on the same time base. In addition, all AC-link protocol timing must be based on the BIT_CLK signal, to ensure that everything on the AC-link will be synchronous.

The following are potential 24.576 MHz clock options available to a Secondary CODEC:

- Using an external 24.576 MHz signal source (external oscillator or AC'97 Digital Controller)
- Using the Primary's XTAL_OUT
- Using the Primary's BIT_CLK output to derive 24.576 MHz

See section 2.2.3: page14 for clock frequencies supported and configurations.

4.4.1. STAC9766/9767 as a Primary CODEC

Primary devices are required to support correctly either of the following clocking options:

- 24.576 MHz crystal attached to XTAL_IN and XTAL_OUT
- 24.576 MHz external oscillator provided to XTAL_IN
- 12.288 MHz oscillator provided to the BIT_CLK input

The Primary device may also optionally support the following clocking option:

- 14.318 MHz external oscillator provided to XTAL_IN

See section 2.2.3: page14 for clock frequencies supported and configurations.

4.4.2. STAC9766/9767 as a Secondary CODEC

Secondary devices are required to function correctly using one or more of the following clocking options:

- 24.576 MHz external oscillator provided to XTAL_IN (synchronous and in phase with Primary 24.576 MHz clock)
- BIT_CLK input provided by the Primary. In this mode, a clock at XTAL_IN (Pin 2) is ignored.

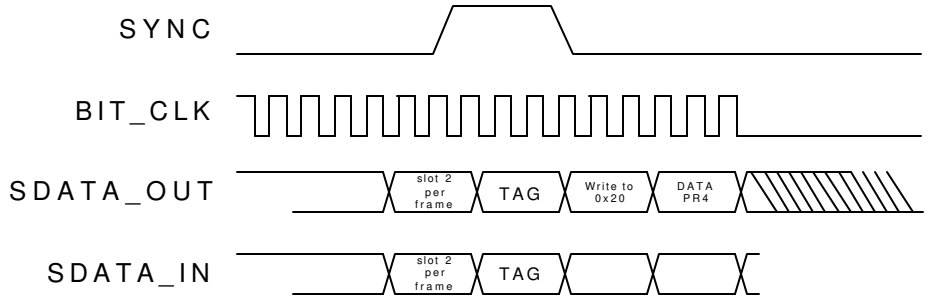
See section 2.2.3: page14 for clock frequencies supported and configurations.

4.5. AC-link Power Management

4.5.1. Powering down the AC-link

The AC-link signals can be placed in a low power mode. When AC'97's Powerdown Register (26h) is programmed to the appropriate value, both BIT_CLK and SDATA_IN are brought to and held at a logic low voltage level. After signaling a reset to AC'97, the AC'97 Controller should not attempt to play or capture audio data until it has sampled a CODEC Ready indication from AC'97.

Figure 13. STAC9766/9767 Powerdown Timing



Note: BIT_CLK not to scale

BIT_CLK and SDATA_IN are transitioned low immediately following decode of the write to the Powerdown Register (26h) with PR4. When the AC'97 Controller driver is at the point where it is ready to program the AC-link into its low power mode, slots 1 and 2 are assumed to be the only valid stream in the audio output frame.

After programming the AC'97 device to this low power, halted mode, the AC'97 Controller is required to drive and keep SYNC and SDATA_OUT low.

Once the AC'97 CODEC has been instructed to halt BIT_CLK, a special "wake-up" protocol must be used to bring the AC-link to the active mode, since normal audio output and input frames can not be communicated in the absence of BIT_CLK.

4.5.2. Waking up the AC-link

There are two methods for bringing the AC-link out of a low power, halted mode. Regardless of the method, it is the AC'97 Controller that performs the wake-up task.

AC-link protocol provides for a "Cold AC'97 Reset", and a "Warm AC'97 Reset". The current power down state would ultimately dictate which form of AC'97 reset is appropriate. Unless a "cold" or "register" reset (a write to the Reset Register) is performed, wherein the AC'97 registers are initialized to their default values, registers are required to keep state during all power down modes.

Once powered down, re-activation of the AC-link via re-assertion of the SYNC signal must not occur for a minimum of four audio frame times following the frame in which the power down was triggered. When AC-link powers up the CODEC indicates readiness via the CODEC Ready bit (input slot 0, bit 15).

4.5.3. CODEC Triggers Wake-up

The STAC9766/9767 (running off Vaux) can trigger a wake event (PME#) by transitioning SDATA_IN from low to high and holding it high until either a warm or cold reset is observed on the AC-link. This functionality is typically implemented in modem CODECs that detect ring, Caller ID, etc.

Note that when the AC-link is either programmed to the low power mode or shut off completely, BIT_CLK may stop if the primary CODEC is supplying the clock, which shuts down the AC-link clock to the Secondary CODEC[1]. In order for a Secondary CODEC to react to an external event (phone ringing), it must support an independent clocking scheme for any PME# associated logic that must be kept alive when the AC-link is down. This includes logic to asynchronously drive SDATA_IN to a logic high-level which signals a wake request to the AC'97 Digital Controller.

4.5.4. CODEC Reset

There are three types of AC'97 reset:

- A *cold* reset where all AC'97 logic (most registers included) is initialized to its default state.
- A *warm* reset where the contents of the AC'97 register set are left unaltered.
- A *register* reset which only initializes the AC'97 registers to their default states.

4.5.4.1. Cold AC'97 Reset

A cold reset is achieved by asserting RESET# low for the minimum specified time, then subsequently de-asserting RESET# high. BIT_CLK and SDATA_IN will be activated, or re-activated as the case may be, and all AC'97 control registers will be initialized to their default power-on reset values.

RESET# is an asynchronous AC'97 input.

4.5.4.2. Warm AC'97 Reset

A warm AC'97 reset will re-activate the AC-link without altering the current AC'97 register values. A warm reset is signaled by driving SYNC high for a minimum of 1 µs in the absence of BIT_CLK.

1. Secondary CODEC always configures its BIT_CLK pin as an input.