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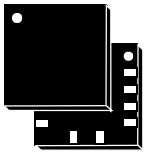
IIS2MDC

High-accuracy, ultra-low-power, 3-axis digital output magnetometer

Datasheet - production data



LGA-12 (2.0x2.0x0.7 mm)

Features

- 3 magnetic field channels
- Up to ±50 gauss magnetic dynamic range
- 16-bit data output
- SPI/I^2C serial interfaces
- Analog supply voltage 1.71 V to 3.6 V
- Selectable power mode/resolution
- Single measurement mode up to 150 Hz
- Support for hard-iron compensation
- Programmable interrupt generator
- Embedded self-test
- Embedded temperature sensor
- ECOPACK®, RoHS and “Green” compliant

Applications

- Anti-tampering in smart meters
- Positional and distance sensors
- Compasses for Inertial Measurement Unit (IMU)
- Presence detection, magnetic switches
- Variable magnetic field monitoring

Description

The IIS2MDC is a high-accuracy, ultra-low-power 3-axis digital magnetic sensor.

The IIS2MDC has a magnetic field dynamic range up to ±50 gauss.

The IIS2MDC includes an I^2C serial bus interface that supports standard, fast mode, fast mode plus, and high-speed (100 kHz, 400 kHz, 1 MHz, and 3.4 MHz) and an SPI serial standard interface.

The device can be configured to generate an interrupt signal for magnetic field detection.

The IIS2MDC is available in a plastic land grid array package (LGA) and is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Part number	Temp. range [°C]	Package	Packaging
IIS2MDCTR	-40 to +85	LGA-12	Tape and reel

Contents

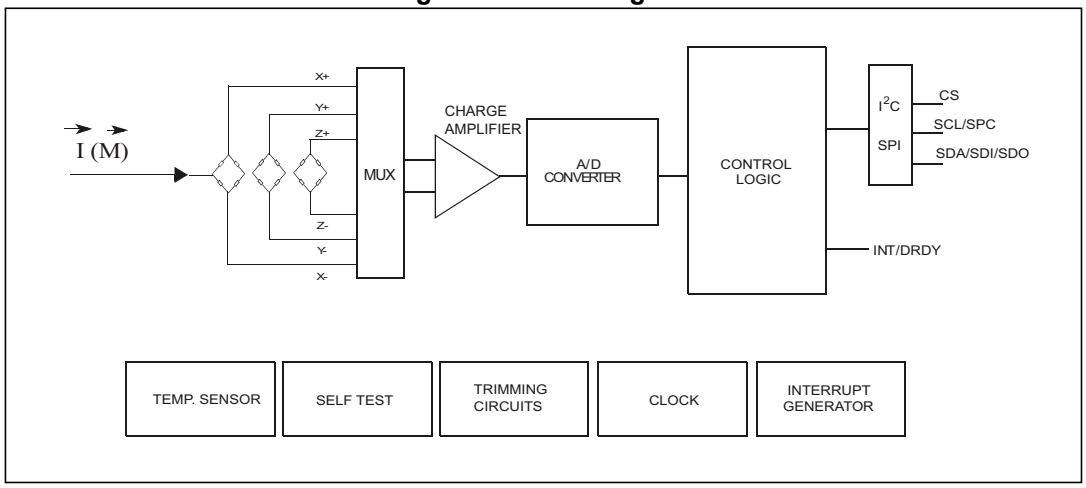
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

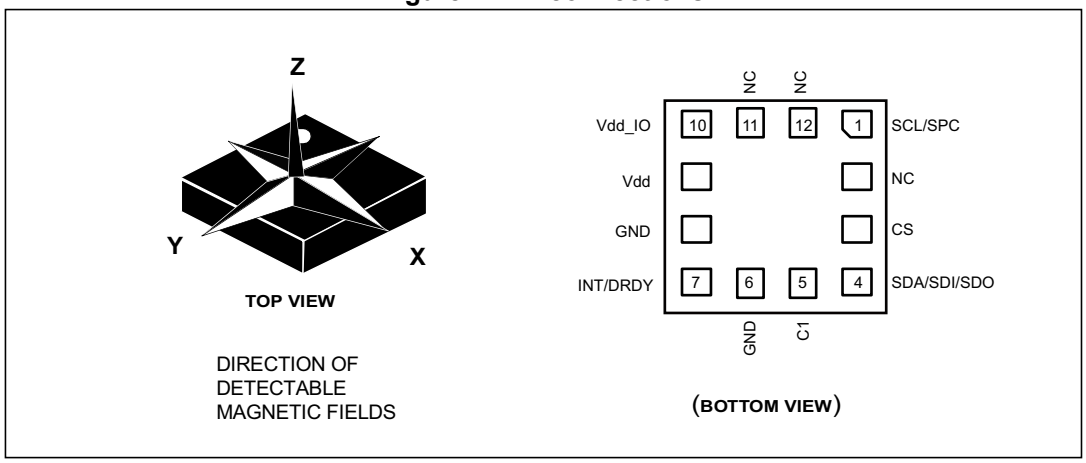


Table 2. Pin description

Pin#	Name	Function
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
2	NC	Internally not connected. Can be tied to Vdd, Vdd_IO or GND.
3	CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	C1	Capacitor connection (C1 = 220 nF)
6	GND	Connected to GND
7	INT/DRDY	Interrupt/data-ready signal
8	GND	0 V
9	Vdd	Power supply
10	Vdd_IO	Power supply for I/O pins
11	NC	Internally not connected. Can be tied to Vdd, Vdd_IO or GND.
12	NC	Internally not connected. Can be tied to Vdd, Vdd_IO or GND.

2 Module specifications

2.1 Sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted[a].

Table 3. Sensor characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ.(2)	Max.(1)	Unit
FS	Magnetic dynamic range(3)		±25	±49.152		gauss
So	Sensitivity(4)		-7%	1.5	+7%	mgauss/ LSB
TCSo	Sensitivity change vs. temperature(5)			±0.03		%/°C
TyOff	Magnetic sensor offset	With offset cancellation(6)(7)	-60		+60	mgauss
TCOff	Magnetic sensor offset change vs. temp.(6)	With offset cancellation	-0.3		+0.3	mgauss/°C
RMS	RMS noise(8)	High-resolution mode		3	4.6	mgauss (RMS)
ODR	Output data rate			10 20 50 100 150(9)		Hz
ST	Self-test(10)		15		500	mgauss
Top	Operating temperature range		-40		+85	°C

1. Min/Max values are based on characterization results, not tested in production and not guaranteed.
2. Typical specifications are not guaranteed.
3. The typical value of the magnetic dynamic range applies when the magnetic field is fully aligned with one of the sensitive axes. In presence of a stray field in the cross-axis direction, the magnetic dynamic range (max module) can decrease down to the min value.
4. Values after factory calibration test and trimming.
5. Measurements are performed in a uniform temperature setup and they are based on characterization data in a limited number of samples, not measured during final test for production.
6. Based on characterization data on a limited number of samples, not measured during final test for production.
7. Excluding drift due to magnetic shock.
8. With low-pass filter or offset cancellation enabled.
9. LP, single measurement mode.
10. “Self-test” is defined as: $OUTPUT[gauss]_{(Self\text{-}test\ enabled)} - OUTPUT[gauss]_{(Self\text{-}test\ disabled)}$.

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

2.2 Temperature sensor characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted [b].

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temp.			8		digit/°C(2)
TODR	Temperature refresh rate			ODR(3)		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. 12-bit resolution.
3. Refer to *Table 25*.

2.3 Electrical characteristics

@ Vdd = 2.5 V, T = 25 °C unless otherwise noted.[b]

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.71	2.5	3.6	V
Vdd_IO	Module power supply for I/O		1.71		3.6	V
Idd_HR	Current consumption in high-resolution mode(2)	ODR = 100 Hz		1130		µA
Idd_LP	Current consumption in low-power mode(3)	ODR = 10 Hz		25		µA
Idd_PD	Current consumption in power-down			1.5		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage	IOH = 4 mA	Vdd_IO - 0.2			V
VOL	Low-level output voltage	IOL = 4 mA			0.2	V
T_{OP}	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Offset cancellation turned on.
3. Offset cancellation turned off.

b. The product is factory calibrated at 2.5 V.The operational power supply range is from 1.71 V to 3.6 V.

2.4 Communication interface characteristics

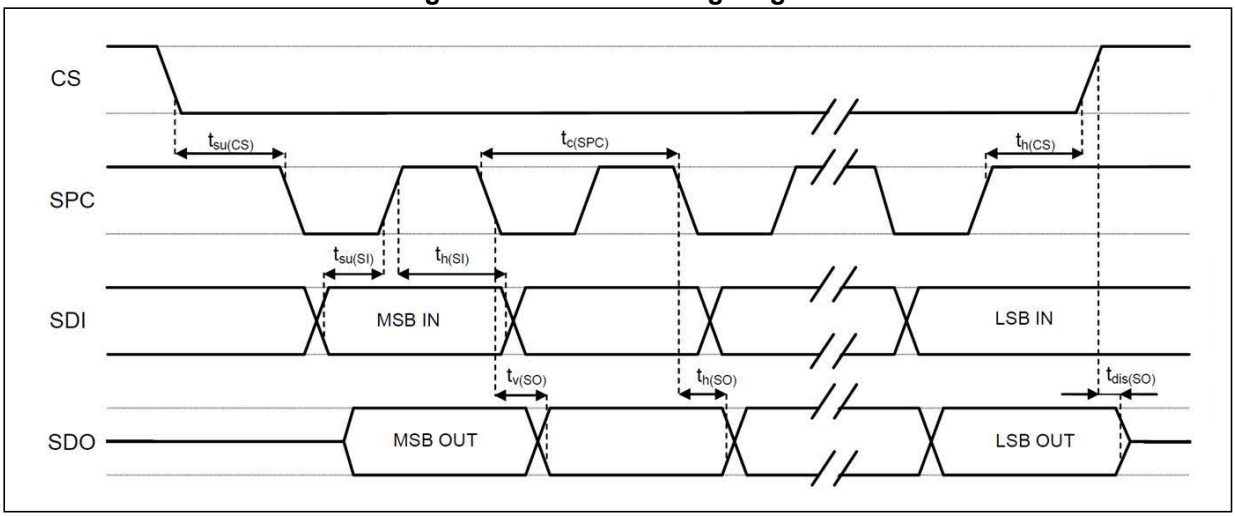
2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	5		ns
$t_{h(CS)}$	CS hold time	20		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	5		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 3. SPI slave timing diagram



Note: Values are guaranteed at 10 MHz clock frequency for SPI with 3 wires, based on characterization results, not tested in production.

Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values (standard and fast mode)

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	Low period of the SCL clock	4.7		1.3		µs
$t_{w(SCLH)}$	High period of the SCL clock	4.0		0.6		
$t_{su(SDA)}$	Data setup time	250		100		ns
$t_{h(SDA)}$	Data hold time	0	3.45	0	0.9	µs
$t_{h(ST)}$	START condition hold time	4		0.6		
$t_{su(SR)}$	Setup time for a repeated START condition	4.7		0.6		
$t_{su(SP)}$	Setup time for STOP condition	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

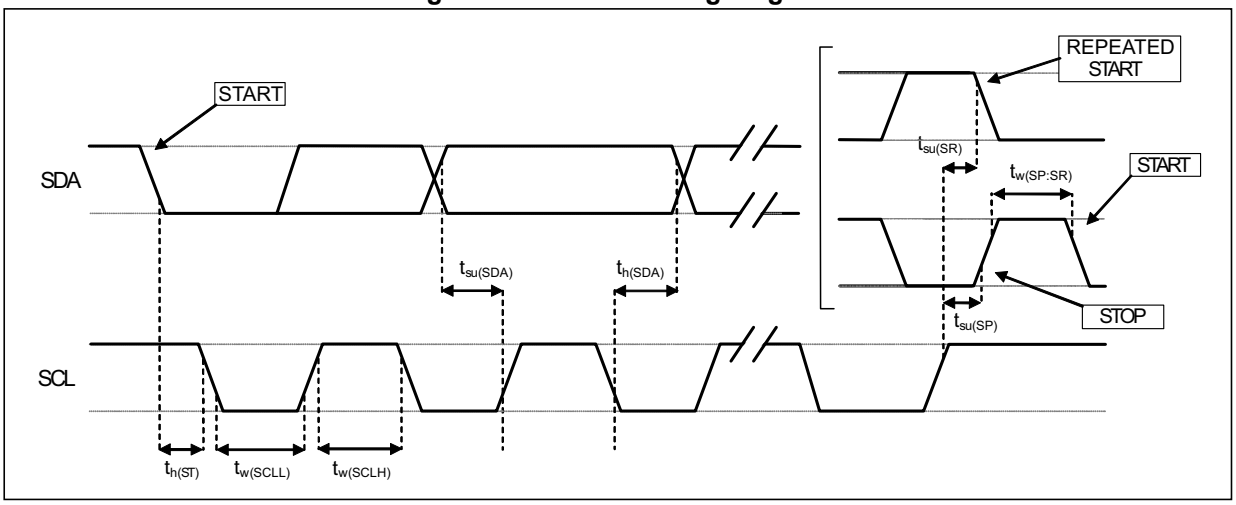
1. Data based on standard I²C protocol requirement, not tested in production.

Table 8. I²C slave timing values (fast mode plus and high speed)

Symbol	Parameter	I²C fast mode plus(1)		I²C high speed(1)		Unit
		Min	Max	Min	Max	
$f_{(SCL)}$	SCL clock frequency	0	1	0	3.4	MHz
$t_{w(SCLL)}$	Low period of the SCL clock	0.5		0.16		µs
$t_{w(SCLH)}$	High period of the SCL clock	0.26		0.06		
$t_{su(SDA)}$	Data setup time	50		10		ns
$t_{h(SDA)}$	Data hold time	0		0	0.07	µs
$t_{h(ST)}$	START condition hold time	0.26		0.16		
$t_{su(SR)}$	Setup time for a repeated START condition	0.26		0.16		
$t_{su(SP)}$	Setup time for STOP condition	0.26		0.16		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	0.5				

1. Data based on standard I²C protocol requirement, not tested in production.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 9. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO)	-0.3 to Vdd_IO +0.3	V
M_{EF}	Maximum exposed field	10000	gauss
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection (HBM)	2	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

Sensitivity describes the ratio of the output digital data expressed in LSB units and the applied magnetic field expressed in mG (milligauss). It can be measured, for example, by applying a known magnetic field along one axis and measuring the digital output of the device.

3.2 Zero-*gauss* level

Zero-*g*auss level offset (TyOff) describes the deviation of an actual output signal from the ideal output if no magnetic field is present.

3.3 Magnetic dynamic range

The magnetic dynamic range of the sensor can be fully exploited when the applied magnetic field is entirely aligned with one of the sensitive axes of the sensor.

In the presence of a stray field in the cross-axis direction, the exploitable magnetic dynamic range (maximum module) can decrease.

4 Functionality

4.1 Power modes

The IIS2MDC provides two different power modes: high-resolution and low-power modes.

The tables below summarize the RMS noise values and current consumption in different product configurations.

When the low-pass filter is enabled, the bandwidth is reduced while noise performance is improved without any increase in power consumption.

Table 10. RMS noise of operating modes

CFG_REG_B[LPF] or CFG_REG_B[OFF_CANC]	(CFG_REG_A[LP = 0]) high-resolution mode		(CFG_REG_A[LP = 1]) low-power mode	
	BW [Hz]	Noise RMS [mg]	BW [Hz]	Noise RMS [mg]
0 (disable)	ODR/2	4.5	ODR/2	9
1 (enable)	ODR/4	3	ODR/4	6

Table 11. Current consumption of operating modes

ODR (Hz)	Current consumption (µA) (CFG_REG_A [LP] = 0) high-resolution CFG_REG_B [OFF_CANC] = 0	Current consumption (µA) (CFG_REG_A [LP] = 1) low-power CFG_REG_B [OFF_CANC] = 0	Current consumption (µA) (CFG_REG_A [LP] = 0) high-resolution CFG_REG_B [OFF_CANC] = 1	Current consumption (µA) (CFG_REG_A [LP] = 1) low-power CFG_REG_B [OFF_CANC] = 1
10	100	25	120	50
20	200	50	235	100
50	475	125	575	235
100	950	250	1130	460

The following table summarizes the turn-on time of the device in the two different power modes with the offset cancellation function enabled or disabled (see *Section : Where Current_consumption_in_power_down and Current_consumption_10Hz can be found, respectively, in Table 5 and Table 11.*).

Table 12. Operating mode and turn-on time

Operating mode	Turn-on time	
CFG_REG_A[LP]	**CFG_REG_A[OFF_CANC = 0]**	**CFG_REG_A[OFF_CANC = 1]**
0 (high-resolution)	9.4 ms	9.4 ms + 1/ODR
1 (low-power)	6.4 ms	6.4 ms + 1/ODR

The IIS2MDC offers single measurement mode in both high-resolution and low-power modes.

Single measurement mode is enabled by writing bits MD[1:0] to '01' in *CFG_REG_A (60h)*.

In single measurement mode, once the measurement has been performed, the DRDY pin is set to high, data is available in the output register and the IIS2MDC is automatically configured in idle mode by setting the MD[1] bit to '1'.

Single measurement is independent of the programmed ODR but depends on the frequency at which the MD[1:0] bits are written by the microcontroller/application processor.

Maximum ODR frequency achievable in single mode measurement is given in the following table.

Table 13. Maximum ODR in single measurement mode (HR and LP modes)

Maximum ODR	Power mode (CFG_REG_A[LP])
100 Hz	High resolution (LP = ‘0’)
150 Hz	Low power (LP = ‘1’)

In single measurement mode, for ODR < 10 Hz, current consumption can be calculated with the following formula:

(Current_consumption_10Hz - Current_consumption_in_power_down) / (10 Hz / ODR) + Current_consumption_in_power_down

Where Current_consumption_in_power_down and Current_consumption_10Hz can be found, respectively, in *Table 5* and *Table 11*.

4.2 IC interface

The complete measurement chain is composed of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The magnetic data may be accessed through an I^2C/SPI interface thus making the device particularly suitable for direct interfacing with a microcontroller.

The IIS2MDC features a data-ready signal which indicates when new sets of measured magnetic data are available, thus simplifying data synchronization in the digital system that uses the device.

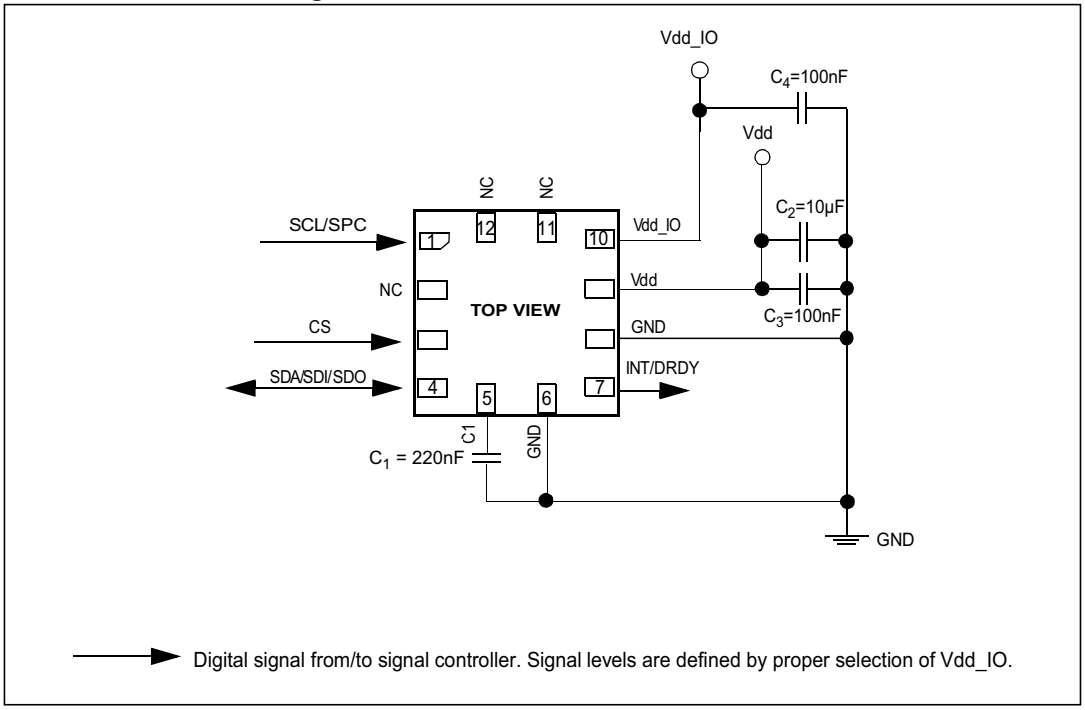
4.3 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*gauss* level (TyOff).

The trim values are stored inside the device in nonvolatile memory. Anytime the device is turned on, the trim parameters are downloaded into the registers to be used during active operation. This allows using the device without further calibration.

5 Application hints

Figure 5. IIS2MDC electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 9 of the device (common design practice).

It is possible to remove Vdd, maintaining Vdd_IO, without blocking the communication bus, in this condition the measurement chain is powered off.

The following recommendations apply to capacitor C1:

- It must be connected as close as possible to pins 5 and 6 since very high current pulses flow from C1 to pin 5 and 6. This avoids problems caused by inductive effects due to the length of the copper strips.
- It is highly recommended to use low ESR (max 200 mOhm)

The functionality of the device and the measured acceleration data are selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high (i.e. connected to Vdd_IO).

The functions, the threshold and the timing of the interrupt pin (INT) can be completely programmed by the user through the I^2C/SPI interface.

Table 14. Internal pin status

Pin#	Name	Function	Pin status
1	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)	Default: input without pull-up
2	NC		Internally not connected
3	CS	I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)	Default: input without pull-up
4	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)	Default: (SDA) input without pull-up
5	C1	Capacitor connection (C1 = 220 nF)	External capacitor, voltage forced by the device
6	GND	0 V	
7	INT/DRDY	Interrupt/data-ready signal	Default: output high impedance
8	GND	0 V	
9	Vdd	Power supply	
10	Vdd_IO	Power supply for I/O pins	
11	NC		Internally not connected
12	NC		Internally not connected

Note: *In order to program INT/DRDY as a push-pull output, write the INT_on_PIN or DRDY_on_PIN bit to '1' in CFG_REG_C (62h).*

Please refer to AN5080 for more information (magnetometer offset cancellation, magnetometer hard-iron compensation, interrupt generation, self-test procedure, Temperature sensor).

5.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Land pattern and soldering recommendations are available at www.st.com.

5.2 High-current wiring effects

High current in wiring and printed circuit traces can be culprits in causing errors in magnetic field measurements for compassing.

Conductor-generated magnetic fields will add to the Earth’s magnetic field, leading to errors in compass heading computation.

Keep currents higher than 10 mA a few millimeters away from the sensor IC.

5.3 Startup sequence

The following general-purpose sequence can be used to configure the device:

1. Write CFG_REG_A = 80h // Enable temperature compensation
2. Write CFG_REG_C = 01h // Mag data-ready interrupt enable

6 Digital interfaces

The registers embedded inside the IIS2MDC may be accessed through both the I^2C and 3-wire SPI serial interfaces.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 15. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire SPI interface serial data output (SDO)

6.1 I^2C serial interface

The IIS2MDC I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 16. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both the lines are high.

The I^2C interface is compliant with standard mode (100 kHz), fast mode (400 kHz), fast mode plus (1 MHz) and high speed mode (3.4 MHz).

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a high-to-low transition on the data line while the SCL line is held high. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the master.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the high period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the IIS2MDC behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is ‘1’, the SUB (register address) is automatically increased to allow multiple data read/writes.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the master will transmit to the slave with direction unchanged. *Table 21* explains how the SAD+read/write bit pattern is composed, listing all the possible configurations.

Table 17. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 18. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 19. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 20. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DAT A		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit

(MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left high by the slave. The master can then abort the transfer. A low-to-high transition on the SDA line while the SCL line is high is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In the presented communication format MAK is Master acknowledge and NMAK is No Master Acknowledge.

Default address:

The slave address is 0011110b.

The slave address is completed with a Read/Write bit. If the bit was '1' (Read), a repeated START (SR) condition must be issued after the sub-address byte. If the bit is '0' (Write) the master will transmit to the slave with direction unchanged. *Table 21* explains how the SAD+Read/Write bit patterns are composed, listing all the possible configurations.

Table 21. SAD + Read/Write patterns

Command	SAD[6:0]	R/W	SAD + R/W
Read	0011110	1	00111101 (3Dh)
Write	0011110	0	00111100 (3Ch)

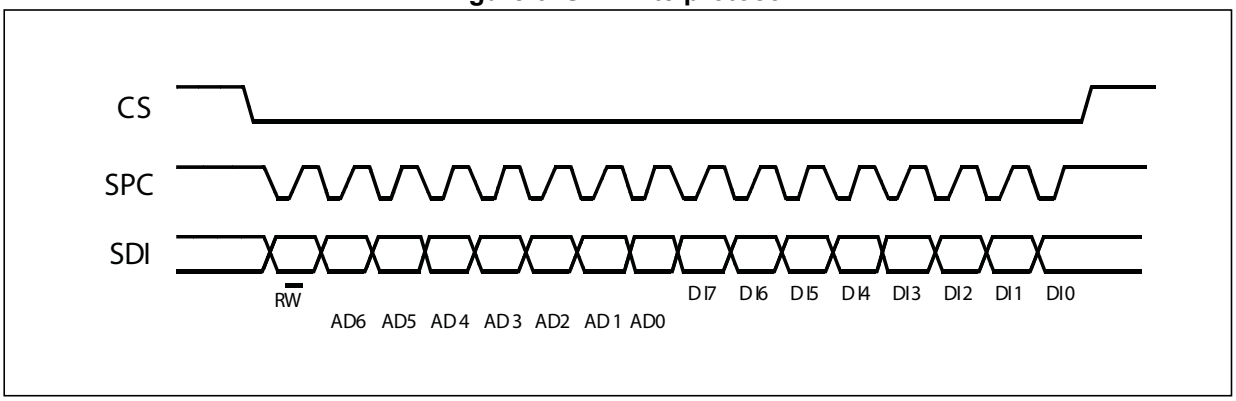
6.2 SPI bus interface

The IIS2MDC SPI is a bus slave. The SPI allows writing and reading the registers of the device.

The serial interface interacts with the application using 3 wires: **CS, SPC**, **SDI/O**.

6.2.1 SPI write

Figure 6. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

bit 1-7: address AD(6:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that is written inside the device (MSb first).

bit 16-... : data DI(...-8). Further data in multiple byte writes.

Figure 7. Multiple byte SPI write protocol (2-byte example)