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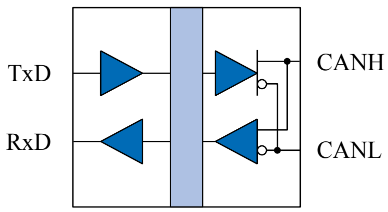
Basic Function Isolated CAN Transceiver

Functional Diagram



IL41050TT

V_{DD2} (V)	TxD[1]	S	CANH	CANL	Bus State	RxD
4.75 to 5.25	↓	Low[2]	High	Low	Dominant	Low
4.75 to 5.25	X	High	$V_{DD2}/2$	$V_{DD2}/2$	Recessive	High
4.75 to 5.25	↑	X	$V_{DD2}/2$	$V_{DD2}/2$	Recessive	High
<2V (no pwr)	X	X	0<V<2.5	0<V<2.5	Recessive	High
$2<V_{DD2}<4.75$	>2V	X	0<V<2.5	0<V<2.5	Recessive	High

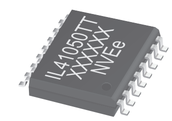
Table 1. Function table.

Notes:

1. TxD input is edge triggered: ↑ = Logic Lo to Hi, ↓ = Hi to Lo
2. Valid for logic state as described or open circuit

X = don't care

Features



- Industry-standard pinout
- 5000 V_{RMS} isolation ("V"-Version)
- 180 ns typical loop delay
- 70 mA maximum bus-side dynamic supply current
- 12 mA maximum quiescent recessive supply current
- 1 Mbps
- Fully compliant with the ISO 11898-2 CAN standard
- −55°C to +100°C operating temperature
- 3 V to 5.5 V power supplies
- >110-node fan-out
- 600 V_{RMS} working voltage per VDE V 0884-10
- 44000 year barrier life
- ±500 V CDM ESD
- 50 kV/µs typ.; 30 kV/µs min. common mode transient immunity
- No carrier or clock for low emissions and EMI susceptibility
- Transmit data (TxD) dominant time-out function
- Edge triggered, non-volatile input improves noise performance
- Thermal shutdown protection
- Bus power short-circuit protection
- No "S" or Vref functions
- 0.3" True 8™ mm 16-pin packages
- UL 1577 recognized; VDE V 0884-1- certified

Applications

- Factory automation
- Battery management systems
- Noise-critical CAN
- DeviceNet

Description

The IL41050TT is a galvanically isolated, CAN (Controller Area Network) transceiver containing basic functions but without "S" or Vref pins. It is a direct replacement for the Texas Instruments ISO1050DW with much better reliability and longer barrier life, less EMI emissions, and true 8 mm external creepage.

The IL41050 family provides isolated differential transmit capability to the bus and isolated differential receive capability to the CAN controller via NVE's patented* IsoLoop spintronic Giant Magnetoresistance (GMR) technology.

A unique ceramic/polymer composite barrier provides excellent isolation and virtually unlimited barrier life.

Designed for harsh CAN and DeviceNet environments, IL41050 transceivers have transmit data dominant time-out, bus pin transient protection, a rugged Charged Device Model ESD rating, thermal shutdown protection, and short-circuit protection. Unique edge-triggered inputs improve noise performance.

REV. A

Absolute Maximum Ratings[1][2]

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Storage temperature	T_S	−55		150	°C	
Junction temperature	T_J	−55		150	°C	
Ambient operating temperature	T_A	−55		100	°C	
DC voltage at CANH and CANL pins	V_{CANH}, V_{CANL}	−45		45	V	0 V< V_{DD2} < 5.25 V; indefinite duration
Supply voltage	V_{DD1}, V_{DD2}	−0.3		7	V	
Digital input voltage	V_{TxD}, V_S	−0.3		V_{DD} + 0.3	V	
Digital output voltage	V_{RxD}	−0.3		V_{DD} + 0.3	V	
DC voltage at V_{REF}	V_{REF}	−0.3		V_{DD} + 0.3	V	
Transient voltage at CANH or CANL	$V_{trt(CAN)}$	−150		150	V	
Electrostatic discharge at all pins	V_{esd}	−4000		4000	V	Human body model
Electrostatic discharge at all pins	V_{esd}	−500		500	V	Machine model

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units	Test Conditions
Supply voltage	V_{DD1} V_{DD2}	3.0 4.75		5.5 5.25	V	
Junction temperature	T_J	−55		140	°C	
Input voltage at any bus terminal (separately or common mode)	V_{CANH} V_{CANL}	−12		12	V	
High-level digital input voltage[3][4]	V_{IH}	2.0 2.4 2.0		V_{DD1} V_{DD1} V_{DD2}	V	V_{DD1} = 3.3 V V_{DD1} = 5.0 V V_{DD2} = 5.0 V
Low-level digital input voltage[3][4]	V_{IL}	0		0.8	V	
Digital output current (RxD)	I_{OH}	−8		8	mA	V_{DD1} = 3.3V to 5V
Ambient operating temperature	T_A	−55		100	°C	
Digital input signal rise and fall times	t_{IR}, t_{IF}			1	μs	

Insulation Specifications

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Creepage distance (external)			8.03	8.3		mm	Per IEC 60601
Total barrier thickness (internal)			0.012	0.013		mm	
Barrier resistance		R_{IO}		$>10^{14}$		Ω	500 V
Barrier capacitance		C_{IO}		7		pF	f = 1 MHz
Leakage current				0.2		μA_{RMS}	240 V_{RMS}, 60 Hz
Comparative Tracking Index		CTI	≥175			V	Per IEC 60112
High voltage endurance (maximum barrier voltage for indefinite life)	AC DC	V_{IO}	1000 1500			V_{RMS} V_{DC}	At maximum operating temperature
Barrier life				44000		Years	100°C, 1000 V_{RMS}, 60% CL activation energy

Thermal Characteristics

Parameter		Symbol	Min.	Typ.	Max.	Units	Test Conditions
Junction–Ambient Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC	θ_{JA}		60 60 60		°C/W	Soldered to double-sided board; free air
Junction–Case (Top) Thermal Resistance	QSOP 0.15" SOIC 0.3" SOIC	Ψ_{JT}		10 10 20		°C/W	
Power Dissipation	QSOP 0.15" SOIC 0.3" SOIC	P_D			675 700 800	mW	

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Safety and Approvals

VDE V 0884-10 (File Number 5016933-4880-0001)

2.5 kV-rated version (IL41050TTE)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 2500 V_{RMS}
- Surge rating 4 kV

5 kV-rated version (IL41050TTVE)

- Working Voltage (V_{IORM}) 600 V_{RMS} (848 V_{PK}); basic insulation; pollution degree 2
- Isolation voltage (V_{ISO}) 5000 V_{RMS}
- Surge rating 4 kV

Safety-Limiting Values	Symbol	Value	Units
Safety rating ambient temperature	T_S	180	°C
Safety rating power (180°C)	P_S	270	mW
Supply current safety rating (total of supplies)	I_S	54	mA

IEC 61010-1 (Edition 2; TUV Certificate Numbers N1502812; N1502812-101)
Reinforced Insulation; Pollution Degree II; Material Group III
Working Voltage 600 V_{RMS}

UL 1577 (Component Recognition Program File Number E207481)

2.5 kV-rated version (IL41050TTE)
Each part tested at 3 kV_{RMS} (4.24 kV_{PK}) for 1 second; each lot sample tested at 2.5 kV_{RMS} (3.54 kV_{PK}) for 1 minute

5 kV-rated version (IL41050TTVE)
Each part tested at 6 kV_{RMS} (8.48 kV_{PK}) for 1 second; each lot sample tested at 5 kV_{RMS} (7.07 kV_{PK}) for 1 minute

Soldering Profile

Per JEDEC J-STD-020C; MSL=1

Notes:

1. Absolute Maximum specifications mean the device will not be damaged if operated under these conditions. It does not guarantee performance.
2. All voltages are with respect to network ground except differential I/O bus voltages.
3. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
4. The maximum time allowed for a logic transition at the TxD input is 1 µs.

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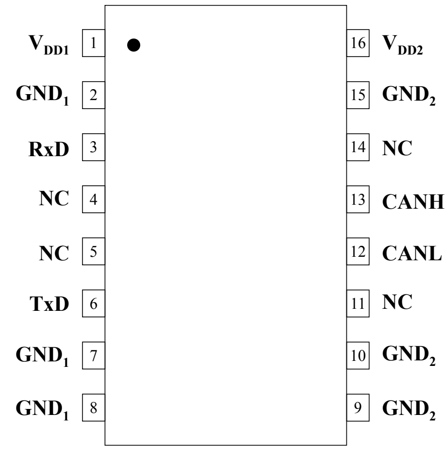
IL41050TT Pin Connections

1	V_{DD1}	V_{DD1} power supply input
2	GND_1	V_{DD1} power supply ground return (pin 2 is internally connected to pin 8)
3	RxD	Receive Data output
4	NC	No internal connection
5	NC	No internal connection
6	TxD	Transmit Data input
7,8	GND_1	V_{DD1} power supply ground return (pin 8 is internally connected to pin 2)
9,10	GND_2	V_{DD2} power supply ground return (pin 9 is internally connected to pin 15)
11	NC	No internal connection
12	CANL	Low level CANbus line
13	CANH	High level CANbus line
14	NC	No internal connection
15	GND_2	V_{DD2} power supply ground return (pin 15 is internally connected to pin 9)
16	V_{DD2}	V_{DD2} isolation power supply input



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Operating Specifications

Electrical Specifications (T_{min} to T_{max} and V_{DD1}, V_{DD2}= 4.75 V to 5.25 V unless otherwise stated)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Power Supply Current						
Quiescent supply current (recessive)	IQ_{VDD1}	1 0.7	1.75 1.4	3.0 2.0	mA	dr = 0 bps; V_{DD1} = 5 V dr = 0 bps; V_{DD1} = 3.3 V
Dynamic supply current (dominant)	I_{VDD1}	1.2 0.9	2.0 1.6	3.2 2.2	mA	dr = 1 Mbps, R_L= 60Ω; V_{DD1} = 5 V dr = 1 Mbps, R_L= 60Ω; V_{DD1} = 3.3 V
Quiescent supply current (recessive) Dynamic supply current (dominant)	IQ_{VDD2} I_{VDD2}	3.5 26	7 52	12 70	mA	0 bps 1 Mbps, R_L = 60Ω
Transmitter Data input (TxD)(1)						
High level input voltage ↑	V_{IH}	2.4		5.25	V	V_{DD1} = 5 V; recessive
High level input voltage ↑	V_{IH}	2.0		3.6	V	V_{DD1} = 3.3 V; recessive
Low level input voltage ↓	V_{IL}	−0.3		0.8	V	Output dominant
TxD input rise and fall time(2)	t_r			1	µs	10% to 90% tr
High level input current	I_{IH}	−10		10	µA	$V_{TxD} = V_{DD1}$
Low level input current	I_{IL}	10		10	µA	V_{TxD} = 0 V
Receiver Data output (RxD)						
High level output current	I_{OH}	−2	−8.5	−20	mA	V_{RxD} = 0.8 V_{DD1}
Low level output current	I_{OL}	2	8.5	20	mA	V_{RxD} = 0.45 V
Failsafe supply voltage(4)	V_{DD2}	3.6		3.9	V	
Bus lines (CANH and CANL)						
Recessive voltage at CANH pin	$V_{O(reces)}$ CANH	2.0	2.5	3.0	V	$V_{TxD} = V_{DD1}$, no load
Recessive voltage at CANL pin	$V_{O(reces)}$ CANL	2.0	2.5	3.0	V	$V_{TxD} = V_{DD1}$, no load
Recessive current at CANH pin	$I_{O(reces)}$ CANH	−2.5		+2.5	mA	−27V < V_{CANH}< +32V; 0V < V_{DD2}<5.25V
Recessive current at CANL pin	$I_{O(reces)}$ CANL	−2.5		+2.5	mA	−27V < V_{CANL} < +32V; 0 V <V_{DD2} < 5.25V
Dominant voltage at CANH pin	$V_{O(dom)}$ CANH	3.0	3.6	4.25	V	V_{TxD} = 0 V
Dominant voltage at CANL pin	$V_{O(dom)}$ CANL	0.5	1.4	1.75	V	V_{TxD} = 0 V
Differential bus input voltage ($V_{CANH} - V_{CANL}$)	$V_{i(dif)(bus)}$	1.5	2.25	3.0	V	V_{TxD} = 0 V; dominant 42.5 Ω < R_L < 60 Ω
		−120	0	+50	mV	$V_{TxD} = V_{DD1}$; recessive; no load
Short-circuit output current at CANH	$I_{O(sc)}$ CANH	−45	−70	−95	mA	V_{CANH} = 0 V, V_{TxD} = 0
Short-circuit output current at CANL	$I_{O(sc)}$ CANL	45	70	120	mA	V_{CANL} = 36 V, V_{TxD} = 0
Differential receiver threshold voltage	$V_{i(dif)(th)}$	0.5	0.7	0.9	V	−5 V <V_{CANL}< +10 V; −5 V <V_{CANH}< +10 V
Differential receiver input voltage hysteresis	$V_{i(dif)(hys)}$	50	70	100	mV	−5 V <V_{CANL}< +10 V; −5 V <V_{CANH}< +10 V
Common Mode input resistance at CANH	$R_{i(CM)(CANH)}$	15	25	37	kΩ	
Common Mode input resistance at CANL	$R_{i(CM)(CANL)}$	15	25	37	kΩ	
Matching between Common Mode input resistance at CANH, CANL	$R_{i(CM)(m)}$	−3	0	+3	%	$V_{CANL} = V_{CANH}$
Differential input resistance	$R_{i(diff)}$	25	50	75	kΩ	
Input capacitance, CANH	$C_{i(CANH)}$		7.5	20	pF	$V_{TxD} = V_{DD1}$
Input capacitance, CANL	$C_{i(CANL)}$		7.5	20	pF	$V_{TxD} = V_{DD1}$
Differential input capacitance	$C_{i(dif)}$		3.75	10	pF	$V_{TxD} = V_{DD1}$
Input leakage current at CANH	$I_{LI(CANH)}$	100	170	250	µA	V_{CANH}= 5 V, V_{DD2}= 0
Input leakage current at CANL	$I_{LI(CANL)}$	100	170	250	µA	V_{CANL}= 5 V, V_{DD2}= 0
Thermal Shutdown						
Shutdown junction temperature	$T_{j(SD)}$	155	165	180	°C	

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Timing Characteristics (60 Ω / 100 pF bus loading; 20 pF RxD load; see Fig. 1)						
Parameter	**Symbol**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
TxD to bus active delay	$t_{d(TxD\text{-}BUSon)}$	44 36	93 96	160 128	ns	V_S= 0 V; V_{DD1} = 5 V V_S = 0 V; V_{DD1} = 3.3 V
TxD to bus inactive delay	$t_{d(TxD\text{-}BUSoff)}$	34 37	68 71	110 113	ns	V_S = 0 V; V_{DD1} = 5 V V_S = 0 V; V_{DD1} = 3.3 V
Bus active to RxD delay	$t_{d(BUSon\text{-}RxD)}$	29 32	63 66	125 128	ns	V_S = 0 V; V_{DD1} = 5 V V_S = 0 V; V_{DD1} = 3.3 V
Bus inactive to RxD delay	$t_{d(BUSoff\text{-}RxD)}$	69 72	108 111	170 173	ns	V_S = 0 V; V_{DD1} = 5 V V_S = 0 V; V_{DD1} = 3.3 V
Loop delay low-to-high or high-to-low	T_{LOOP}	74	180	210	ns	V_S = 0 V; "Typ." at 25°C and nominal loads
TxD dominant time for timeout	$T_{dom(TxD)}$	250	457	765	µs	V_{TxD} = 0 V 3.0 V > V_{DD1} < 5.5 V
Common Mode Transient Immunity (TxD Logic High or Logic Low)	$\|CM_H\|,\|CM_L\|$	30	50		kV/µs	R_L = 60 Ω; V_{CM} = 1500 V_{DC}; $t_{TRANSIENT}$ = 25 ns

Magnetic Field Immunity[3] (V_{DD2}= 5V, 3V<V_{DD1}<5.5V)						
Power Frequency Magnetic Immunity	H_{PF}	4000	6000		A/m	50Hz/60Hz
Pulse Magnetic Field Immunity	H_{PM}	6000	7000		A/m	t_p = 8µs
Damped Oscillatory Magnetic Field	H_{OSC}	6000	7000		A/m	0.1Hz – 1MHz
Cross-axis Immunity Multiplier	K_X		2			See Fig. 4

Notes:

1. The TxD input is edge sensitive. Voltage magnitude of the input signal is specified, but edge rate specifications must also be met.
2. The maximum time allowed for a logic transition at the TxD input is 1 µs.
3. Test and measurement methods are given in the Electromagnetic Compatibility section on p. 10.
4. If V_{DD2} falls below the specified failsafe supply voltage, RxD will go High.

Timing Test Circuit

Timing parameters are measured with 60 Ω / 100 pF bus line loading and 20 pF on RxD as shown in Figure 1 below:

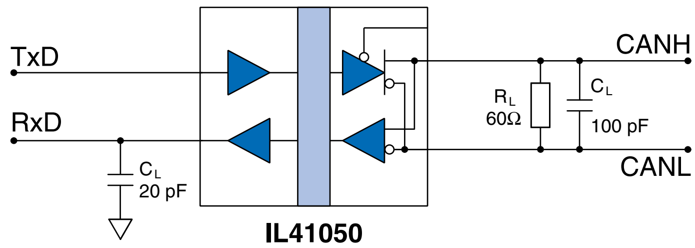

Figure 1. Timing characteristics test circuit.

Block Diagram

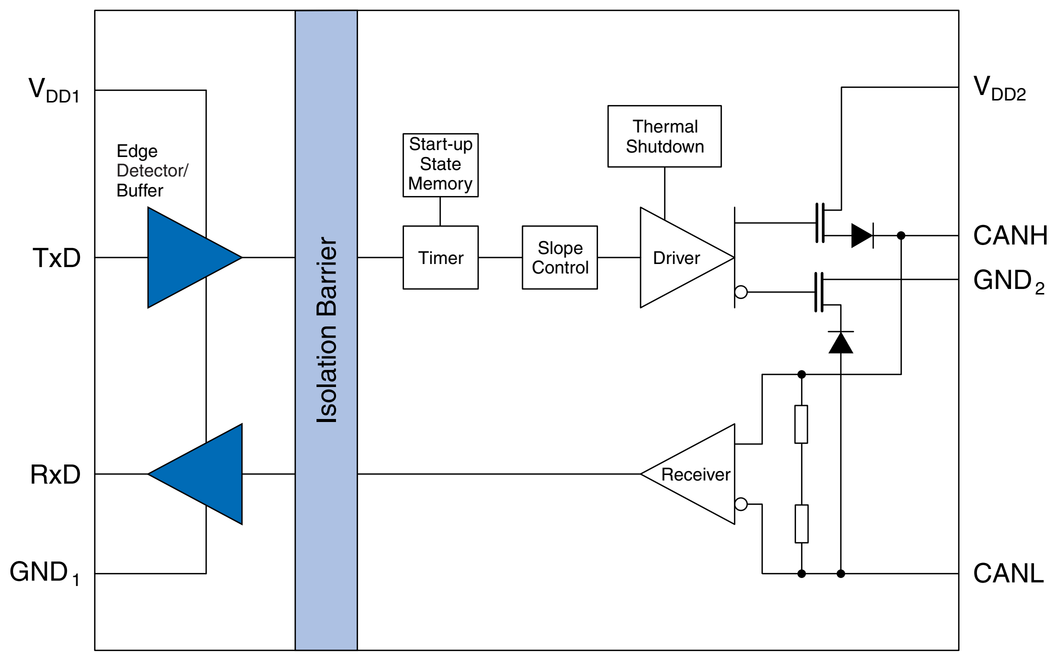

Figure 2. IL41050TT detailed functional diagram.

Application Information

As Figure 3 shows, the IL41050TT can provide isolation and level shifting between a 5 volt CAN bus and a 3 volt microcontroller:

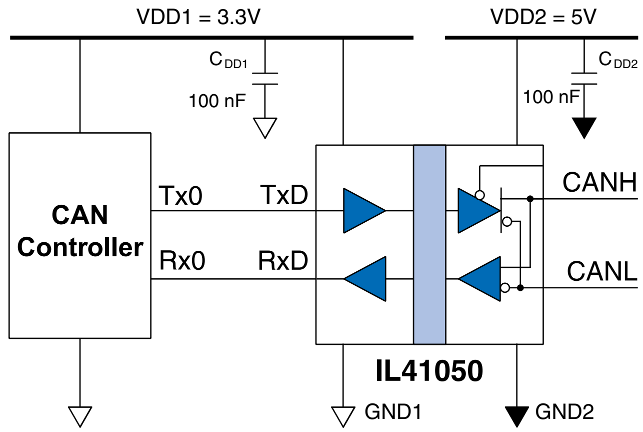

Figure 3. Isolated CAN node using the IL41050TT.

Power Supply Decoupling

Both V_{DD1} and V_{DD2} must be bypassed with 100 nF ceramic capacitors. These supply the dynamic current required for the isolator switching and should be placed as close as possible to V_{DD} and their respective ground return pins.

Maintaining Creepage

Creepage distances are often critical in isolated circuits. In addition to meeting JEDEC standards, NVE isolator packages have unique creepage specifications. Standard pad libraries often extend under the package, compromising creepage and clearance. Similarly, ground planes, if used, should be spaced to avoid compromising clearance. Package drawings and recommended pad layouts are included in this datasheet.

Input Configurations

The TxD input should not be left open as the state will be indeterminate. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 kΩ) should be connected from the input to V_{DD1}.

Dominant Mode Time-out and Failsafe Receiver Functions

CAN bus latch up is prevented by an integrated Dominant mode timeout function. If the TxD pin is forced permanently low by hardware or software application failure, the time-out returns the RxD output to the high state no more than 765 µs after TxD is asserted dominant. The timer is triggered by a negative edge on TxD. If the duration of the low is longer than the internal timer value, the transmitter is disabled, driving the bus to the recessive state. The timer is reset by a positive edge on pin TxD.

If power is lost on Vdd2, the IL41050 asserts the RxD output high when the supply voltage falls below 3.8 V. RxD will return to normal operation when Vdd2 rises above approximately 4.2 V.

Programmable Power-Up

A unique non-volatile programmable power-up feature prevents unstable nodes. A state that needs to be present at node power up can be programmed at the last power down. For example if a CAN node is required to “pulse” dominant at power up, TxD can be sent low by the controller immediately prior to power down. When power is resumed, the node will immediately go dominant allowing self-check code in the microcontroller to verify node operation. If desired, the node can also power up silently by presetting the TxD line high at power down. At the next power on, the IL41050 will remain silent, awaiting a dominant state from the bus.

The microcontroller can check that the CAN node powered down correctly before applying power at the next “power on” request. If the node powered down as intended, RxD will be set high and stored in the IL41050’s non-volatile memory. The level stored in the RxD bit can be read before isolated node power is enabled, avoiding possible CAN bus disruption due to an unstable node.

Replacing Non-Isolated CAN Transceivers

The IL41050 is designed to replace common non-isolated CAN transceivers such as the Philips/NXP TJA1050 with minimal circuit changes. Some notable differences:

- Some non-isolated CAN transceivers have internal TxD pull-up resistors, but the IL41050 TxD input should not be left open. If connected to an open-drain or open collector output, a pull-up resistor (typically 16 kΩ) should be connected from the input to V_{DD1}.
- Initialization behavior varies between CAN transceivers. To ensure the desired power-up state, the IL41050 should be initialized with a TxD pulse (low-to-high for recessive initialization), or shut down the transceiver in the desired power-up state (the "programmable power-up feature").
- Many non-isolated CAN transceivers have a "sleep mode" select input ("S") or V_{REF} output. These pins are not available on the IL41050TT. Please select the NVE IL41050TA if these pins are required.

Replacing Other Isolated CAN Transceivers

The IL41050TT is a pin-for-pin direct replacement for the Texas Instruments ISO1050DW Isolated CAN Transceiver, with advantages of much better reliability and longer barrier life, less EMI emissions, and true 8 mm external creepage per IEC 60601.

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Electrostatic Discharge Sensitivity

This product has been tested for electrostatic sensitivity to the limits stated in the specifications. However, NVE recommends that all integrated circuits be handled with appropriate care to avoid damage. Damage caused by inappropriate handling or storage could range from performance degradation to complete failure.

Electromagnetic Compatibility

The IL41050 is fully compliant with generic EMC standards EN50081, EN50082-1 and the umbrella line-voltage standard for Information Technology Equipment (ITE) EN61000. The IsoLoop Isolator's Wheatstone bridge configuration and differential magnetic field signaling ensure excellent EMC performance against all relevant standards. NVE conducted compliance tests in the categories below:

EN50081-1
Residential, Commercial & Light Industrial
Methods EN55022, EN55014

EN50082-2: Industrial Environment
Methods EN61000-4-2 (ESD), EN61000-4-3 (Electromagnetic Field Immunity), EN61000-4-4 (Electrical Transient Immunity), EN61000-4-6 (RFI Immunity), EN61000-4-8 (Power Frequency Magnetic Field Immunity), EN61000-4-9 (Pulsed Magnetic Field), EN61000-4-10 (Damped Oscillatory Magnetic Field)

ENV50204
Radiated Field from Digital Telephones (Immunity Test)

Immunity to external magnetic fields is higher if the field direction is "end-to-end" (rather than to "pin-to-pin") as shown in the diagram below:

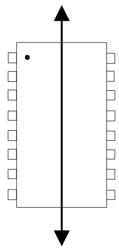
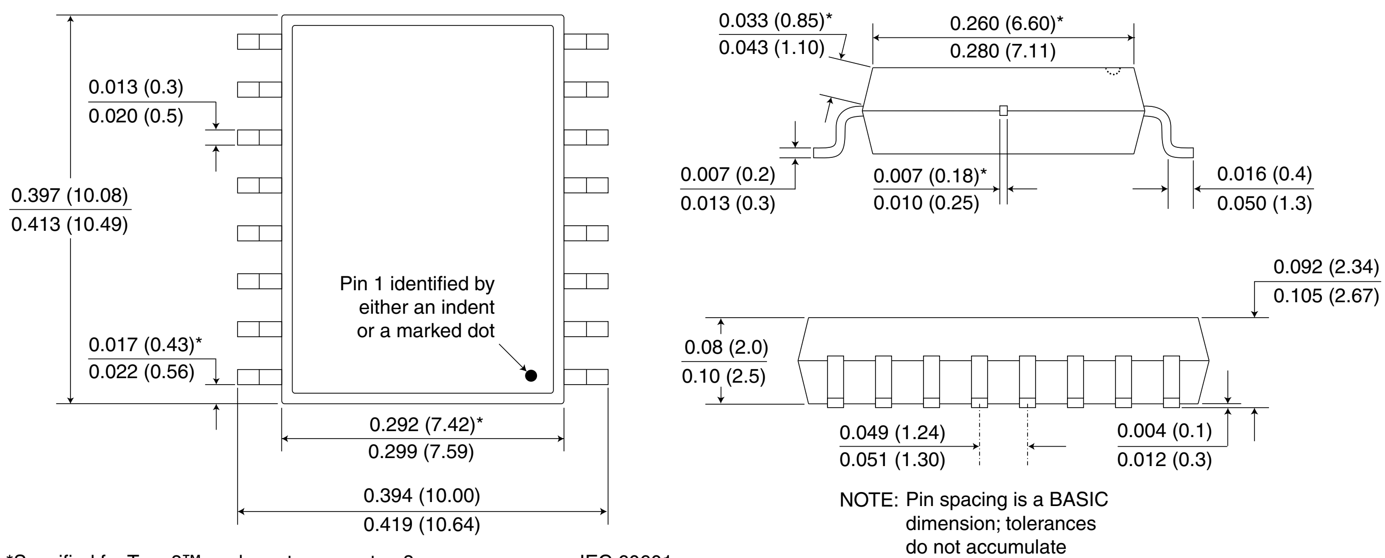


Figure 4. Orientation for high field immunity.

Package Drawing

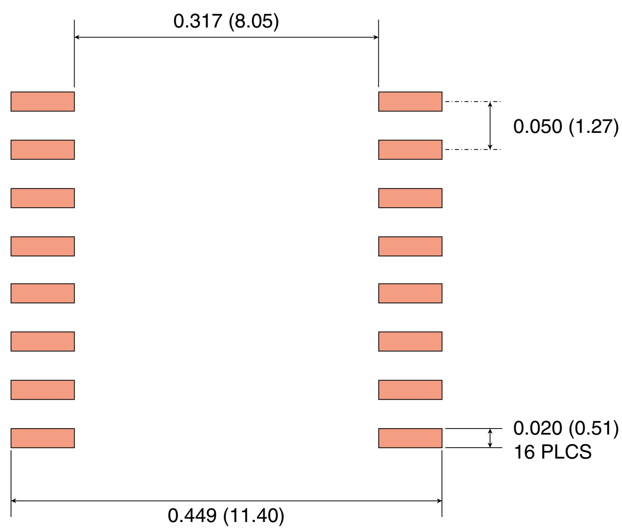
Dimensions in inches (mm); scale = approx. 5X



*Specified for True 8™ package to guarantee 8 mm creepage per IEC 60601.

Recommended Pad Layout

Dimensions in inches (mm); scale = approx. 5X



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Ordering Information

IL 41050 TTVE TR13

Bulk Packaging
Blank = Tube(50pcs)

TR13 = 13" Tape and Reel
(1500pcs)

Package
E = RoHS Compliant

Package Type
Blank = 2.5 kV isolation 0.3'' SOIC
V = 5 kV isolation 0.3'' SOIC

Transceiver Subtype
TT = Basic CAN Transceiver

Channel Configuration
1050 = CAN Transceiver

Base Part Number
4 = Isolated Transceiver

Product Family
IL = Isolators

RoHS
COMPLIANT

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Revision History

ISB-DS-001-IL41050TT-A **Nov. 2015**	**Changes** • Added 2.5 kV isolation version. • Initial Release at Rev. A.
ISB-DS-001-IL41050TT-PRELIM-3 **Oct. 2015**	**Changes** • Deleted non-applicable specification sections on p. 5.
ISB-DS-001-IL41050TT-PRELIM-2 **Sept. 2015**	**Changes** • Updated pin descriptions on p. 4.
ISB-DS-001-IL41050TT-PRELIM **Sept. 2015**	Preliminary Release

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An ISO 9001 Certified Company

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